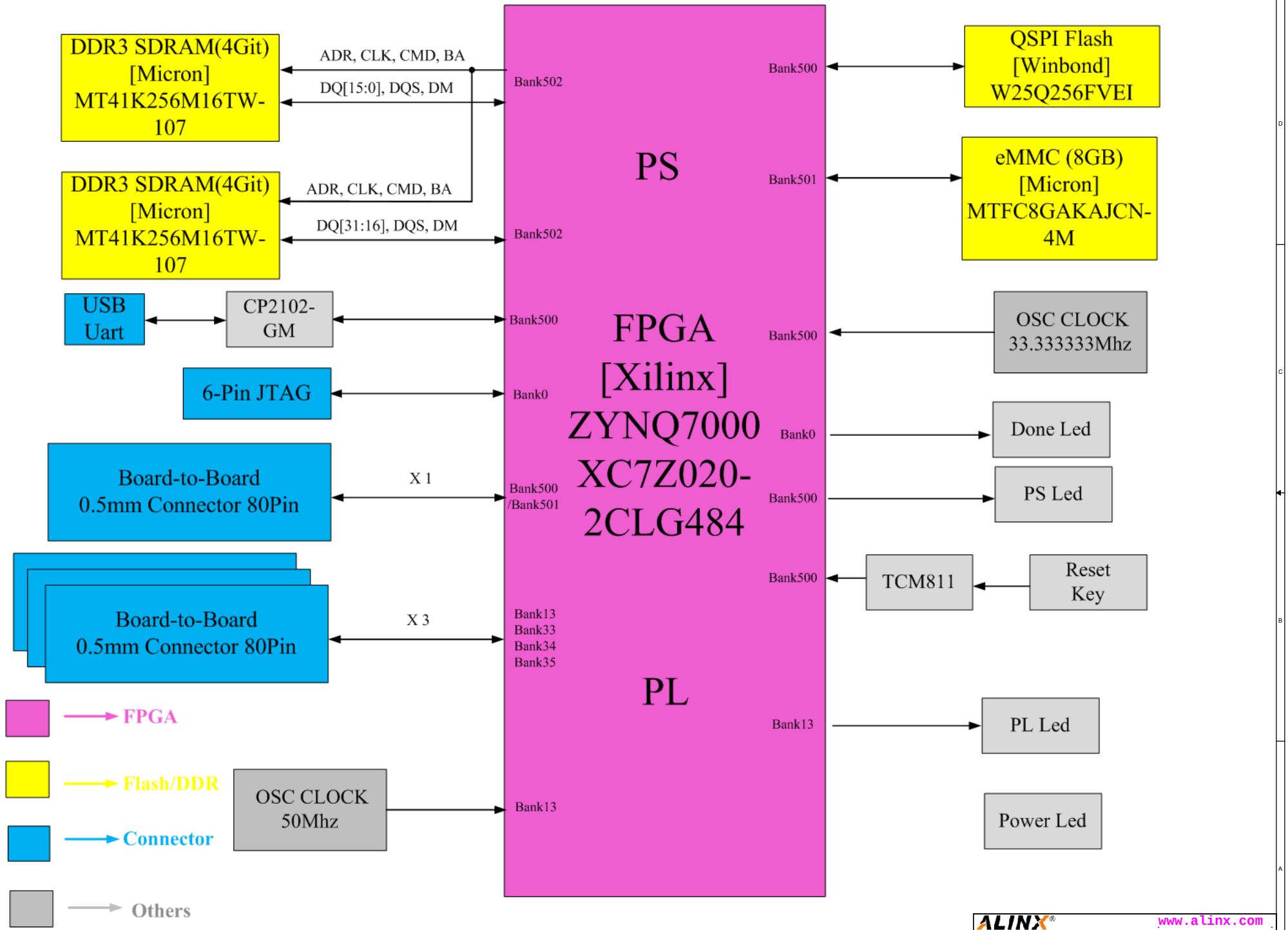

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Title	PAGE01 Block diagram	
Size	Document Number: AC7021B SOM Schematics	Rev 1.0
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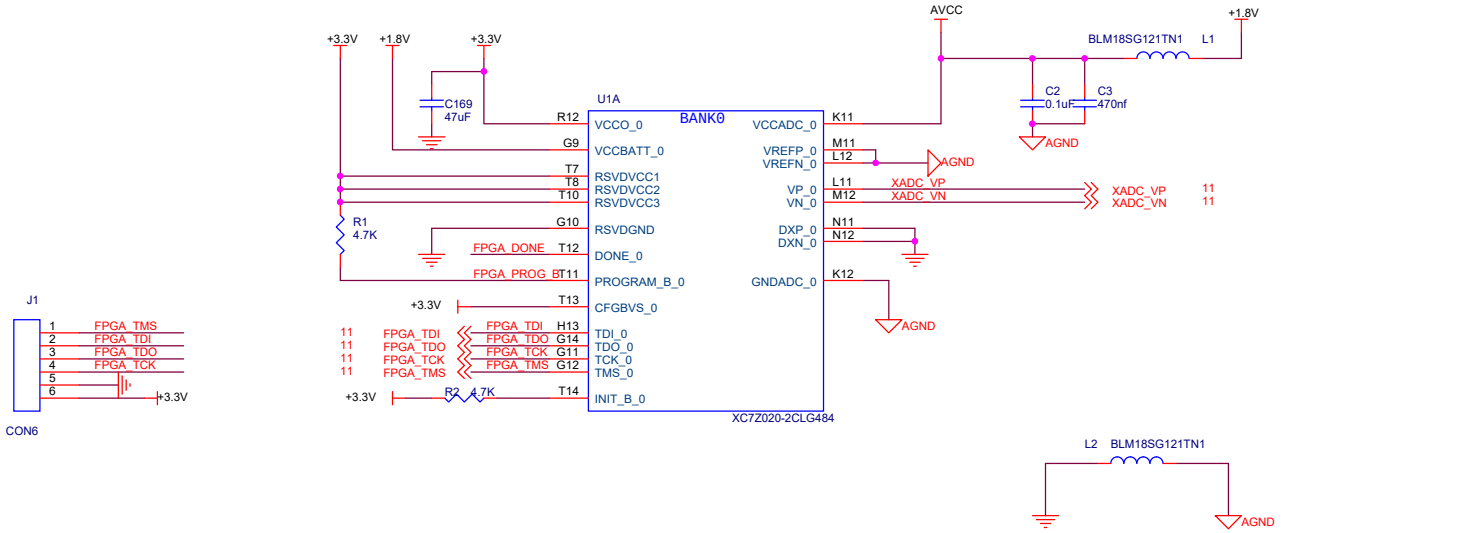

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Title	Page02 Z7 Bank0	
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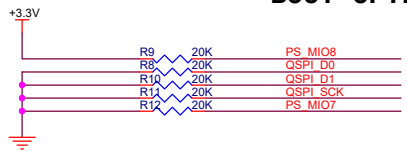
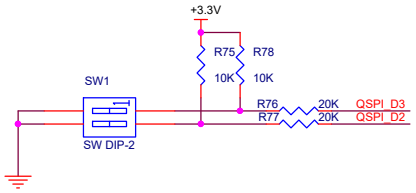
BOOT OPTION

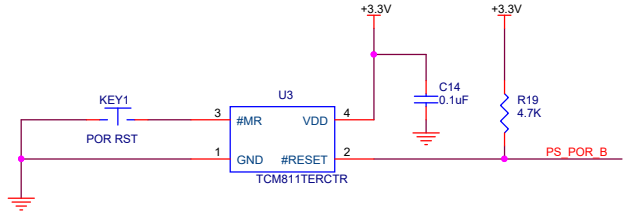


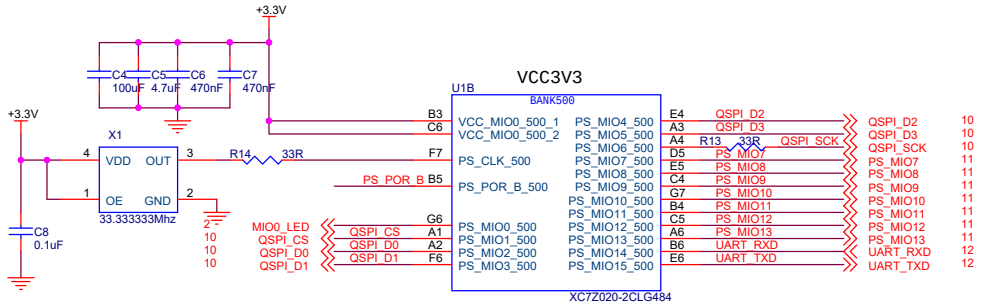
MIO[8] =1 ----MIO bank1 voltage=1.8V
MIO[2] =0 ----cascaded JTAG
MIO[3] =0 ----JTAG/NAND/Quad-SPI/SD
MIO[6] =0 ----PLL used
MIO[7] =0 ----MIO bank0 voltage=3.3V

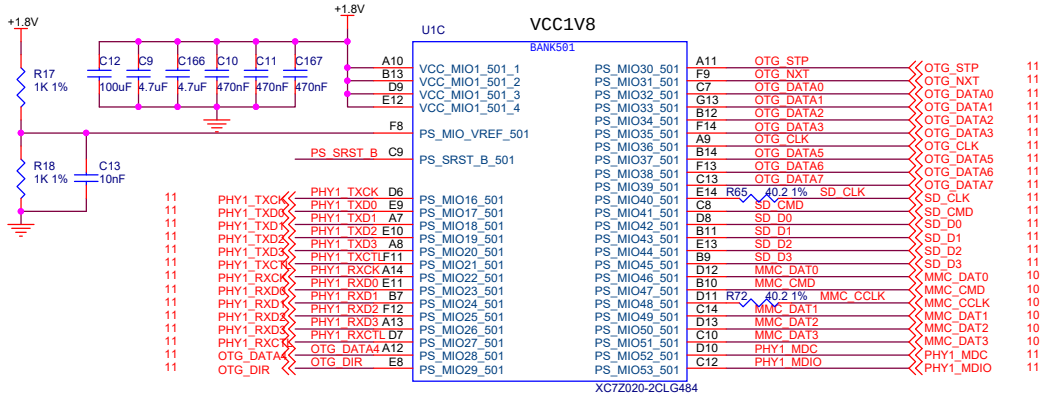


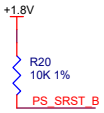
Boot Mode	MIO[5] (QSPI_D3)	MIO[4] (QSPI_D2)
JTAG	0	0
NAND	0	1
QSPI-FLASH	1	0
SD Card	1	1

POWER ON RESET









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Title: PAGE03 Z7 MIO-Config

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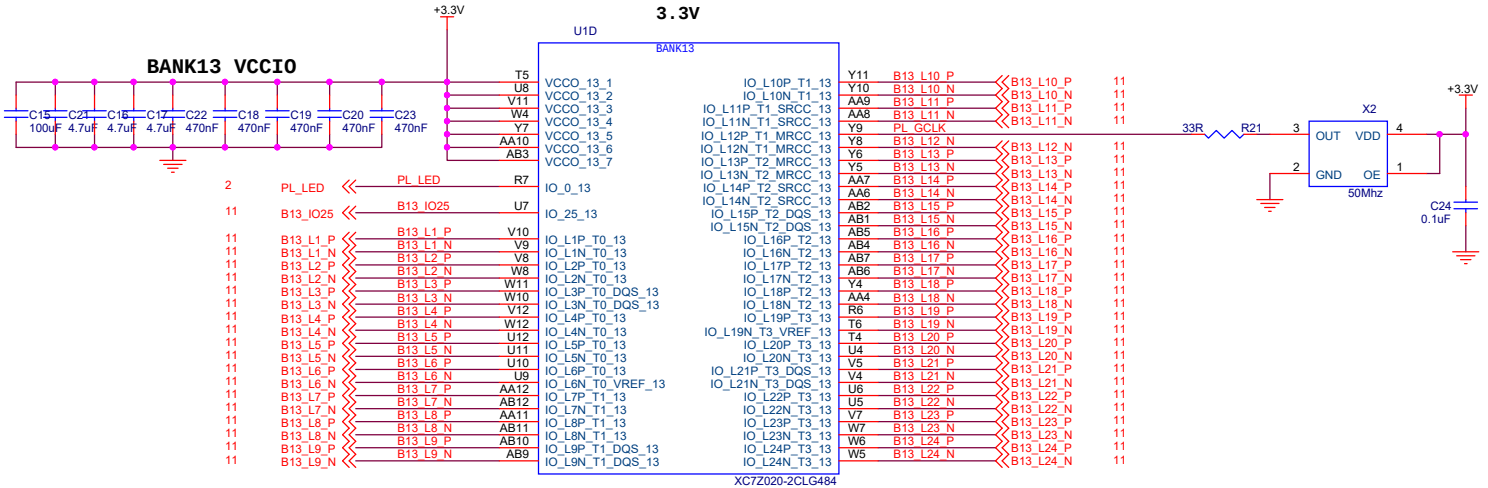

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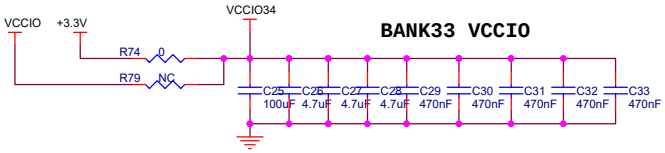
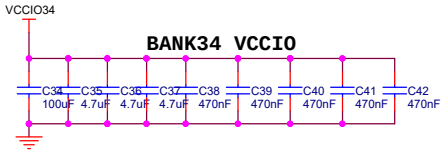
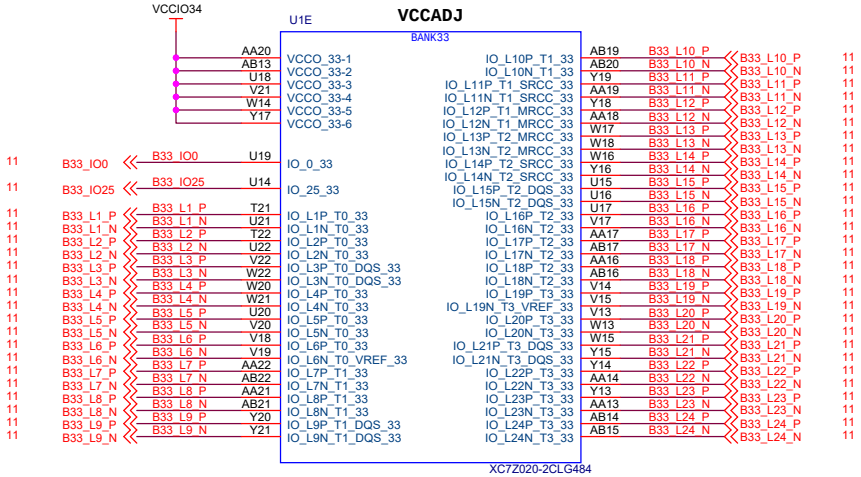
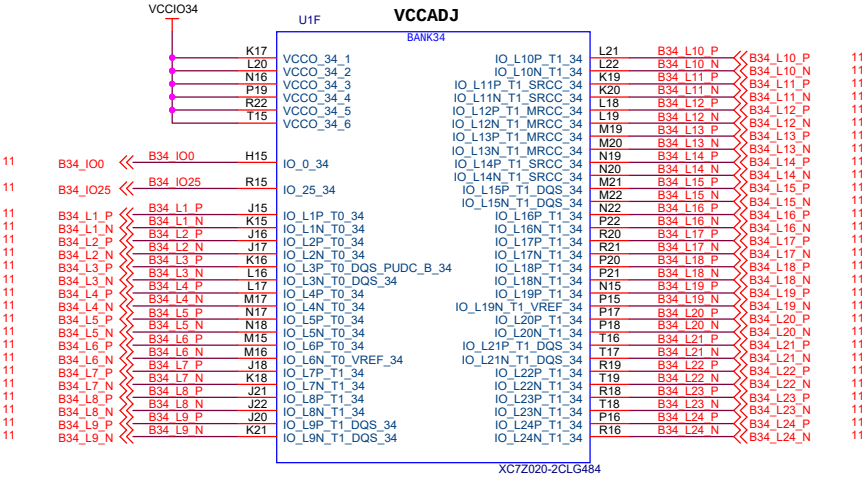
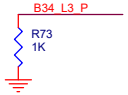








PUDC



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Title: PAGE05 Z7 Bank33 & Bank34

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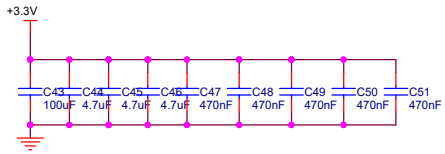

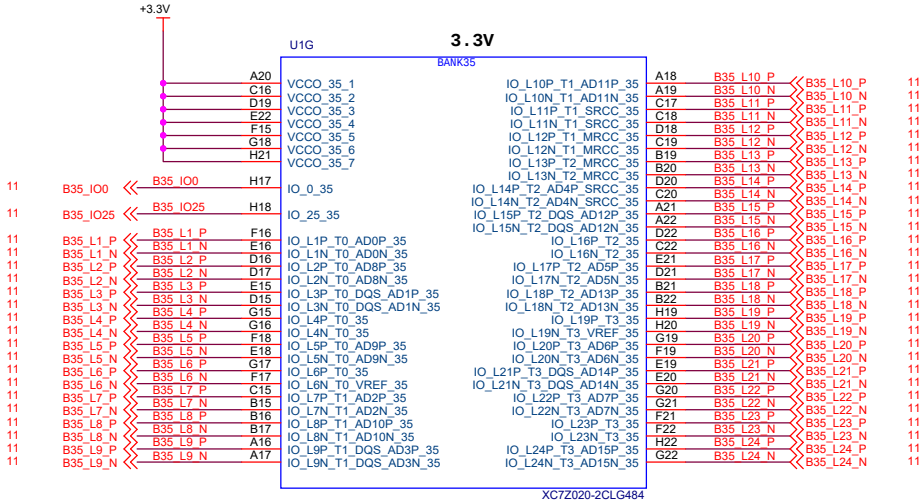

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Title: PAGE06 Z7 Bank35

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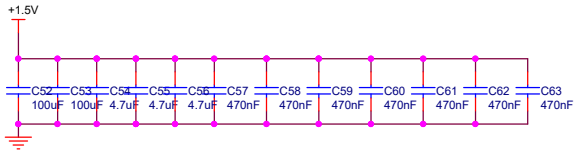

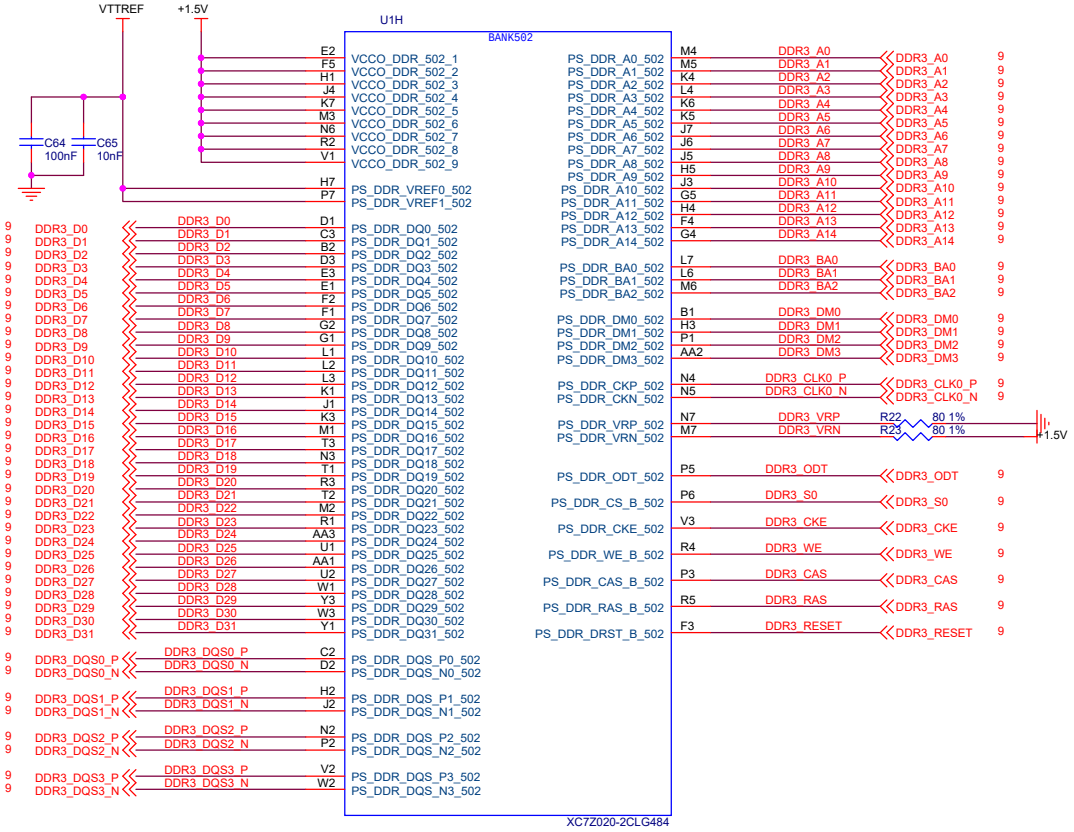

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Title: PAGE07 Z7 Bank502

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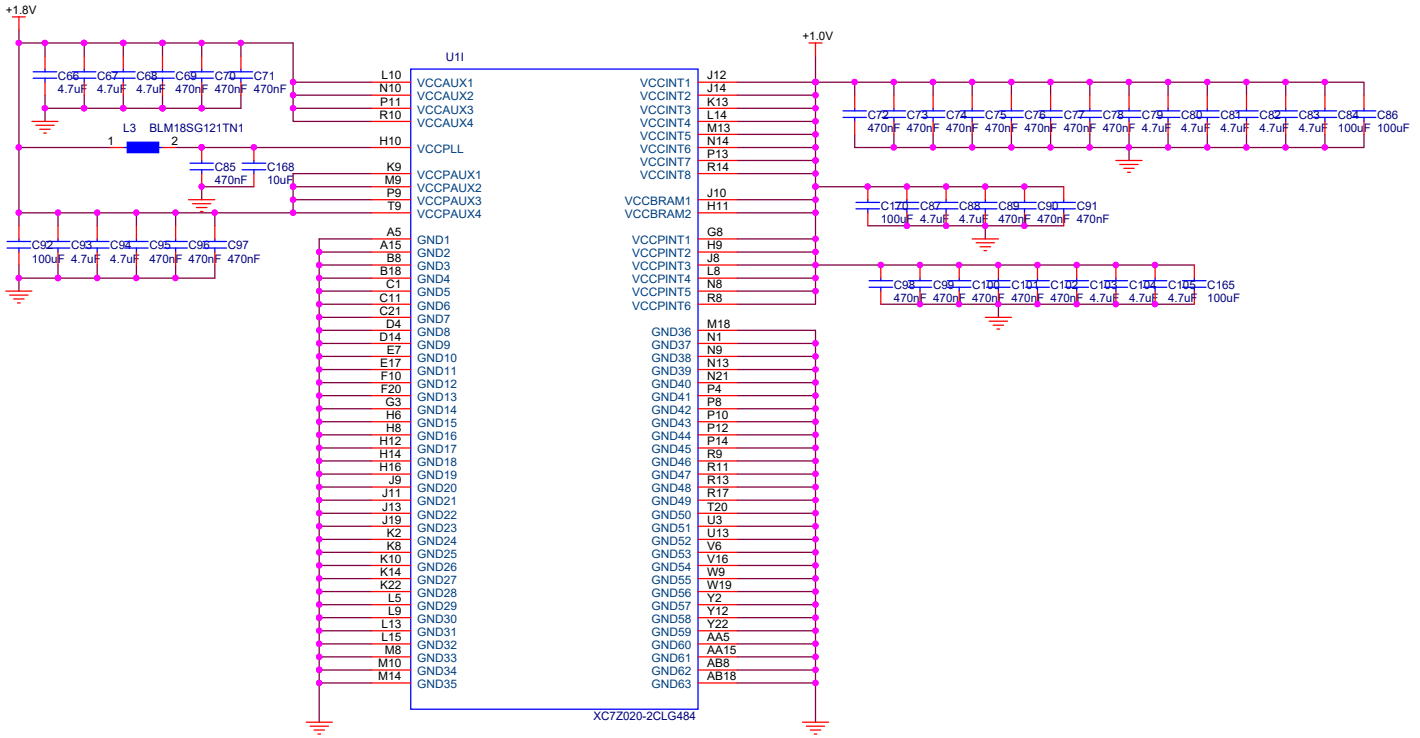

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Title: PAGE08 Z7 Power

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为了PCB走线方便，DDR3数据线组内（DQS除外）可以任意交换。
XILINX 的UG933文档的PAGE66有以下说明：

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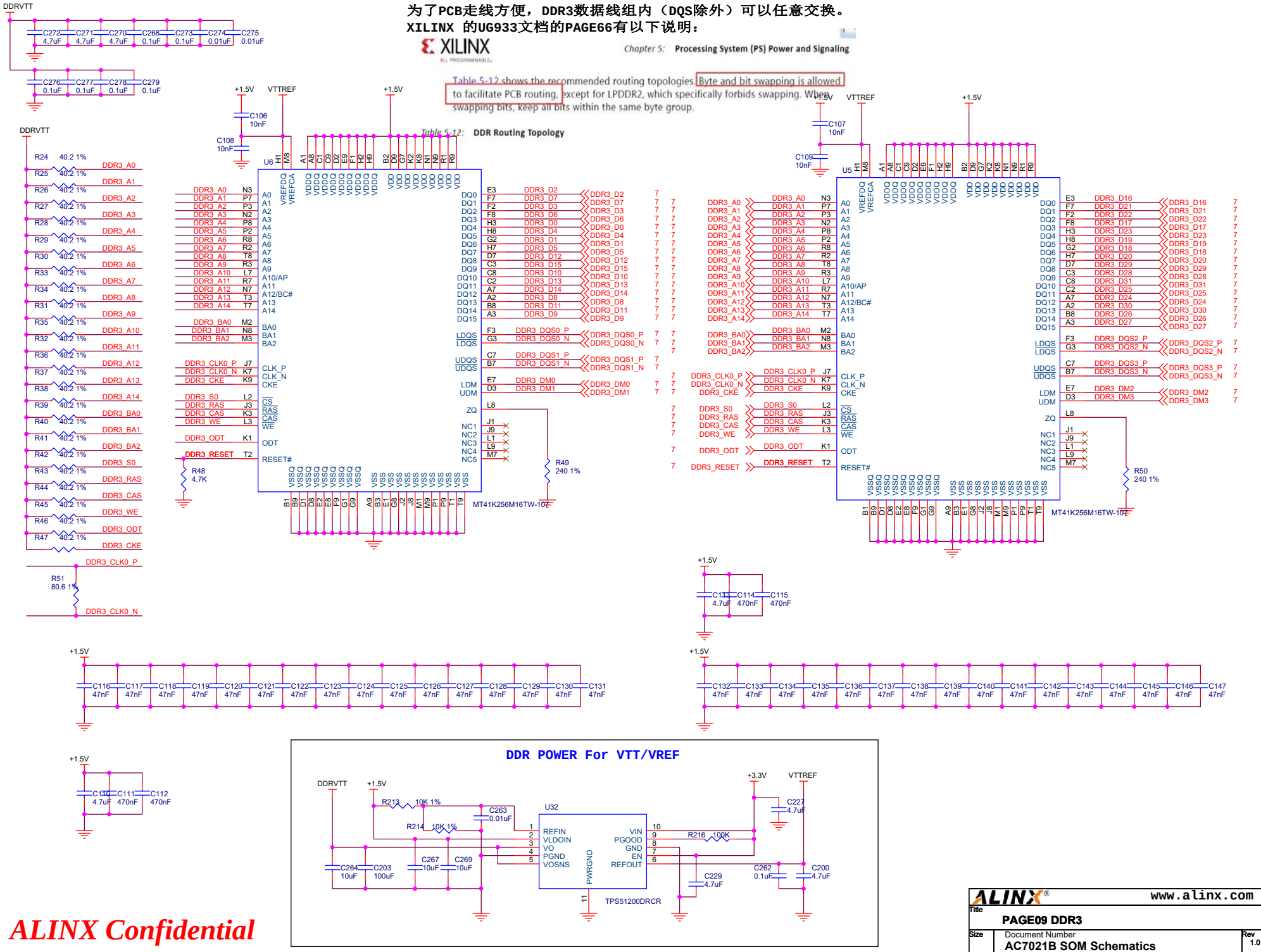
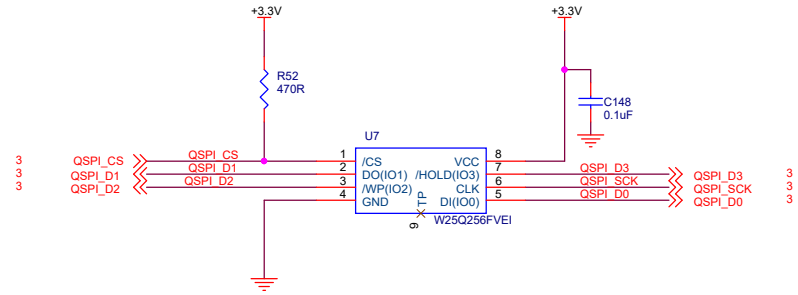
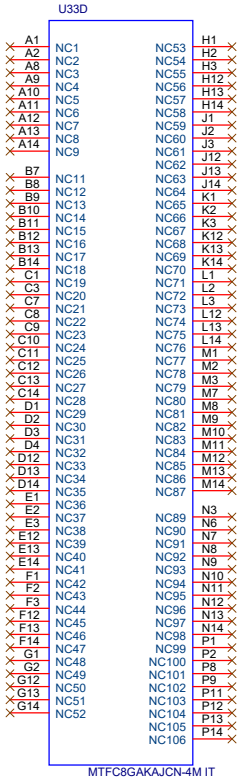
Chapter 5: **Processing System (PS) Power and Signaling**

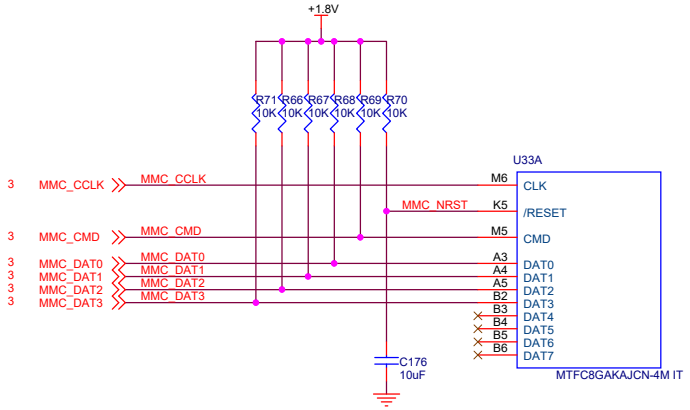
Table 5-12 shows the recommended routing topologies. Byte and bit swapping is allowed to facilitate PCB routing, except for LPDDR2, which specifically forbids swapping. When swapping bits, keep all bits within the same byte group.

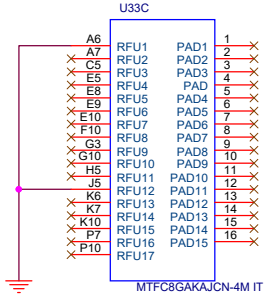
Table 5-12: **DDR Routing Topology**

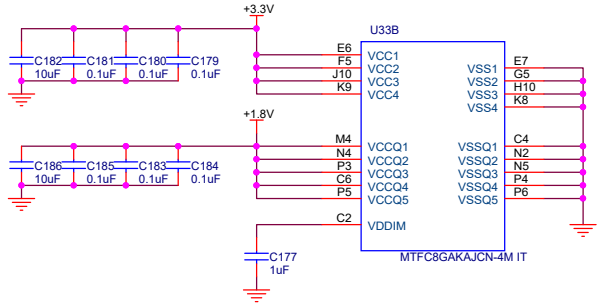












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Title: PAGE10 eMMC & QSPI FLASH		
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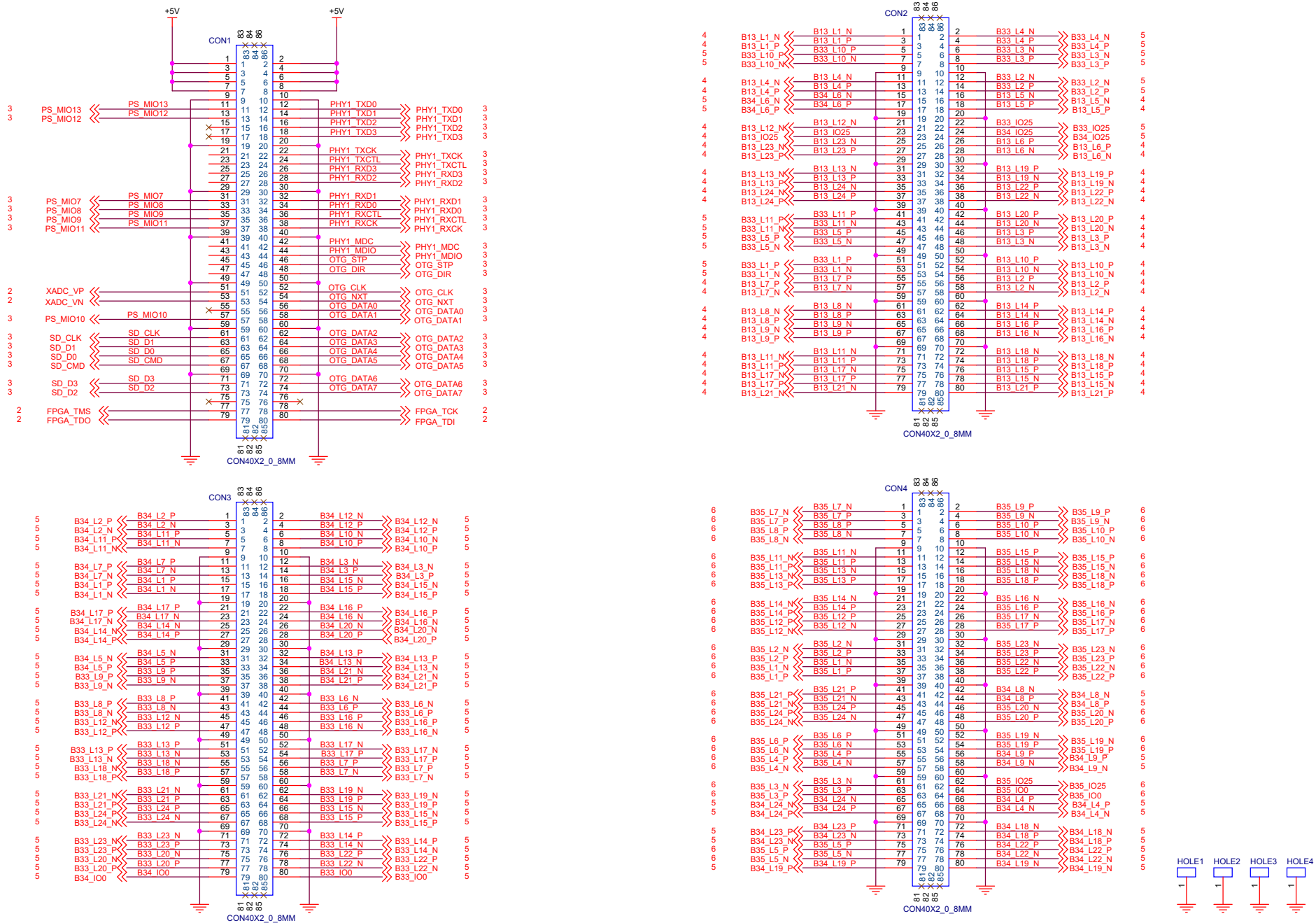

BANK33, BANK34 IO Voltage is adjustable

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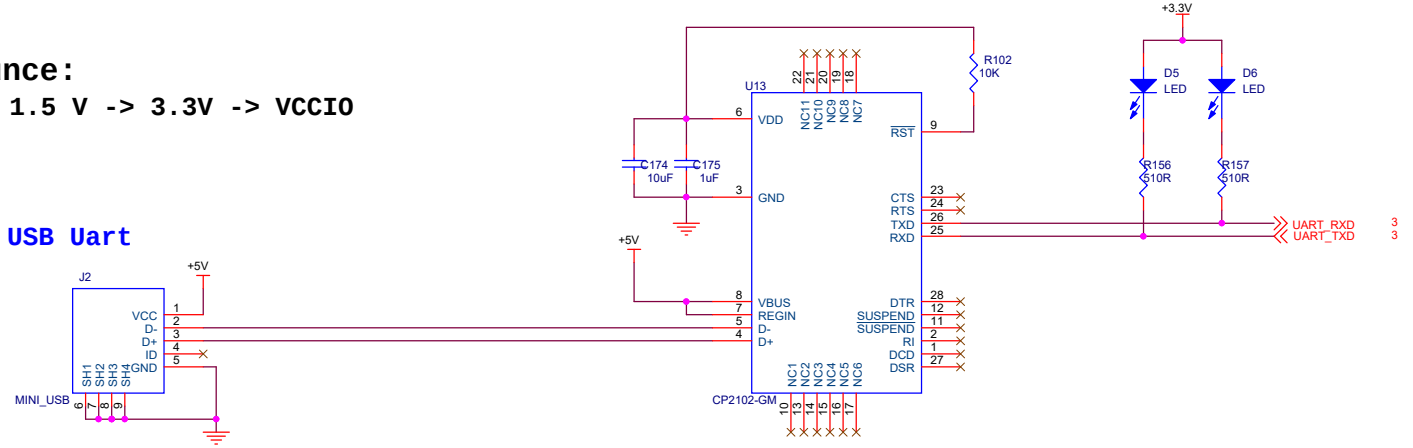
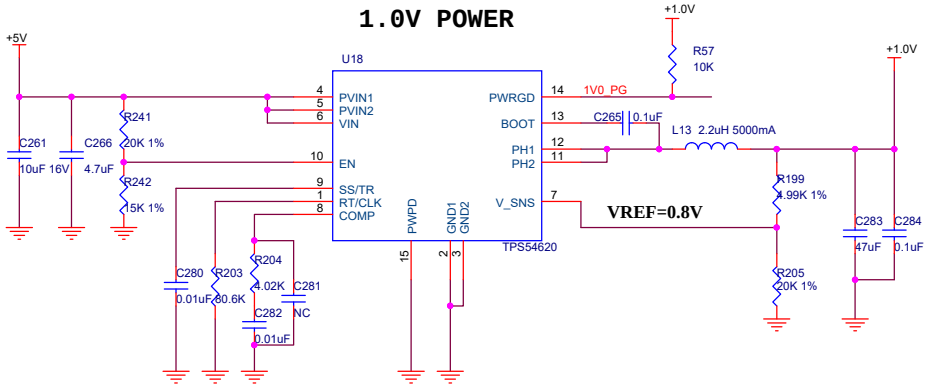
Power On Sequnce:

1.0V -> 1.8V -> 1.5 V -> 3.3V -> VCCIO

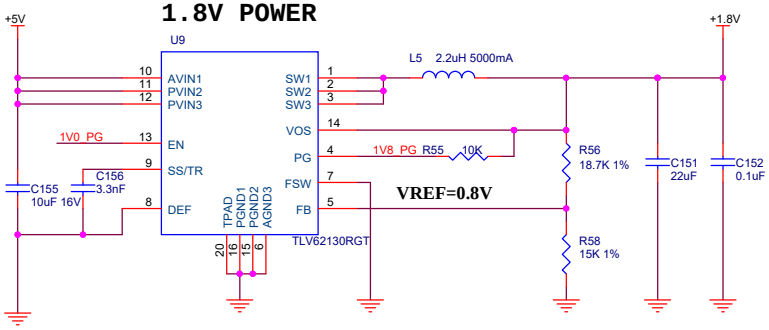
USB Uart



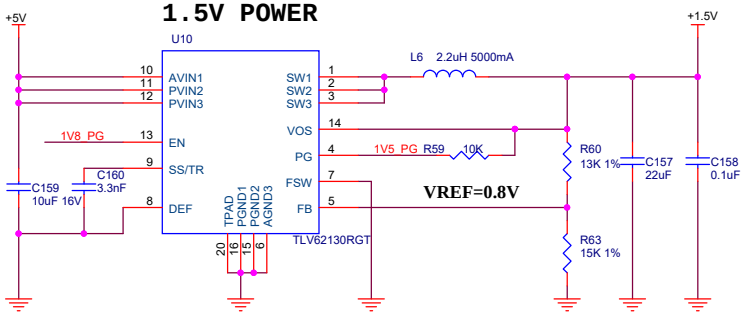
1.0V POWER



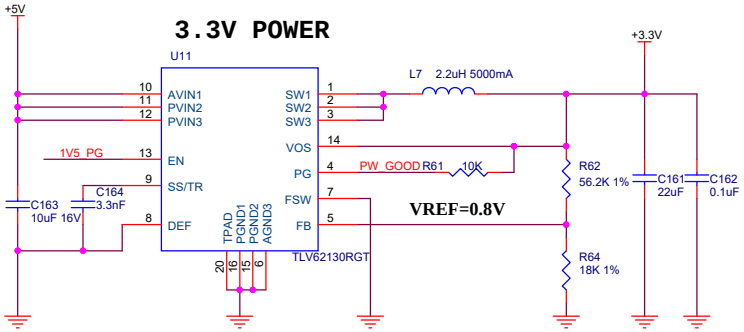
1.8V POWER

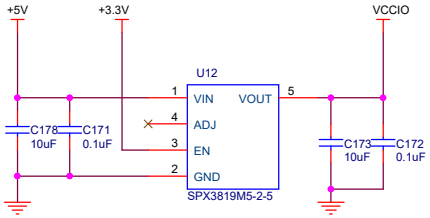


1.5V POWER



3.3V POWER





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Date:	Monday, March 30, 2020 — Sheet 12 of 12