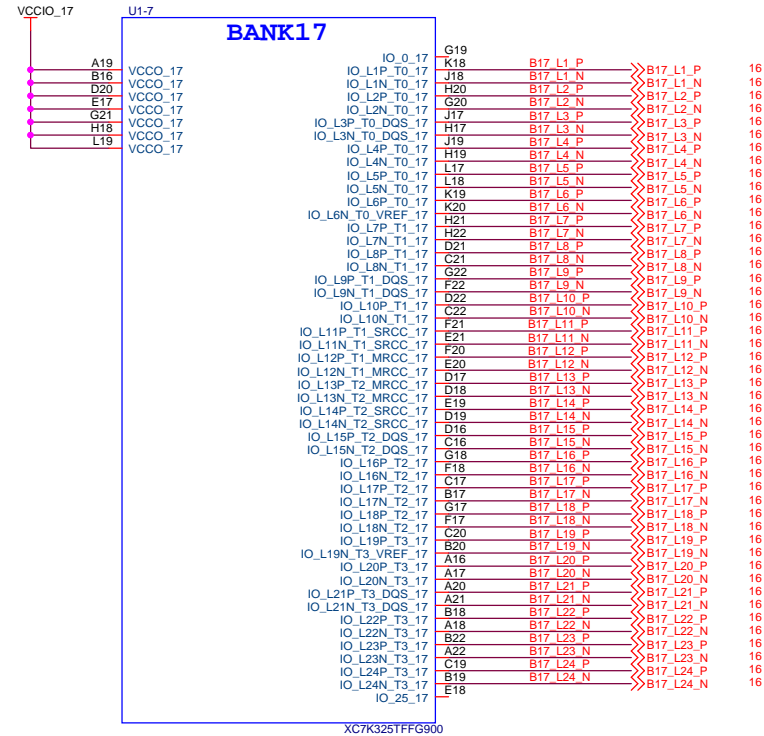
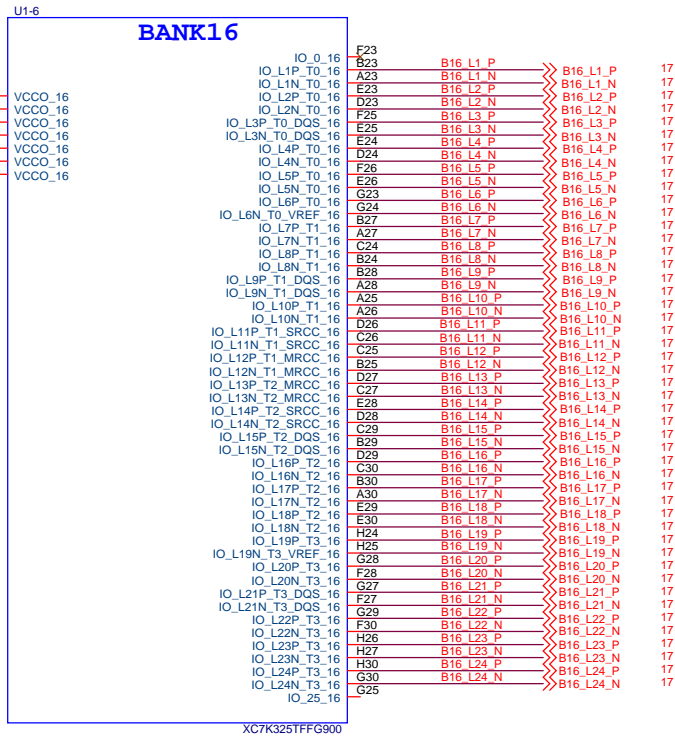
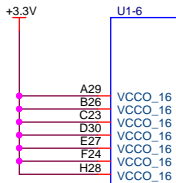
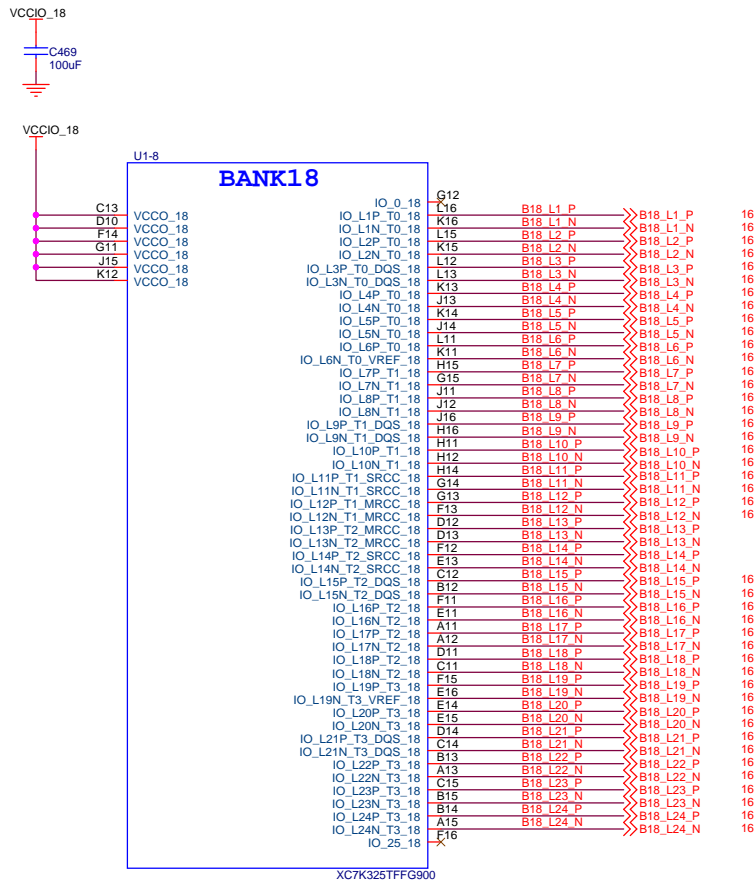
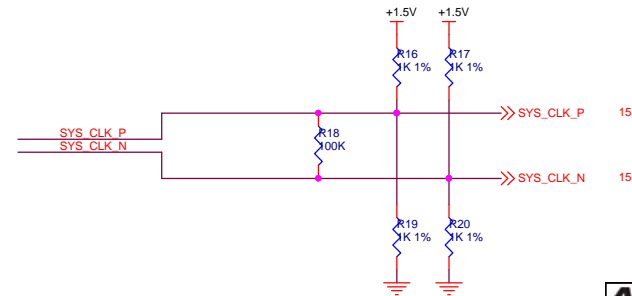
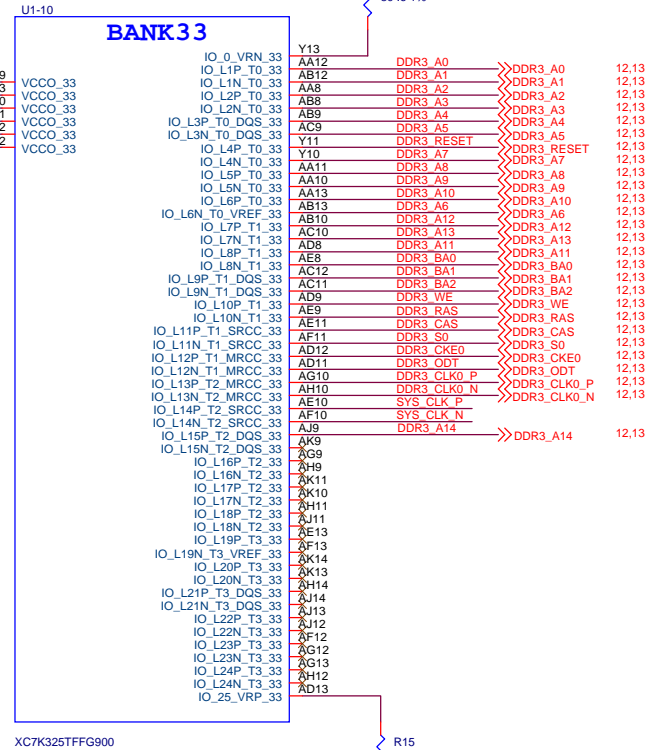
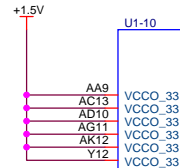
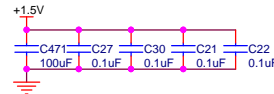
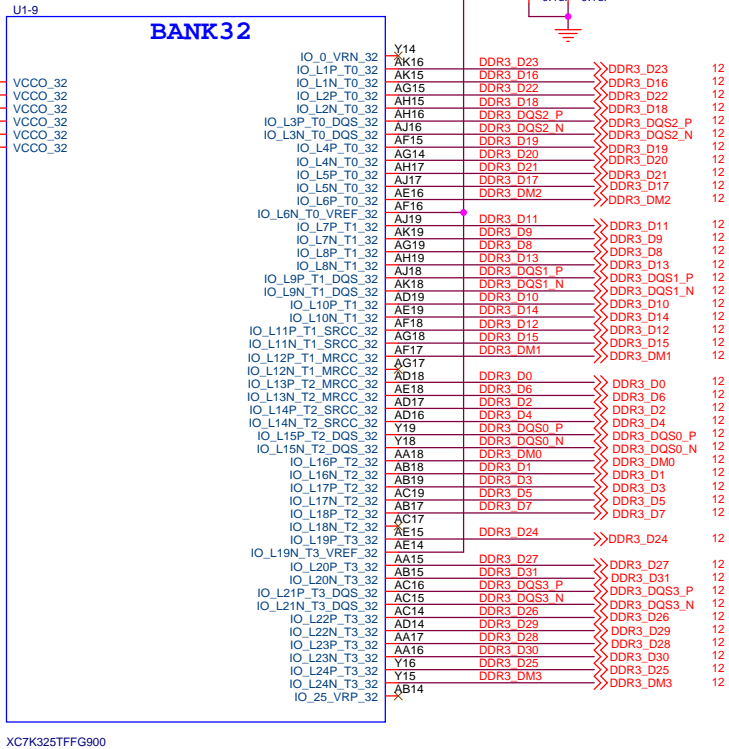
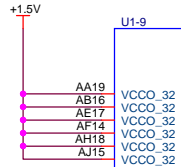
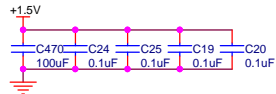


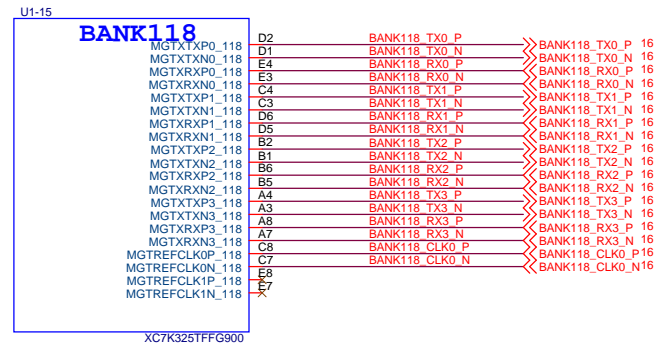
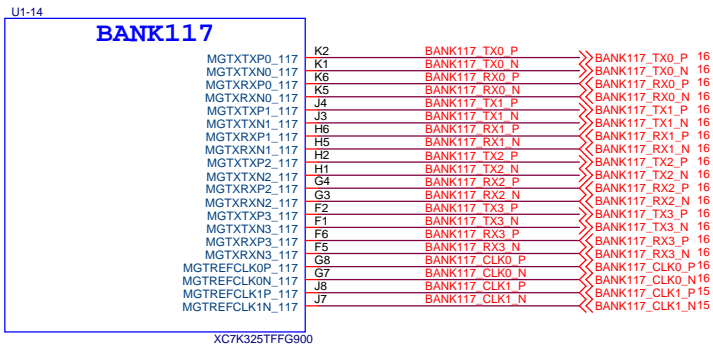
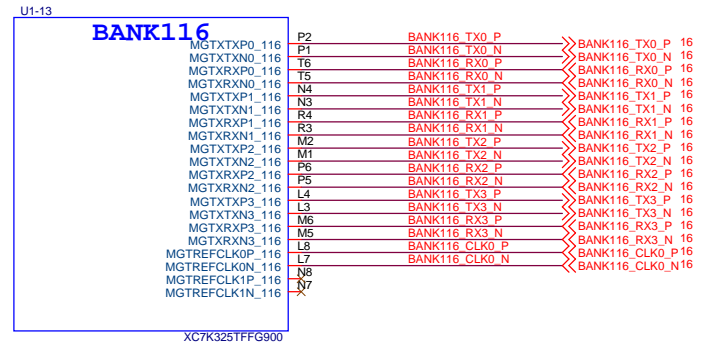
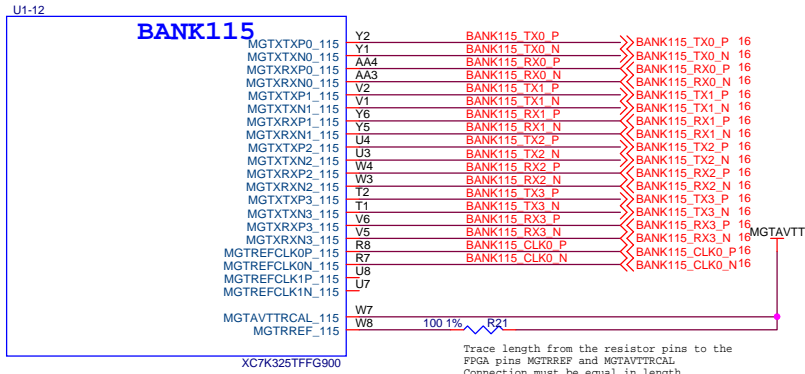
PUDC_B=1: Deactive internal Pull up Resister

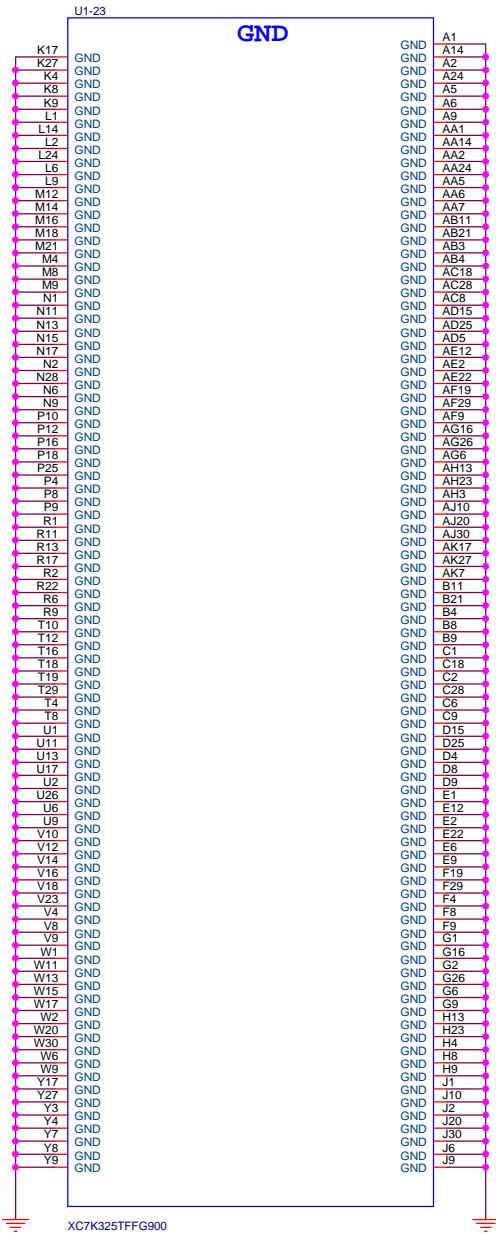


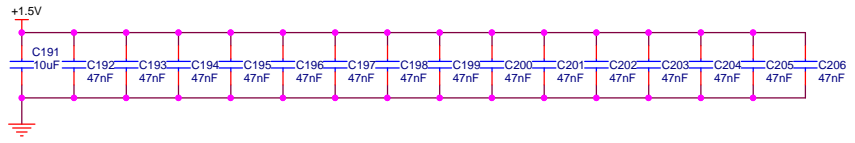
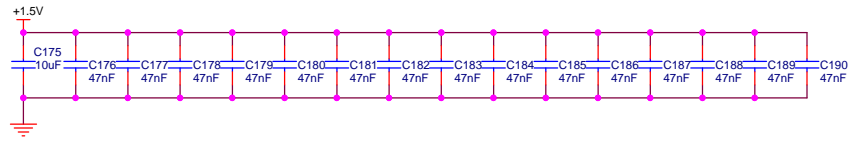
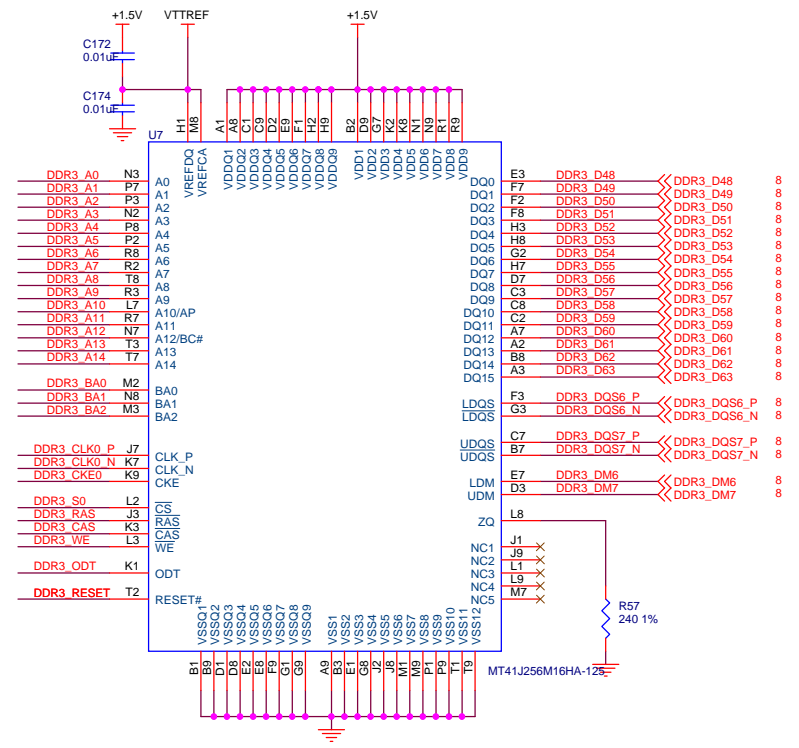
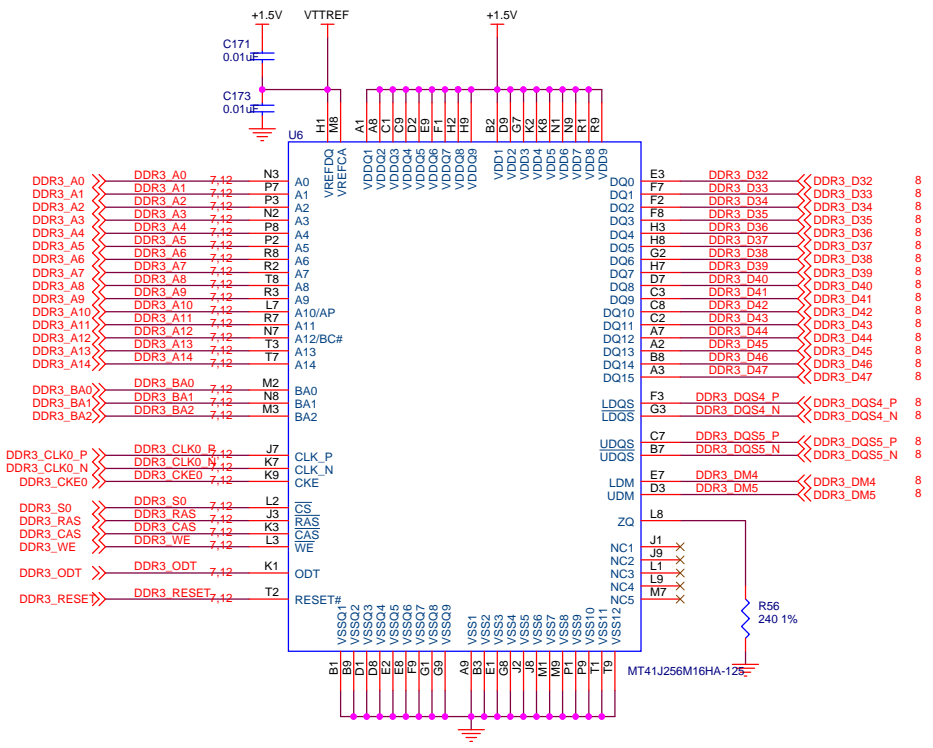
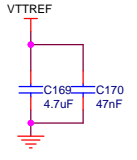
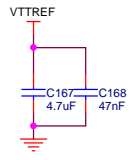




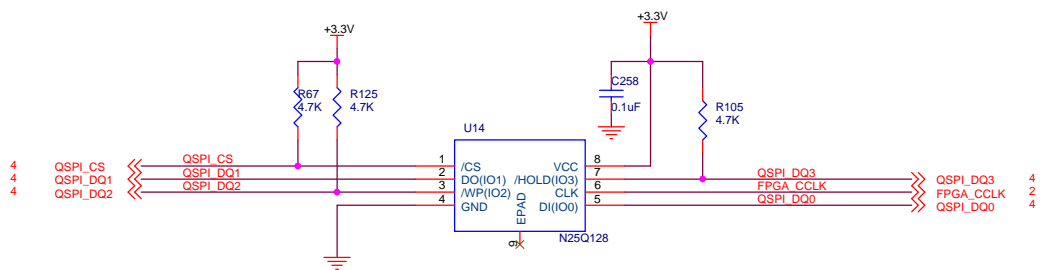






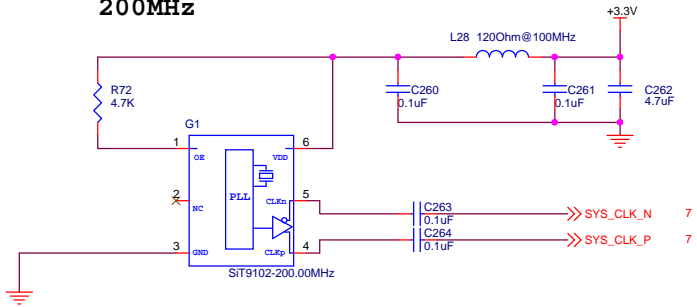


FPGA CONFIG SPI



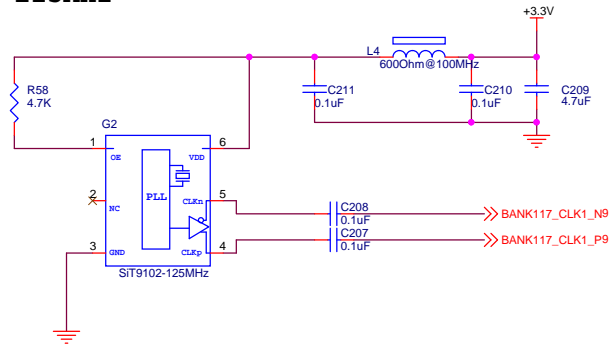
SYSTEM CLOCK

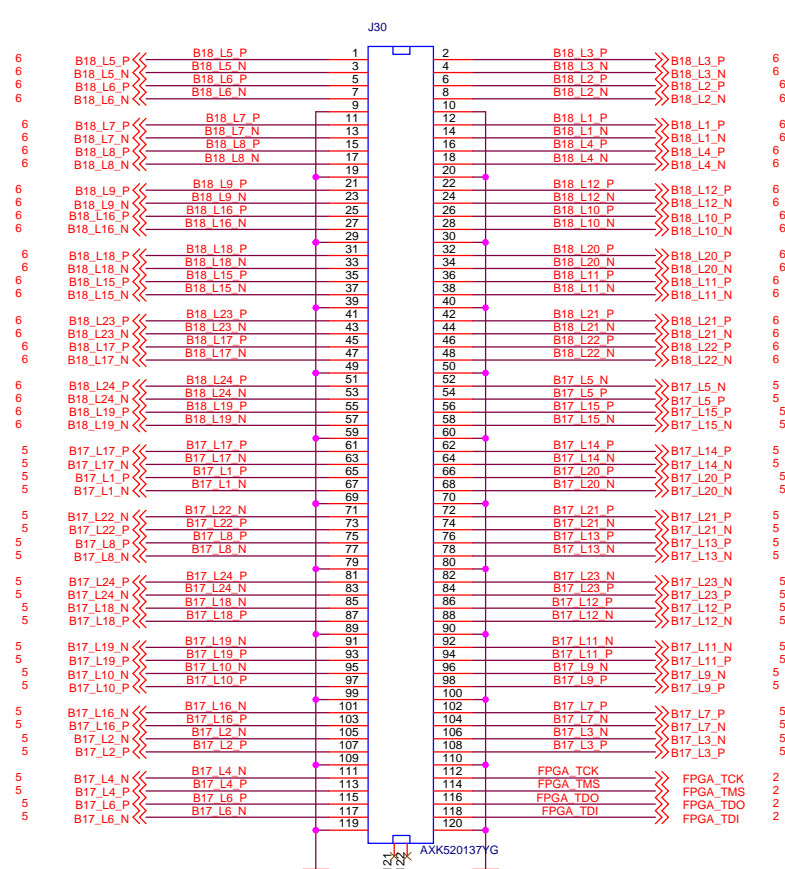
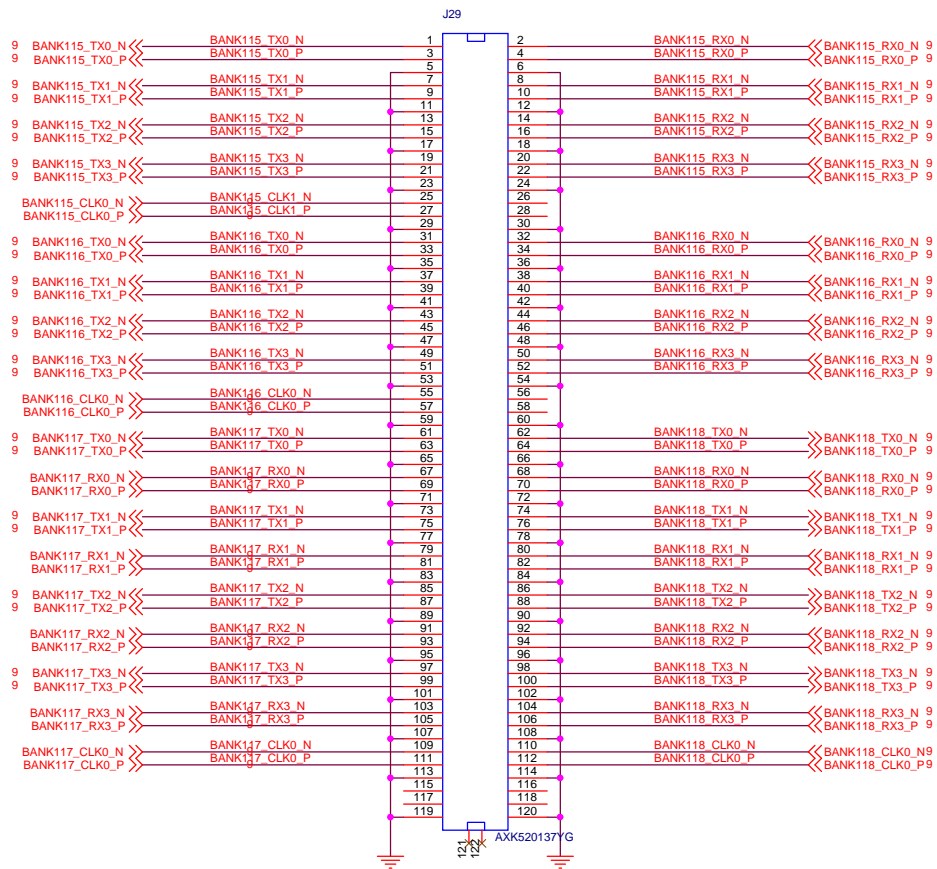
200MHz



GTX CLOCK

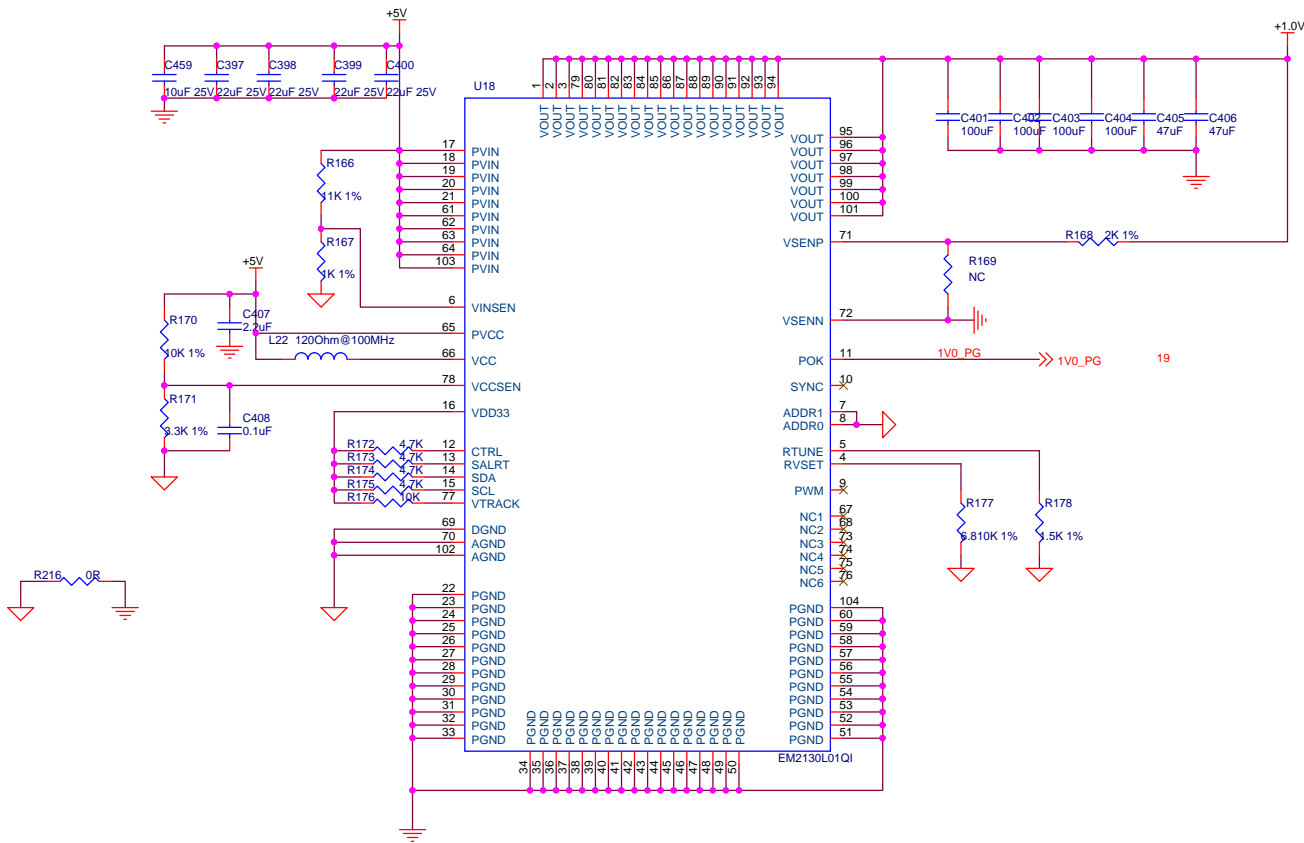
125MHz

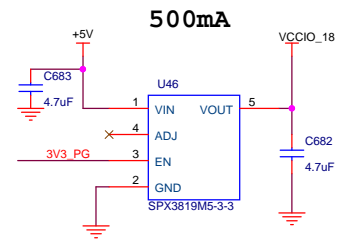
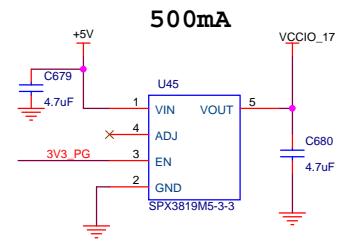
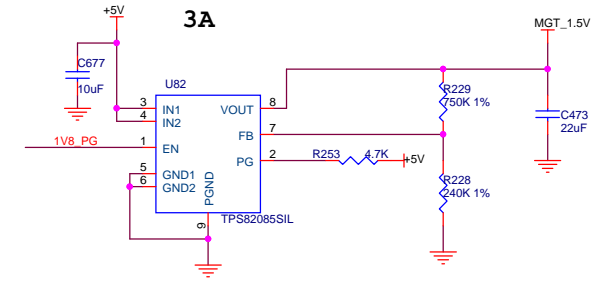
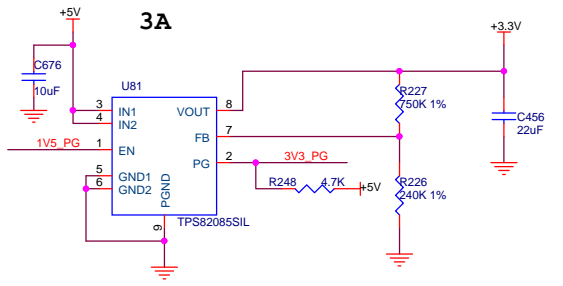
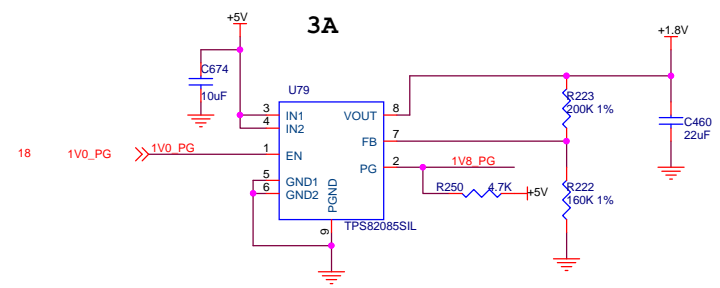
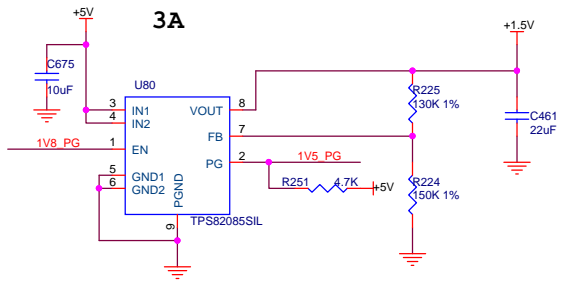




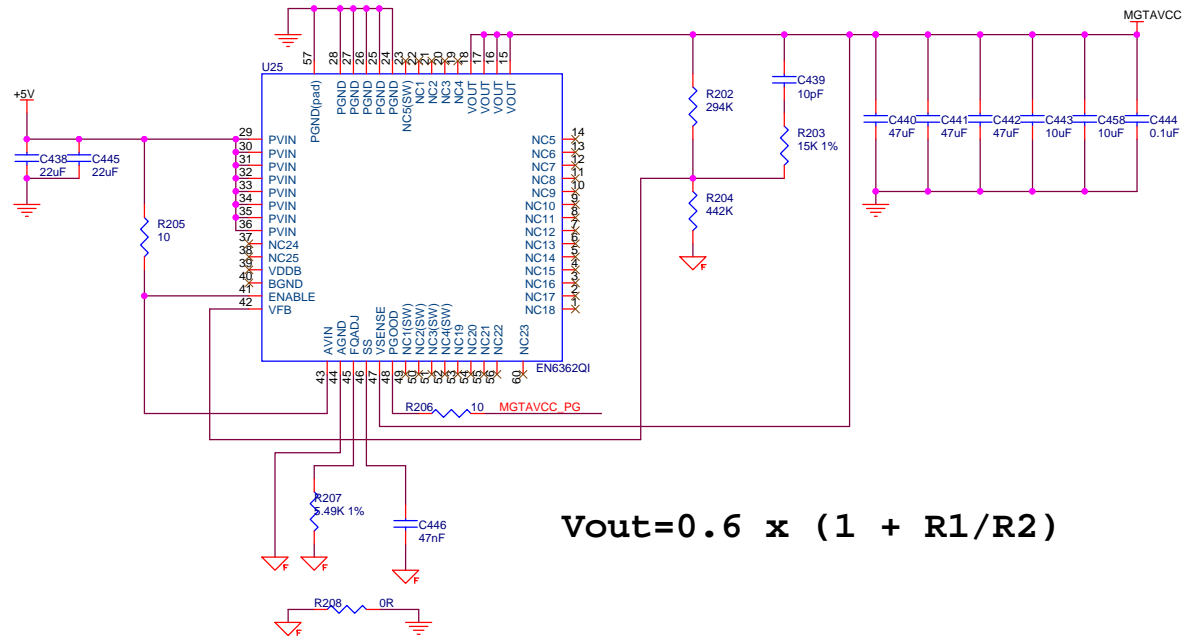
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Rev	1.0



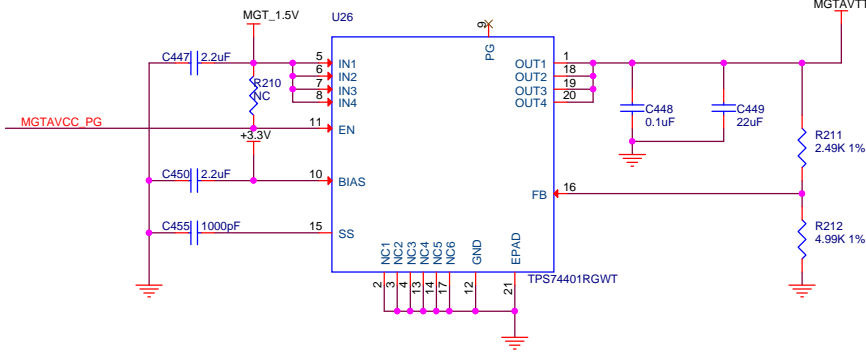


+1.0V 6A



$$V_{out} = 0.6 \times (1 + R1/R2)$$

+1.2V 3A



$$V_{out} = 0.8 \times (1 + R1/R2)$$

