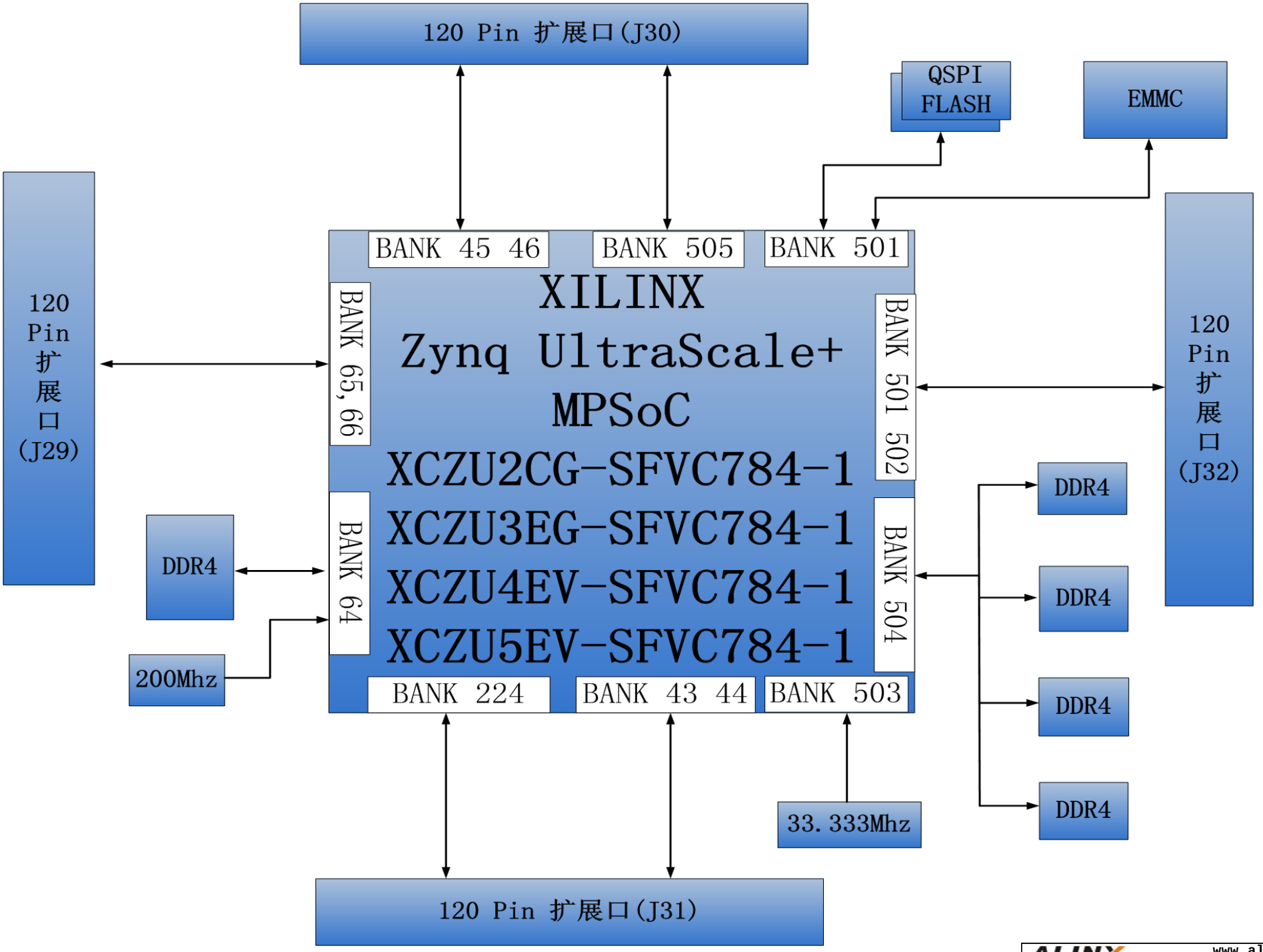

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Title	PAGE01 Block diagram
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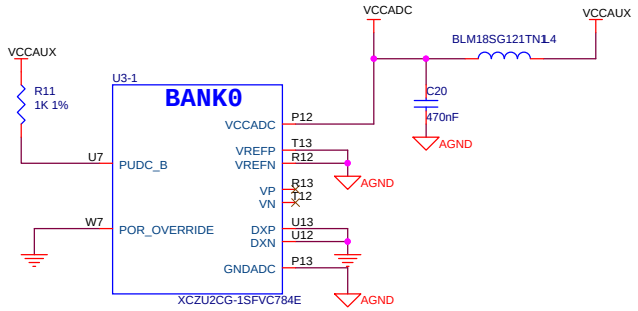
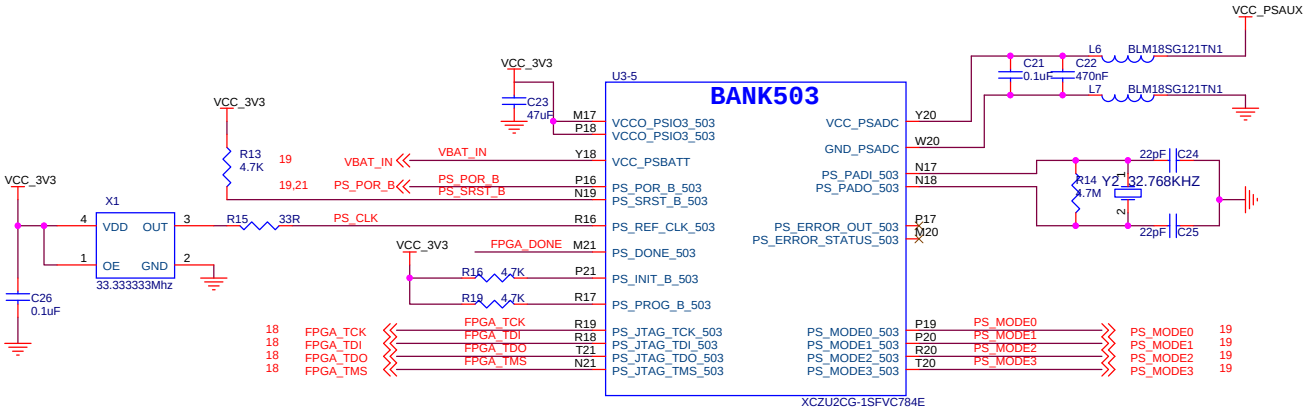
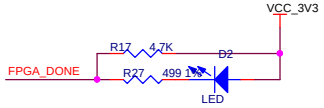
MODE[3:0]	BOOT MODE	Descritpion
0000	PS JTAG	PS JTAG Interface
0001	Quad_SPI(24b)	24-Bit addresssing(QSPI24)
0010	Quad_SPI(32b)	32-Bit addresssing(QSPI32)
0011	SD0(2.0)	SD2.0
0100	NAND	Requires 8-bit data bus width
0101	SD1(2.0)	SD2.0
0110	eMMC(1.8V)	eMMC version 4.5 at 1.8V
0111	USB0(2.0)	USB 2.0 only
1000	PJTAG(MIO #0)	PJTAG connection 0 option
1001	PJTAG(MIO #1)	PJTAG connection 1 option
1110	SD1 LS(3.0)	SD 3.0





FPGA DONE LED



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Title: Page02 Z7 Bank0 & BANK503

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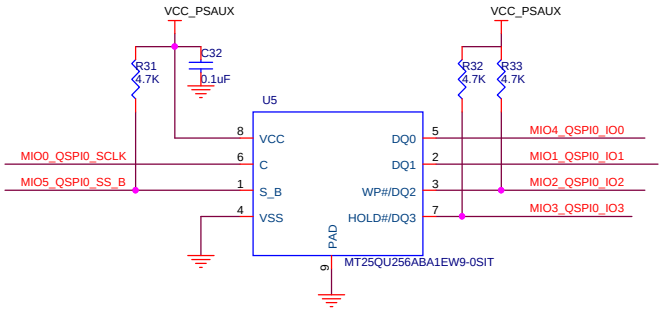

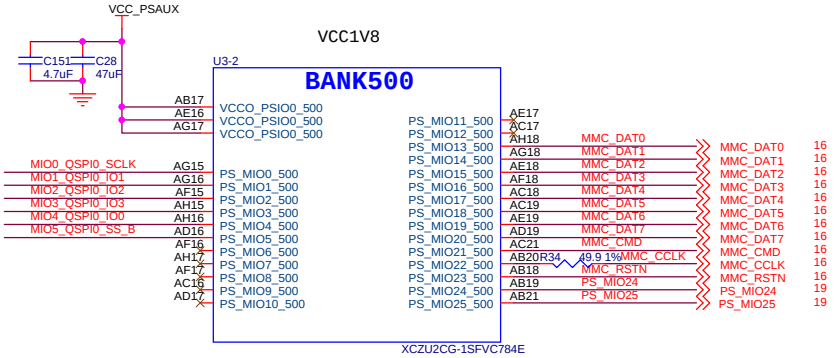

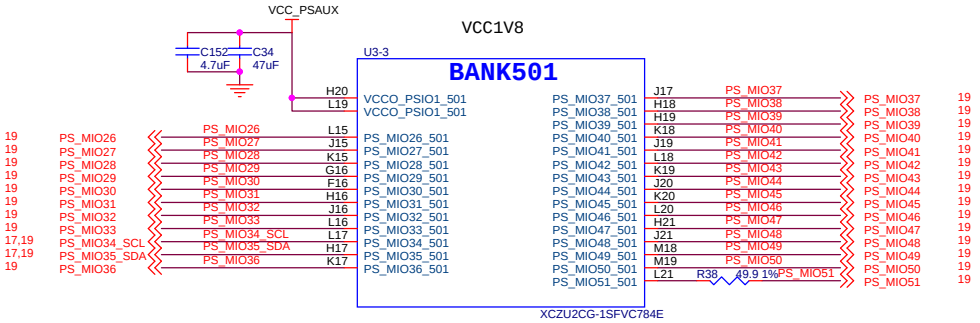

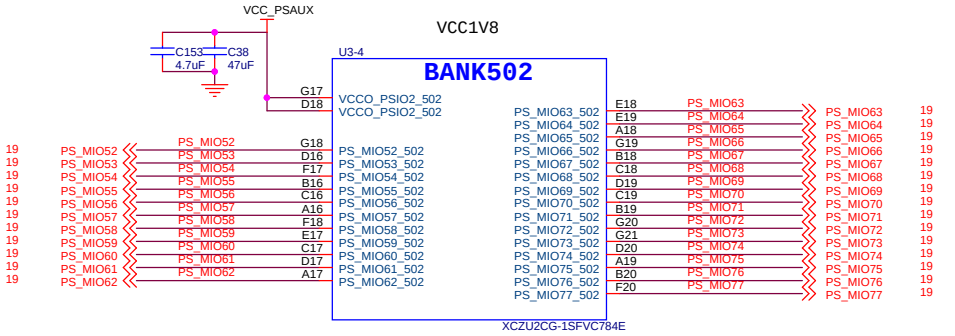

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Title	PAGE03 Z7 MIO-Config
Size	Document Number: ACU2CG-E核心板 Schematics
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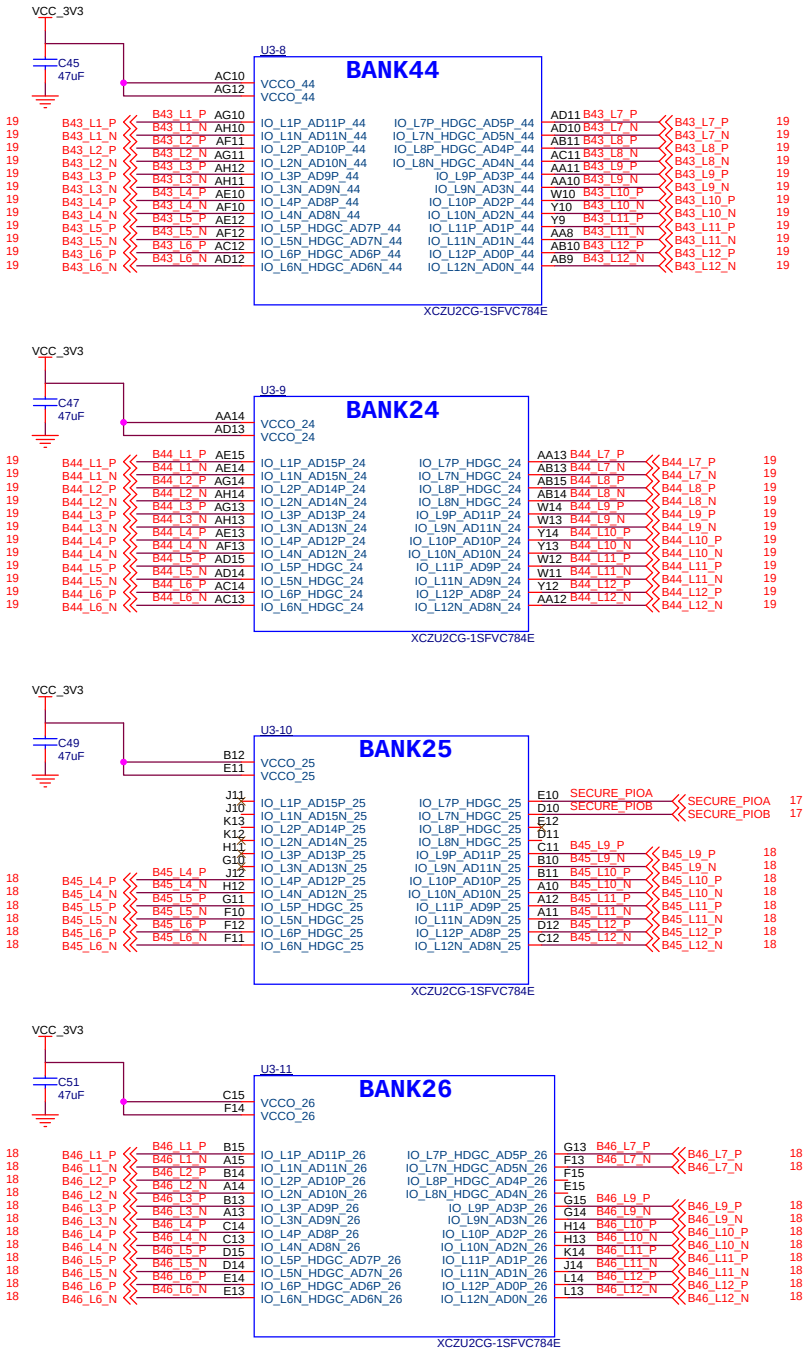

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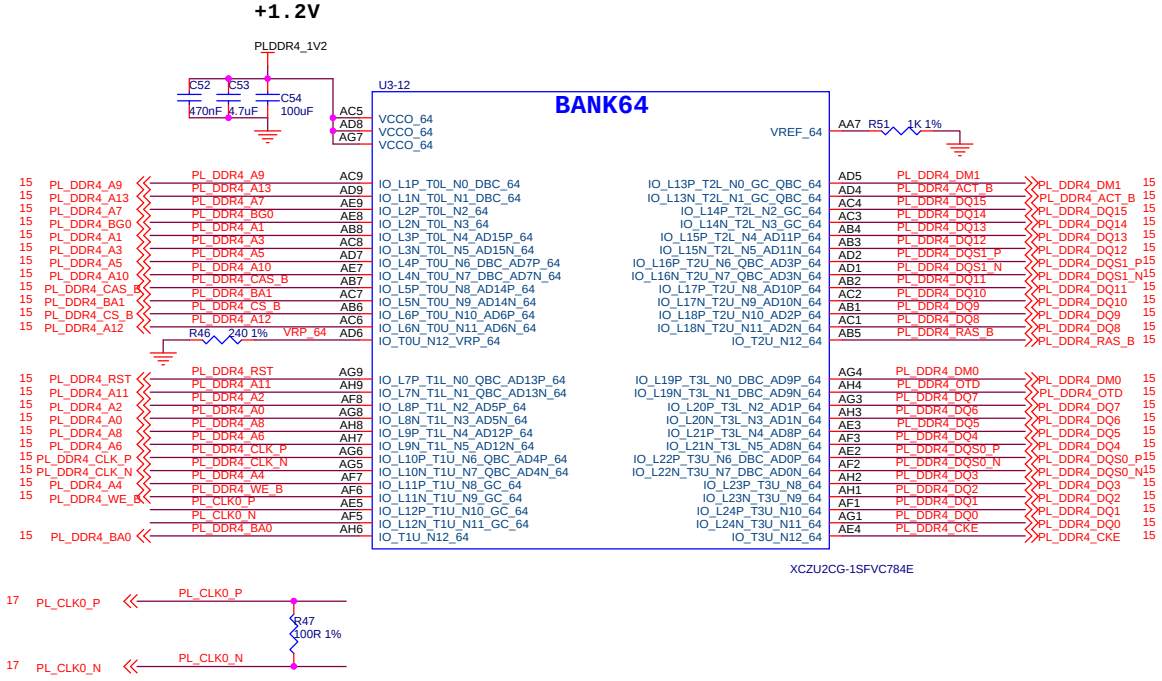
Title	PAGE04 Z7 Bank44_24_25_26
Size	Document Number: ACU2CG-E核心板 Schematics — Rev: 1.0
Date:	Monday, April 12, 2021 — Sheet 4 of 21



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Title	PAGE05 Z7 Bank64
Size	
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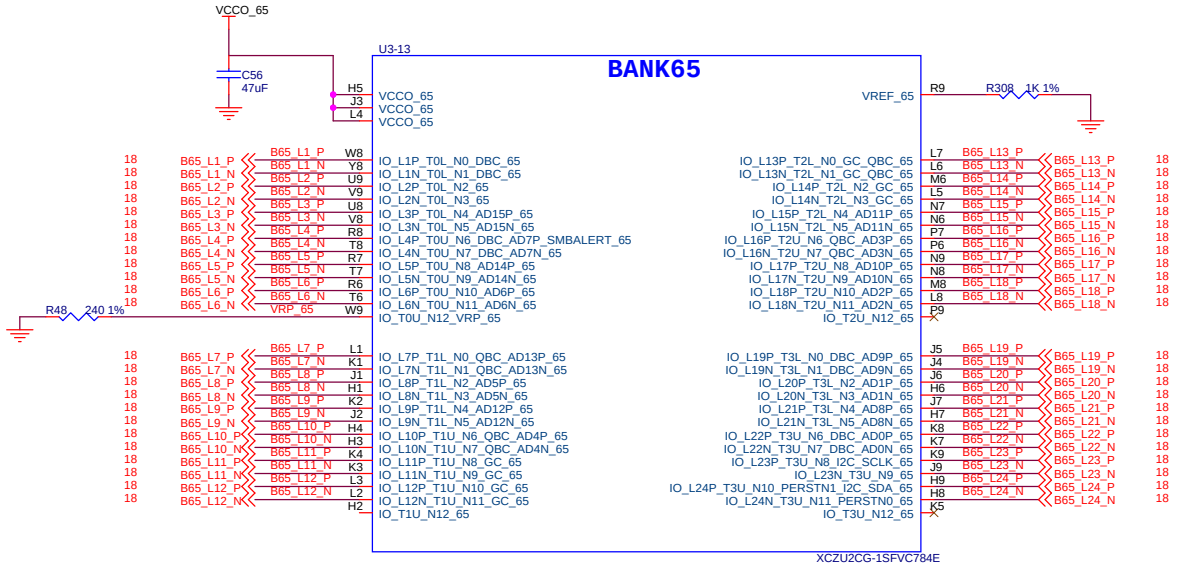

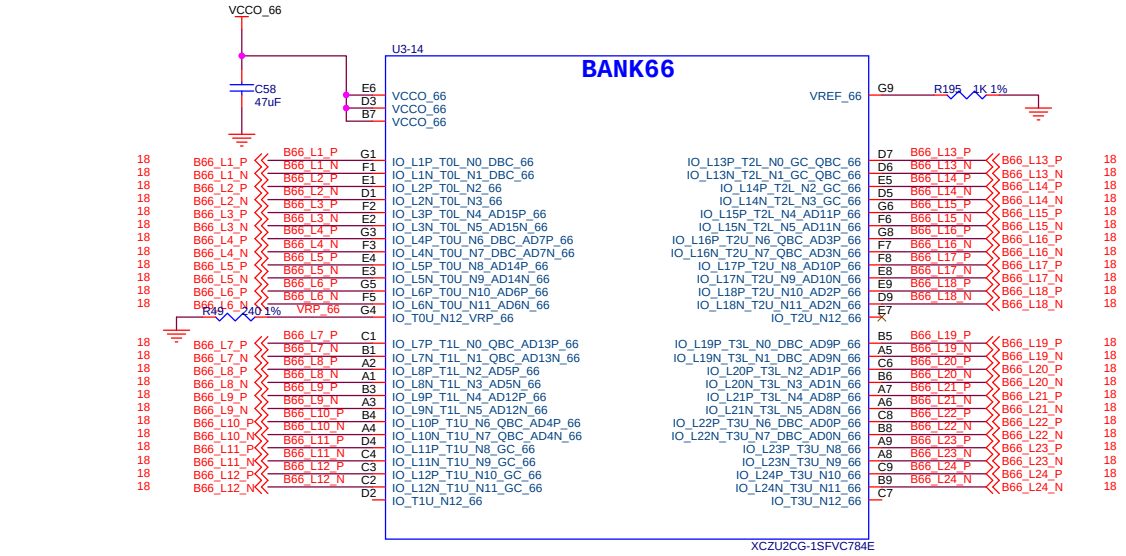

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Title	PAGE06 Z7 Bank65_66		
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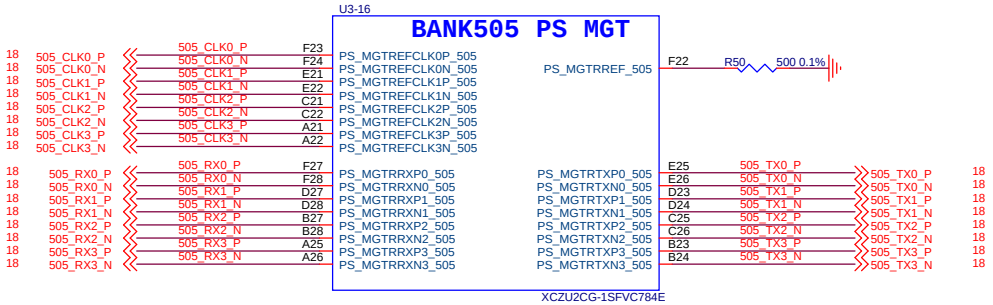

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Title: PAGE07 Z7 Bank505

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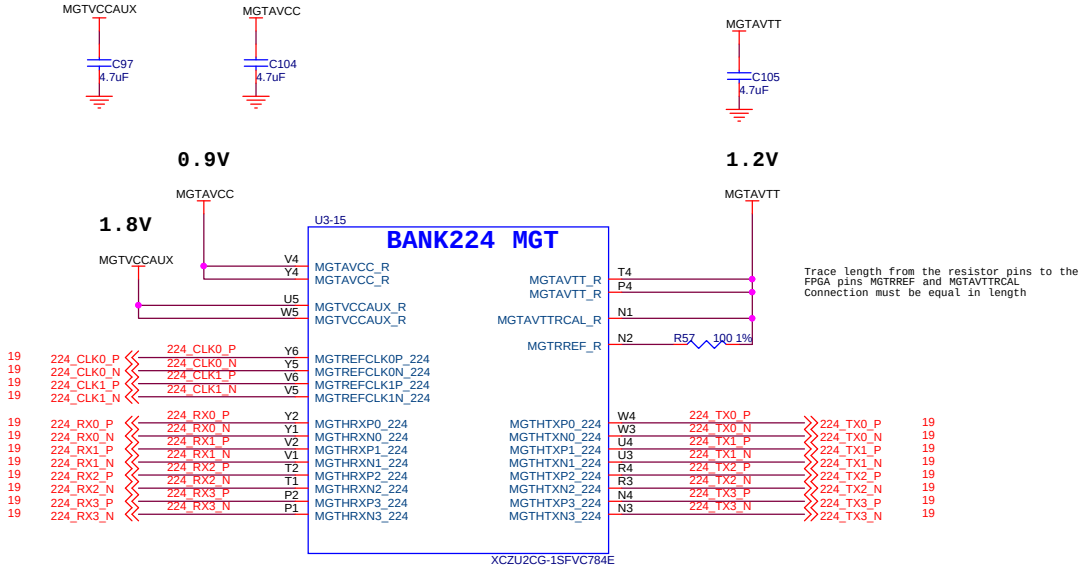

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Title: PAGE08 Z7 Bank224

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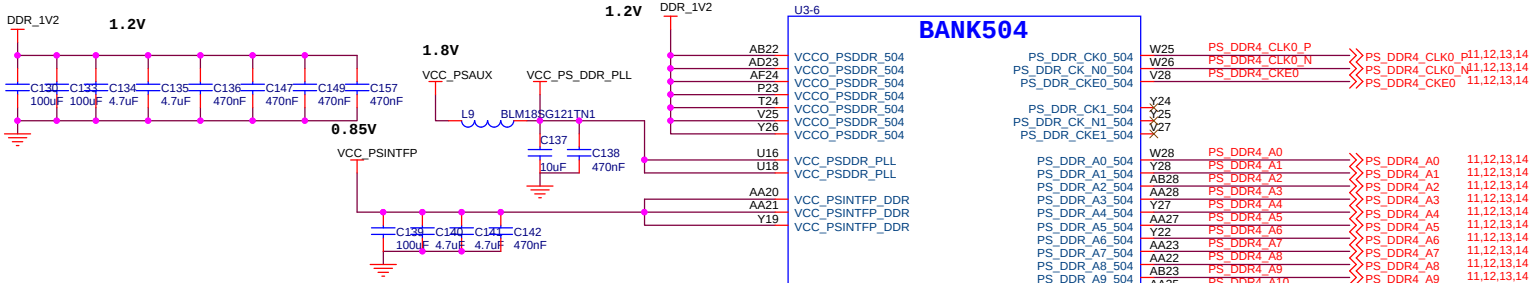

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Title: PAGE09 Z7 Bank504

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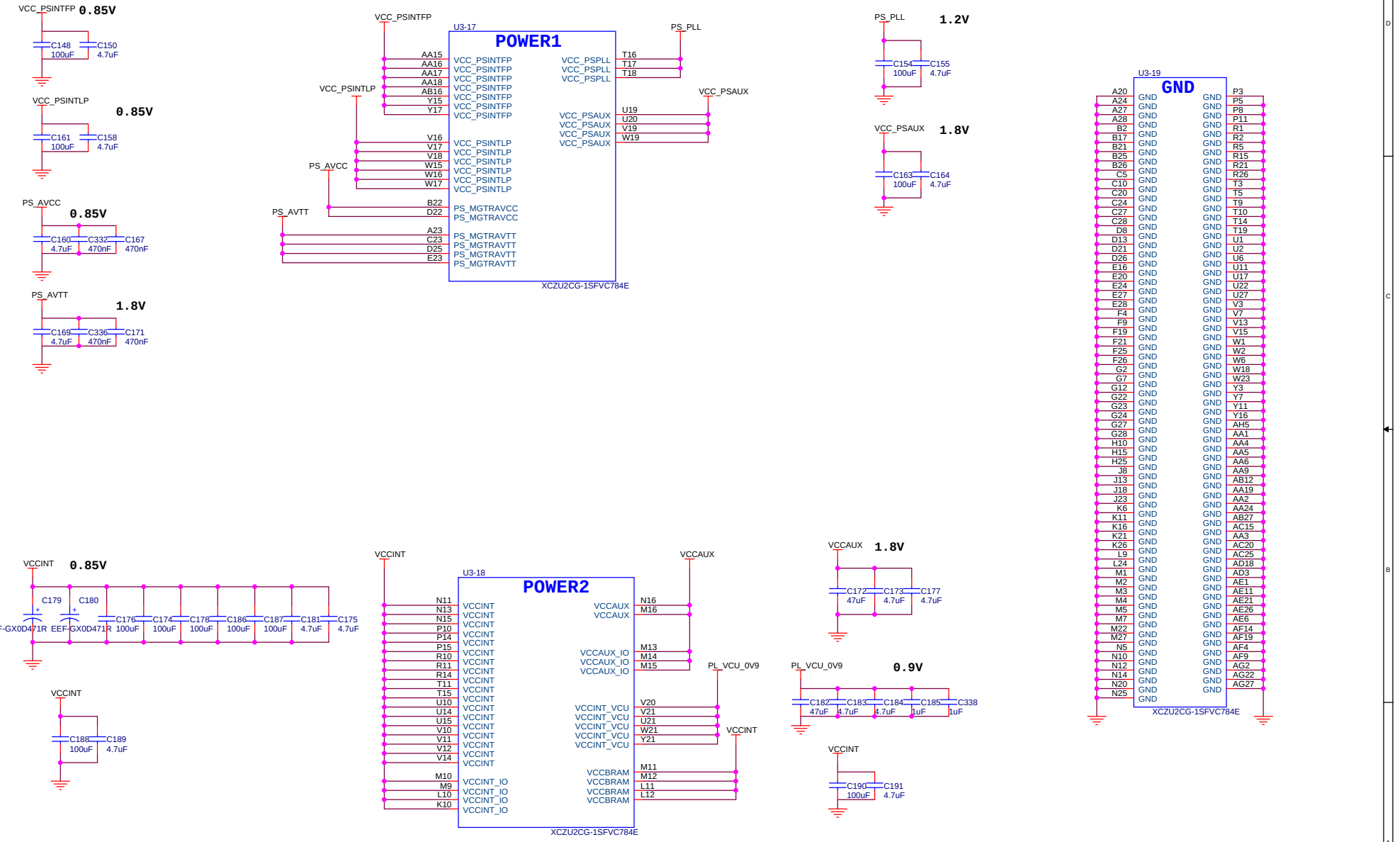

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Title: PAGE10 Z7 Power

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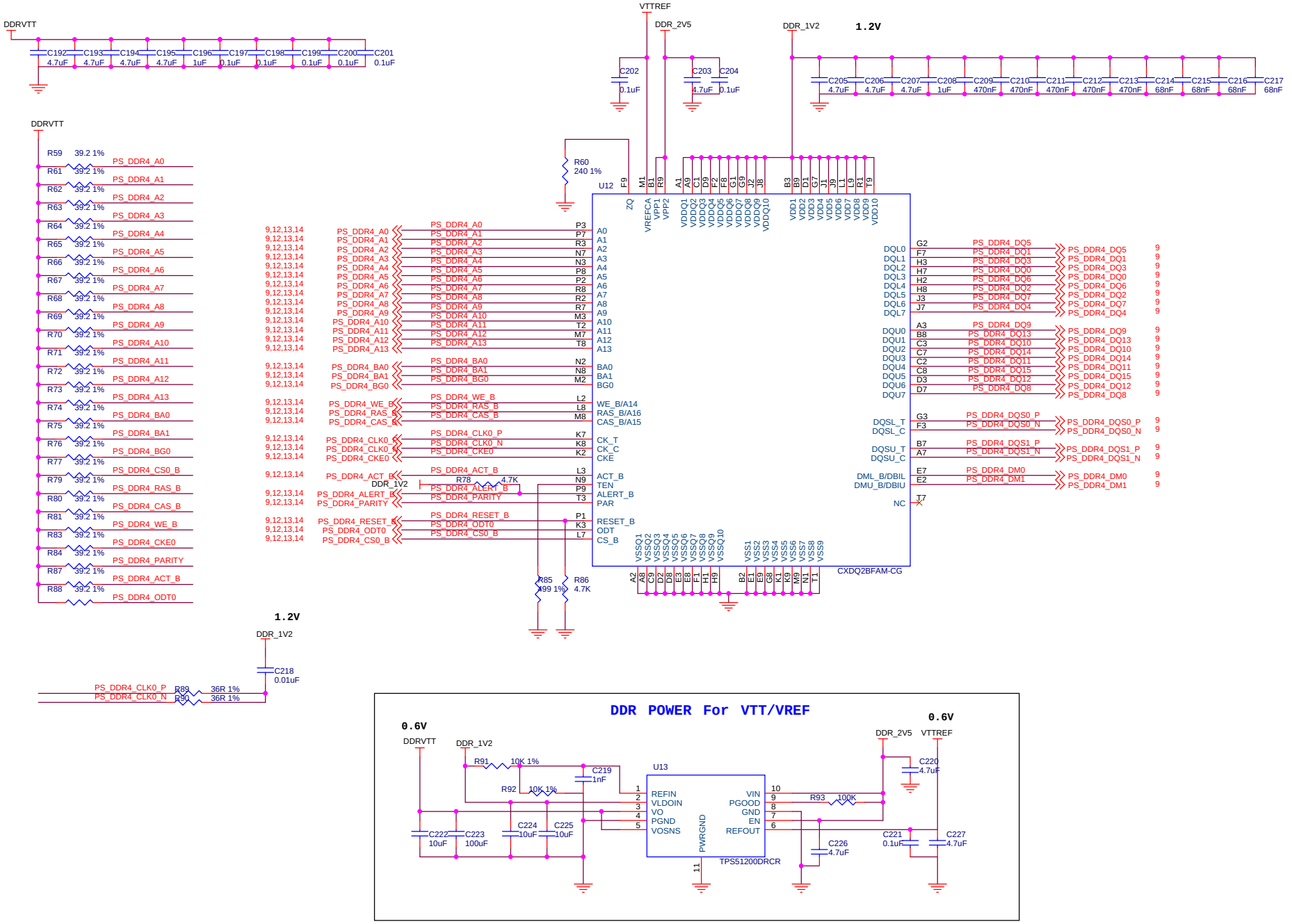

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Title	PAGE11 PS_DDR4_1
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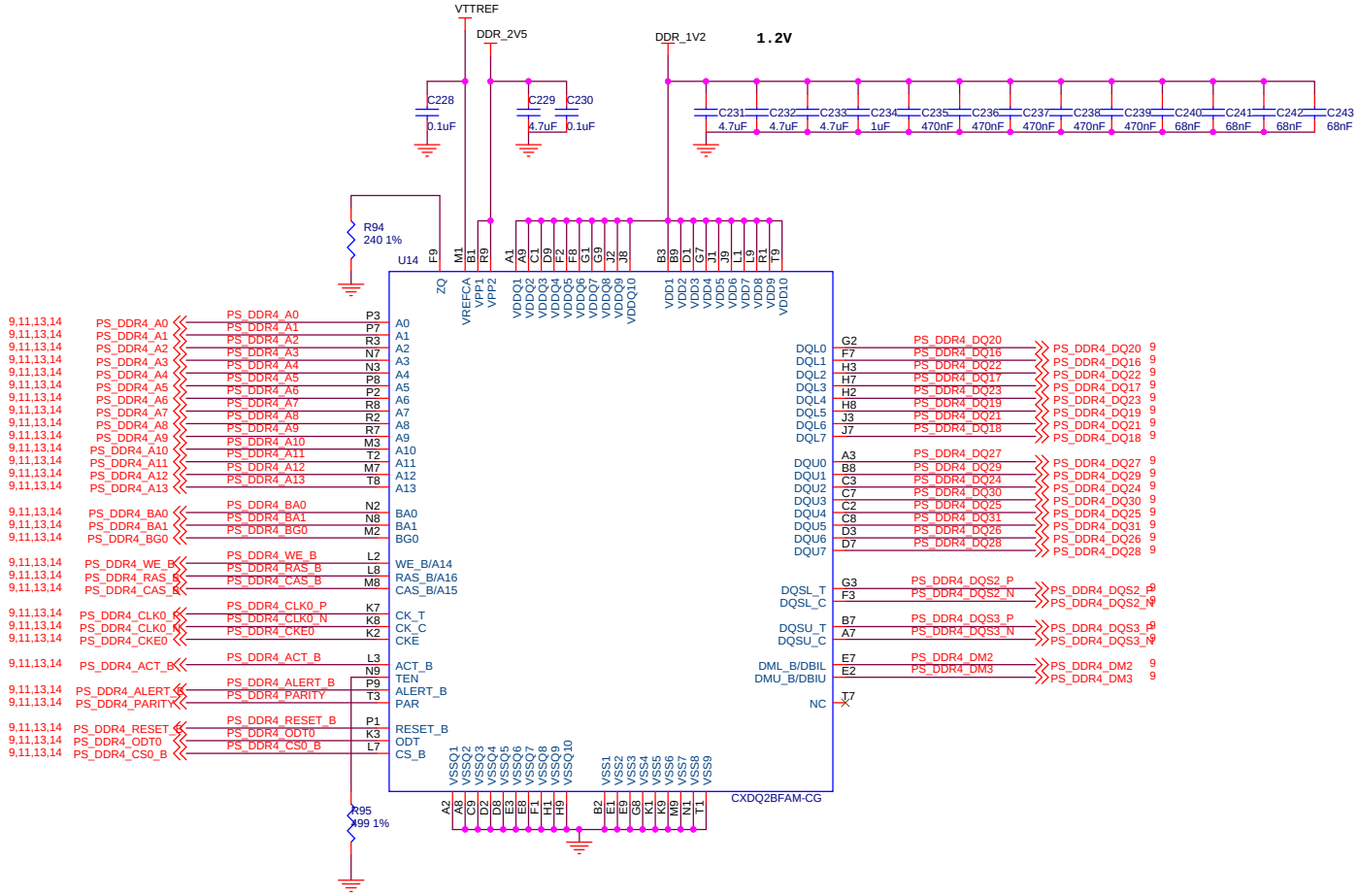

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Title	PAGE12 PS_DDR4_2
Size	Document Number: ACU2CG-E核心板 Schematics
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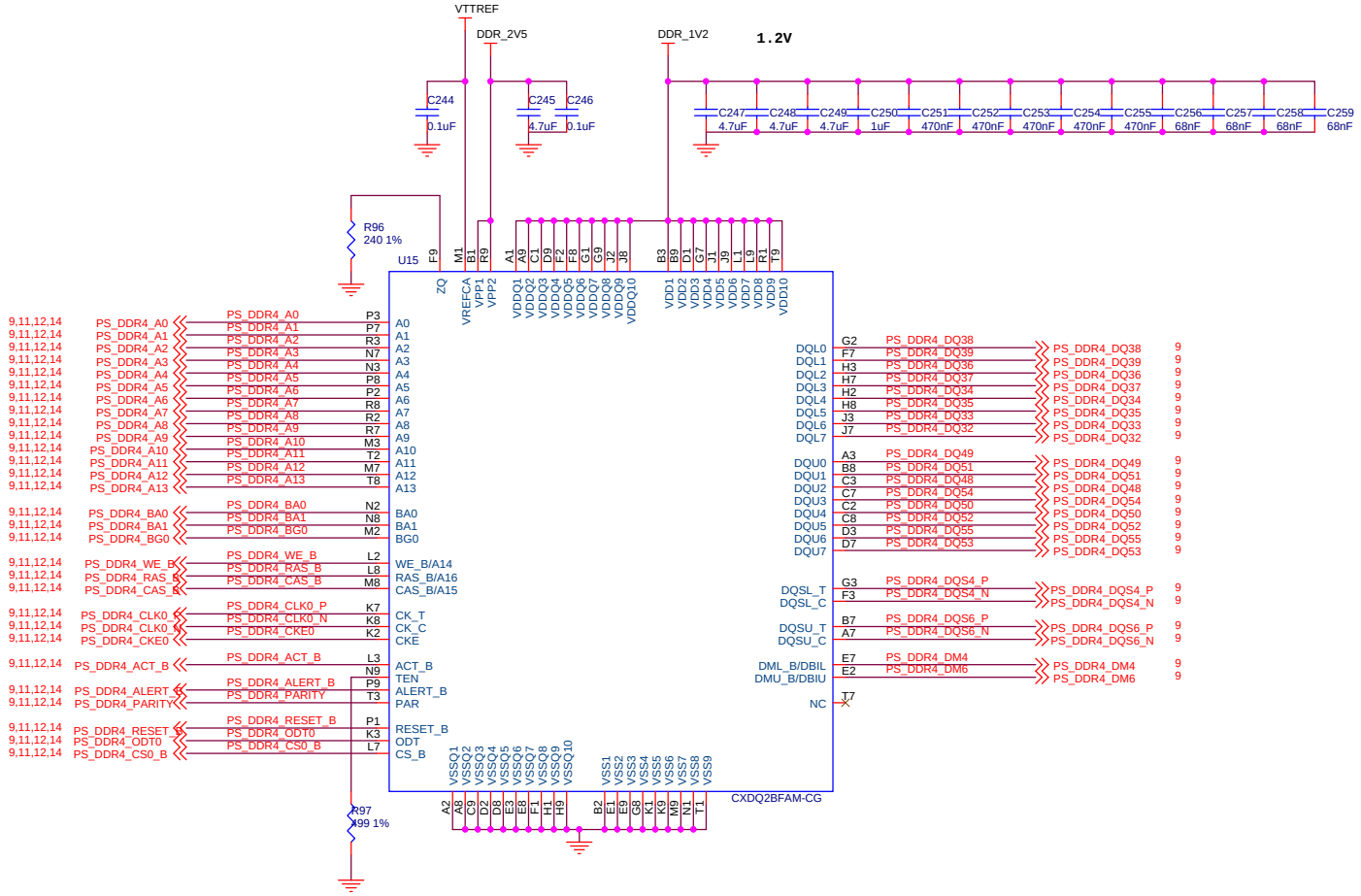

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ALINX	www.alinx.com
Title	PAGE13 PS_DDR4_3
Size	Document Number: ACU2CG-E核心板 Schematics
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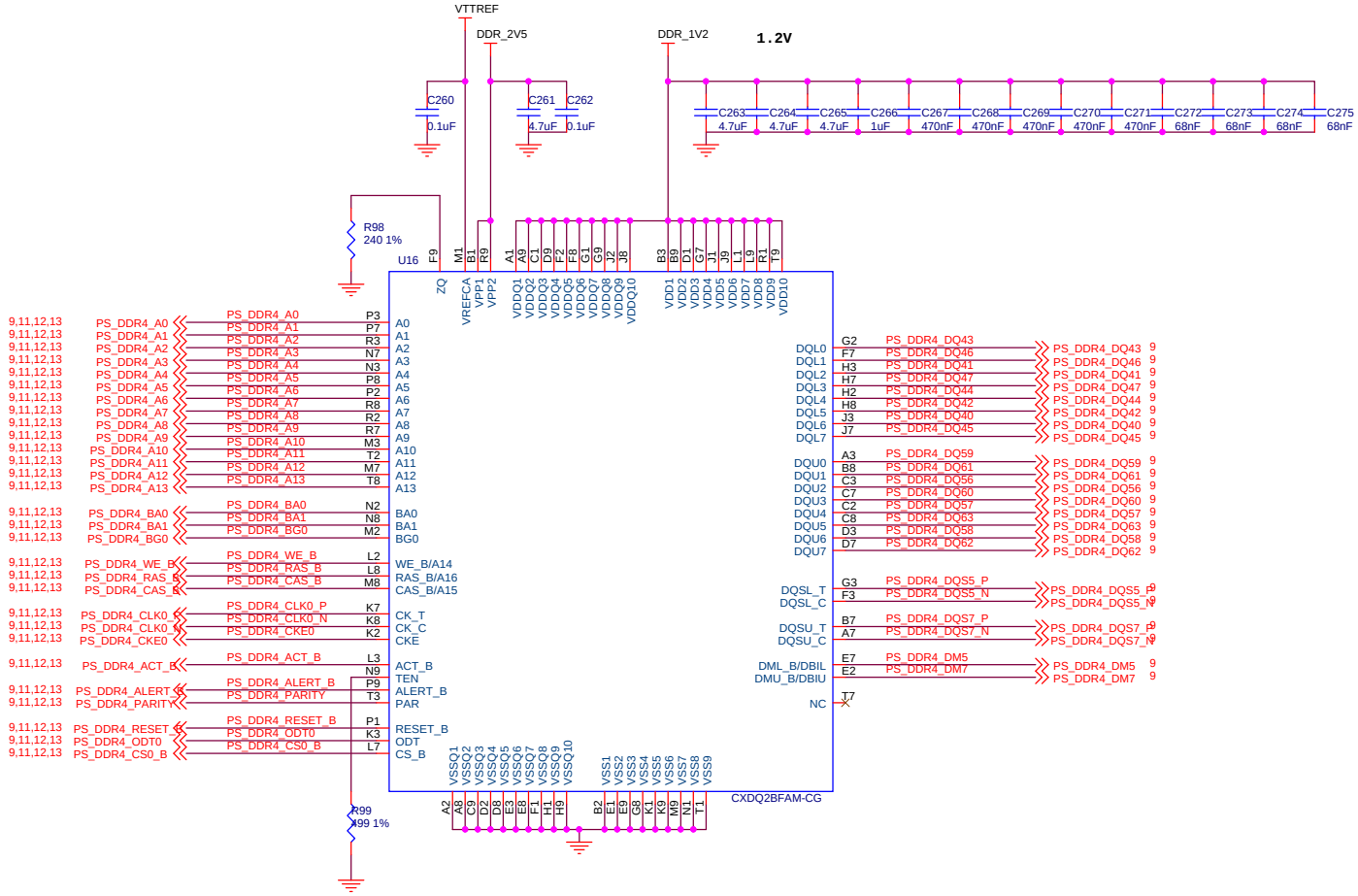

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Title	PAGE14 PS_DDR4_4	
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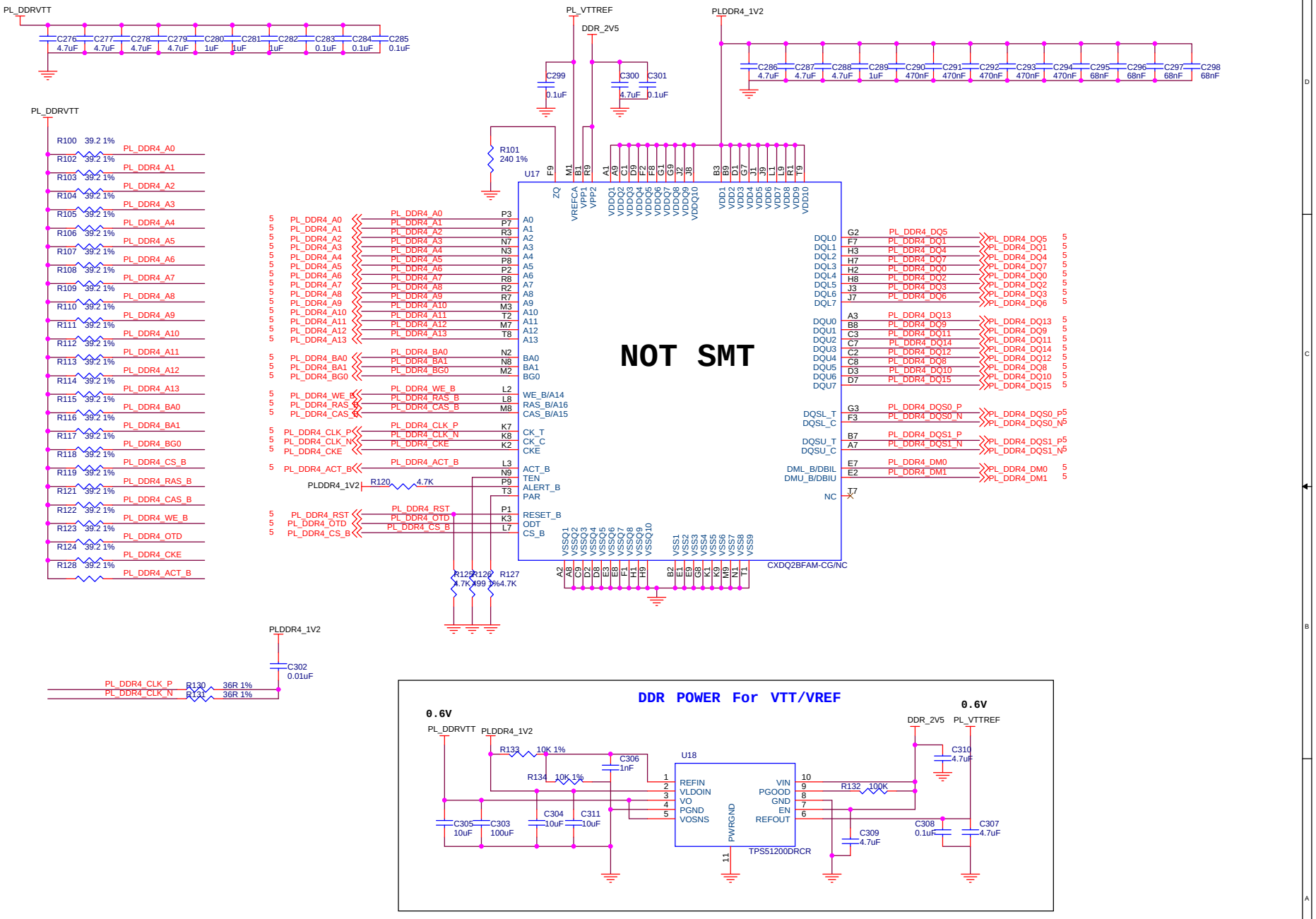

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ALINX	www.alinx.com
Title	PAGE15 PL_DDR4
Size	Document Number: ACU2CG-E核心板 Schematics
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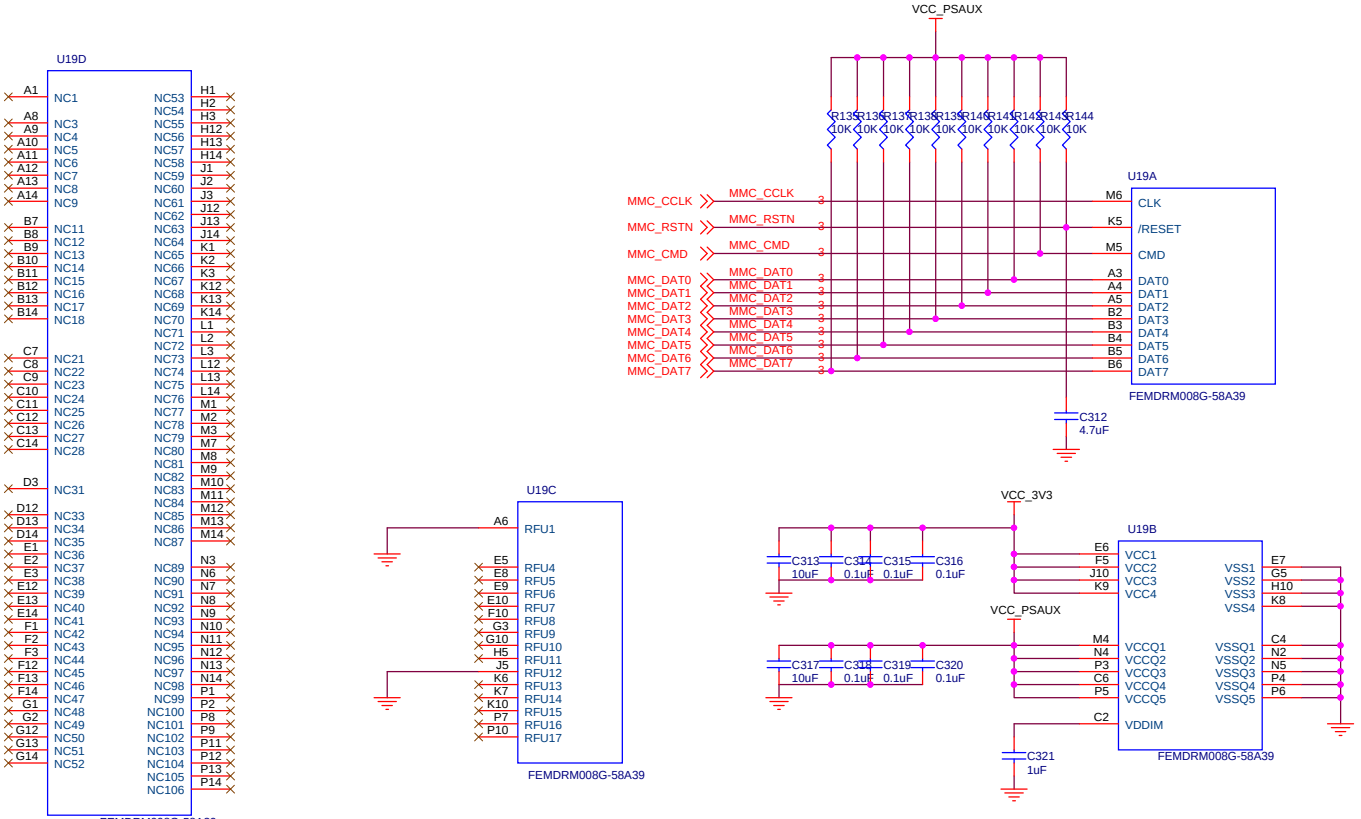

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Title: PAGE16 eMMC

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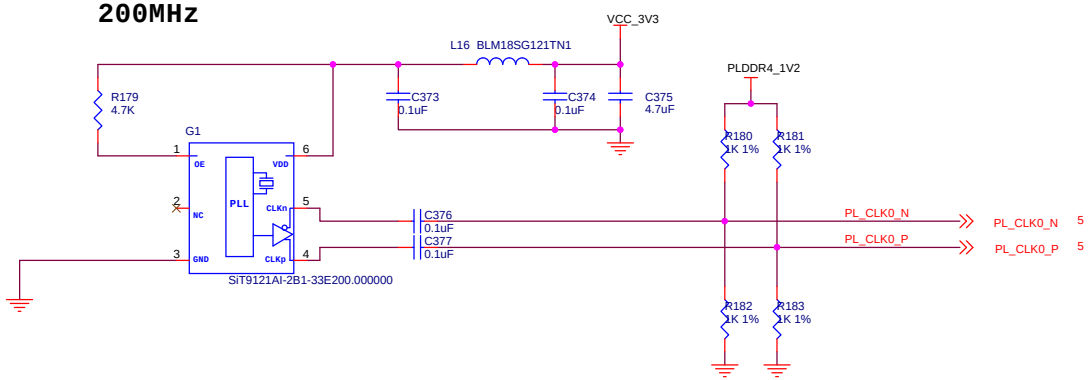
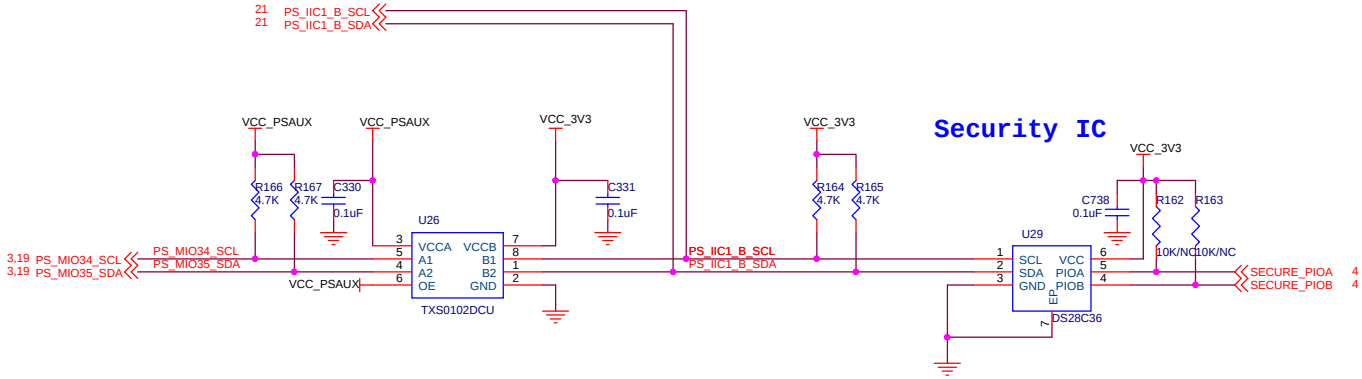
PL SYSTEM CLOCK

200MHz





PS_IIC1: IIC ADDRESS IS 0x1B

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Title: PAGE17 CLOCK & SECURITY		
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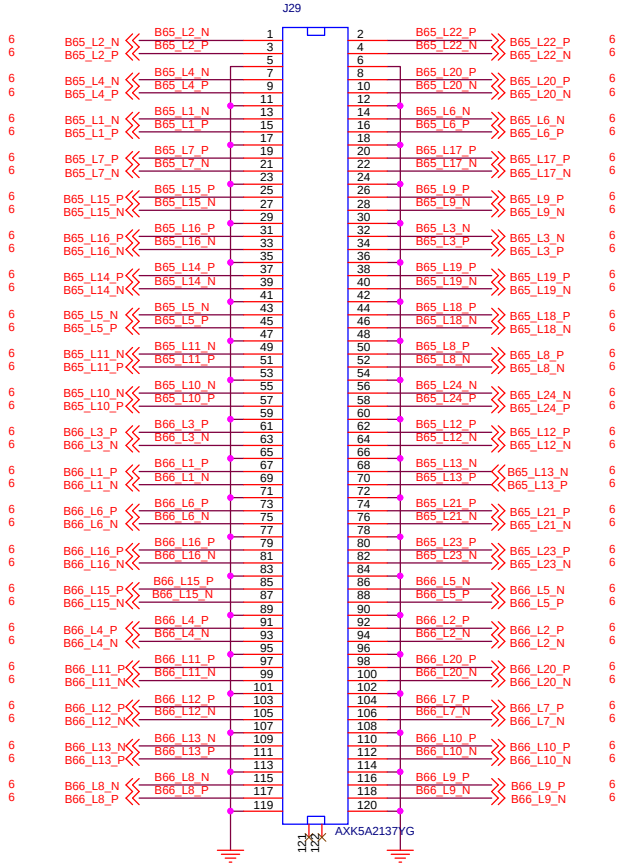
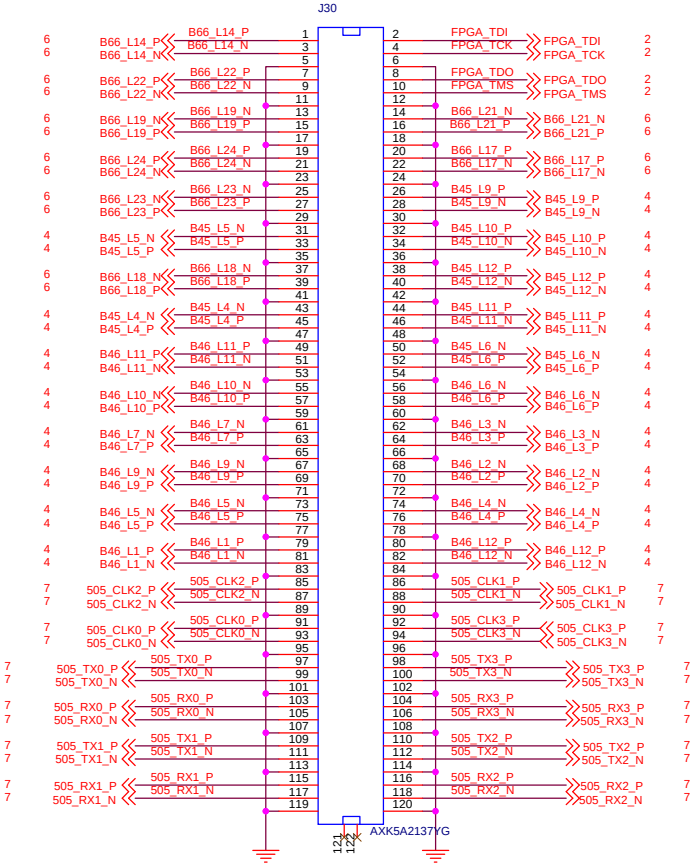
BANK65, BANK66 IO Voltage can not exceed +1.8V



BANK45, BANK46 IO Voltage is +3.3V Standard



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Title: PAGE18 Connector_1

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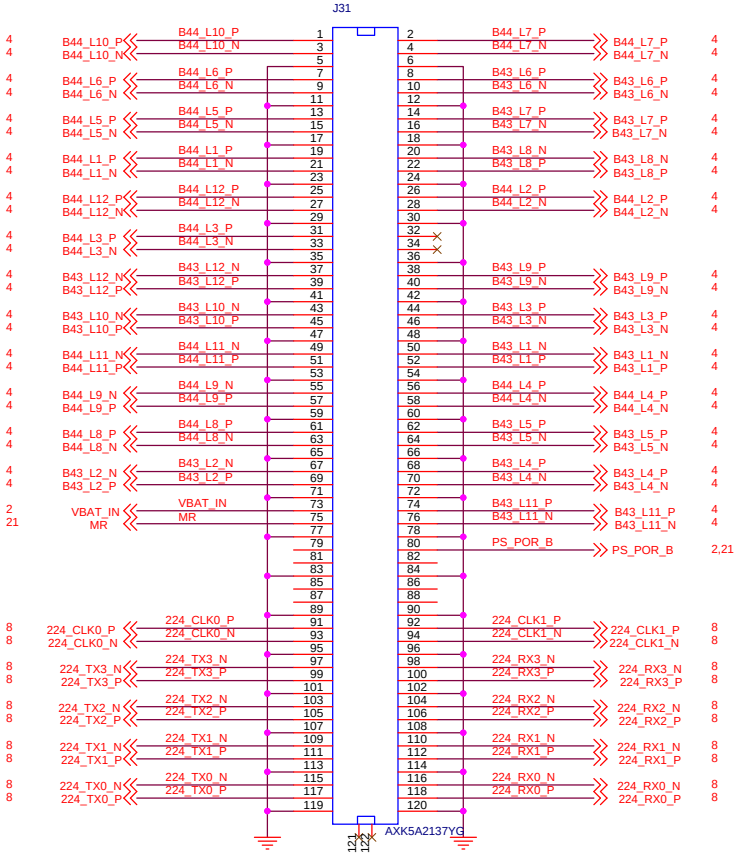
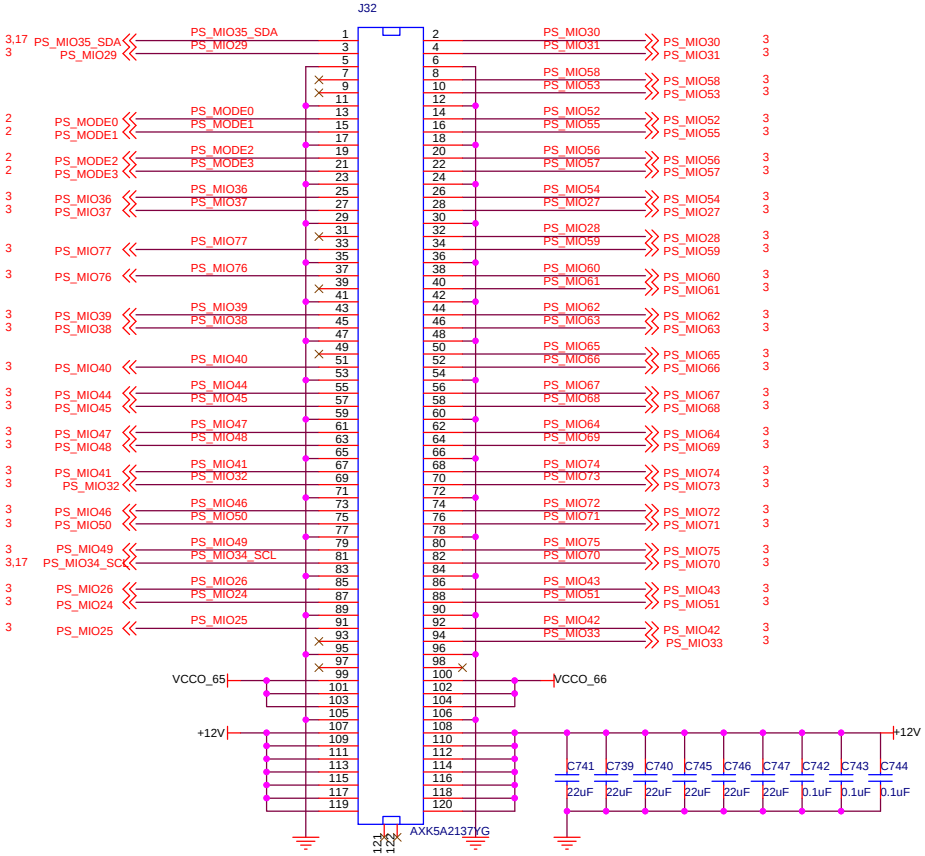
BANK43, BANK44 IO Voltage is +3.3V Standard



The MIO Voltage is +1.8V Standard



VCCO_65 VCCO_66 Power supply can not exceed 1.8V

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Title: PAGE19 Connector_2

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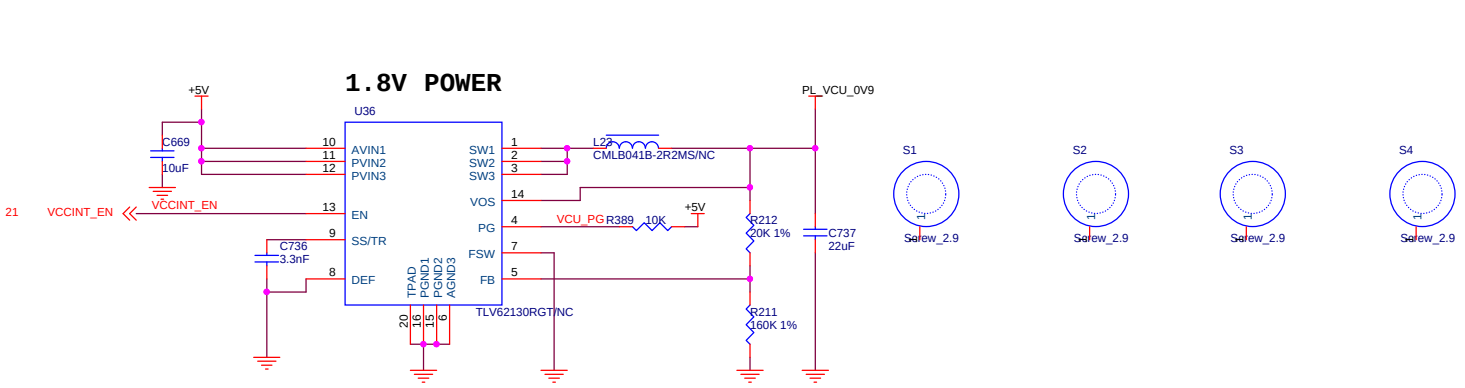
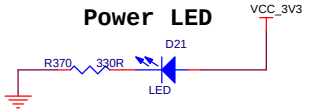
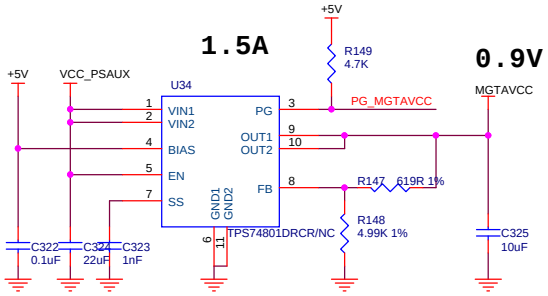
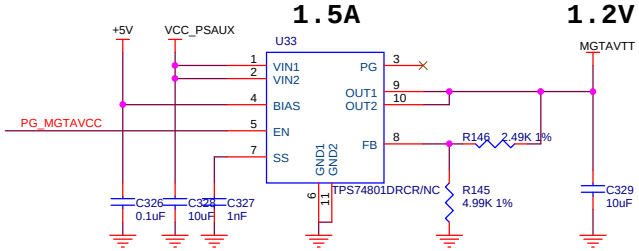
POWER ON: VCCINT/VCCINT_IO/VCCBRAM(+0.85V)->VCCINT_VCU(+0.9V)->VCCAUX/VCCAUX_IO(+1.8V)->VCCO(+3.3V, +1.8V)

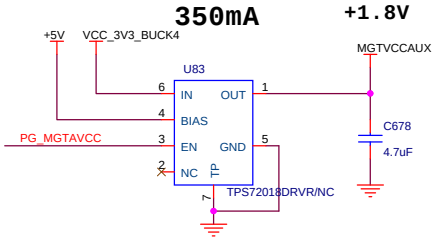
POWER ON: VCCINT(+0.85V)->MGTAVCC(+09V)->MGTAVTT(+1.2V)











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Title: PAGE20 PL POWER

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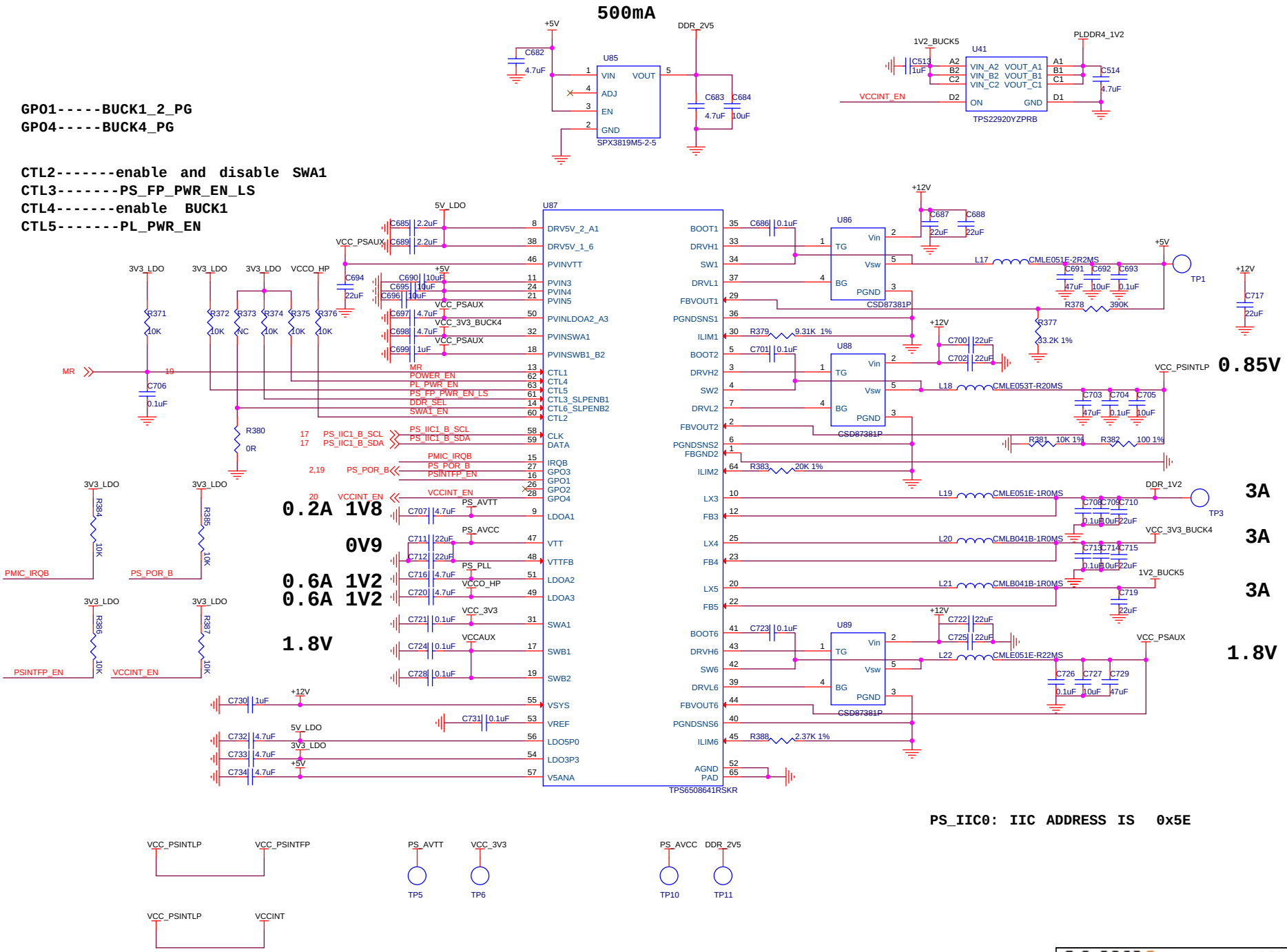
500mA
+5V
C682
4.7uF
U85
VIN
VOUT
ADJ
EN
GND
SPX3819M5-2-5
DDR_2V5
C683
C684
4.7uF
10uF
1V2_BUCK5
C513
1uF
U41
VIN_A2
VOUT_A1
VIN_B2
VOUT_B1
VIN_C2
VOUT_C1
ON
GND
TPS22920YZPRB
PLDDR4_1V2
C514
4.7uF
VCCINT_EN
GPO1-----BUCK1_2_PG
GPO4-----BUCK4_PG
CTL2-------enable and disable SWA1
CTL3-------PS_FP_PWR_EN_LS
CTL4-------enable BUCK1
CTL5-------PL_PWR_EN
U87
5V_LDO
VCC_PSAUX
3V3_LDO
VCCO_HP
+5V
+12V
MR
POWER_EN
PL_PWR_EN
PS_FP_PWR_EN_LS
DDR_SEL
SWA1_EN
PS_IIC1_B_SCL
PS_IIC1_B_SDA
PMIC_IRQB
PS_POR_B
PSINTFP_EN
VCCINT_EN
VCC_3V3_BUCK4
DRV5V_2_A1
DRV5V_1_6
PVINVTT
PVIN3
PVIN4
PVIN5
PVINLDOA2_A3
PVINSWA1
PVINSWB1_B2
CTL1
CTL4
CTL5
CTL3_SLPENB1
CTL6_SLPENB2
CTL2
CLK
DATA
IRQB
GPO3
GPO1
GPO2
GPO4
LDOA1
VTT
VTTFB
LDOA2
LDOA3
SWA1
SWB1
SWB2
VSYS
VREF
LDO5P0
LDO3P3
V5ANA
BOOT1
DRVH1
SW1
DRVL1
FBVOUT1
PGNDSNS1
ILIM1
BOOT2
DRVH2
SW2
DRVL2
FBVOUT2
PGNDSNS2
FBGND2
ILIM2
LX3
FB3
LX4
FB4
LX5
FB5
BOOT6
DRVH6
SW6
DRVL6
FBVOUT6
PGNDSNS6
ILIM6
AGND
PAD
TPS6508641RSKR
U86
U88
U89
TG
BG
Vin
Vsw
PGND
CSD87381P
L17
CMLE051E-2R2MS
L18
CMLE053T-R20MS
L19
CMLE051E-1R0MS
L20
CMLB041B-1R0MS
L21
CMLB041B-1R0MS
L22
CMLE051E-R22MS
TP1
TP3
0.85V
3A
3A
3A
1.8V
0.2A 1V8
0V9
0.6A 1V2
0.6A 1V2
1.8V
PS_AVTT
PS_AVCC
PS_PLL
VCCAUX
VCCO_HP
VCC_3V3
VCC_PSINTLP
VCC_PSINTFP
VCCINT
DDR_1V2
1V2_BUCK5
PS_IIC0: IIC ADDRESS IS 0x5E
TP5
TP6
TP10
TP11
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