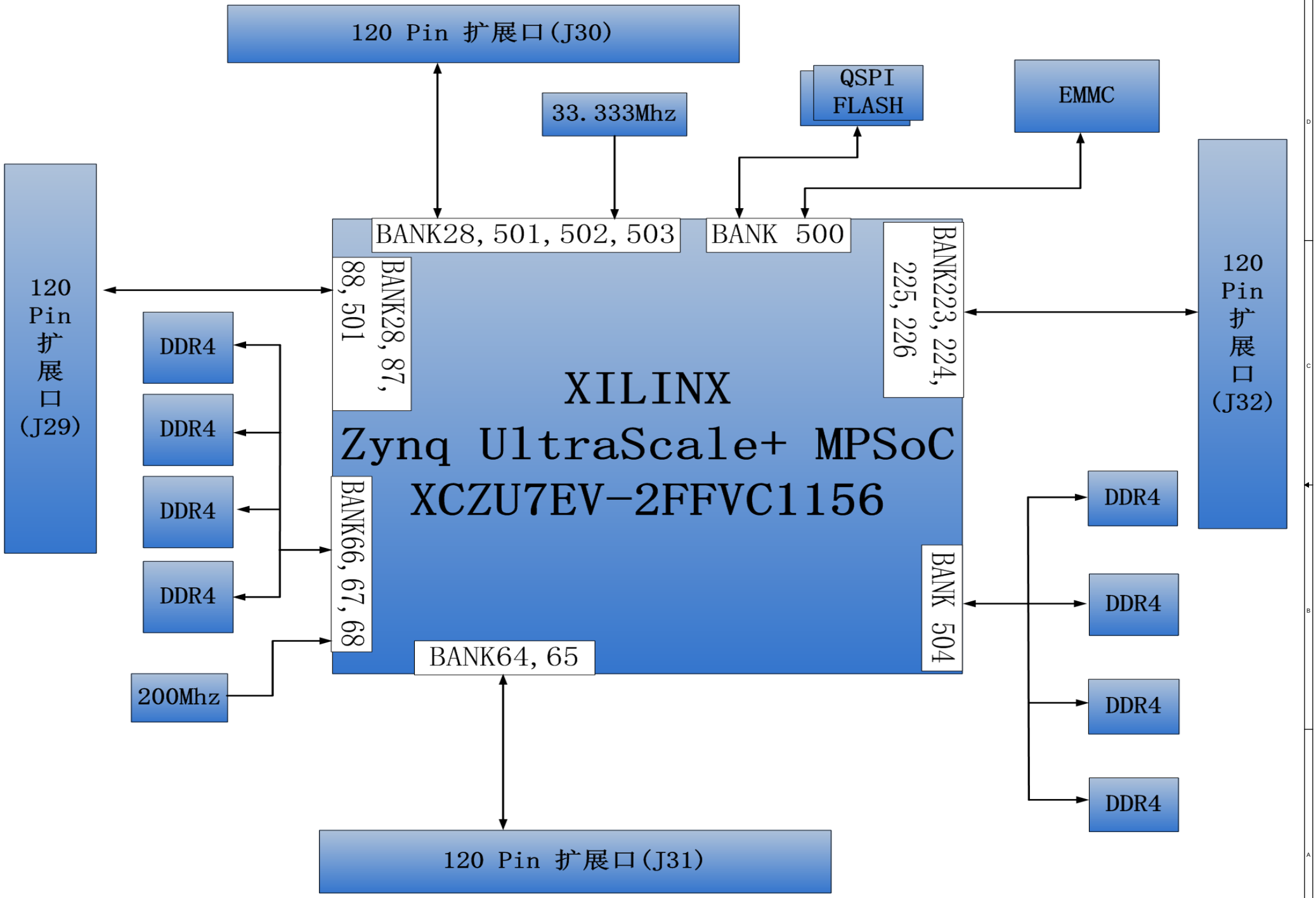

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Title: PAGE01 Block diagram

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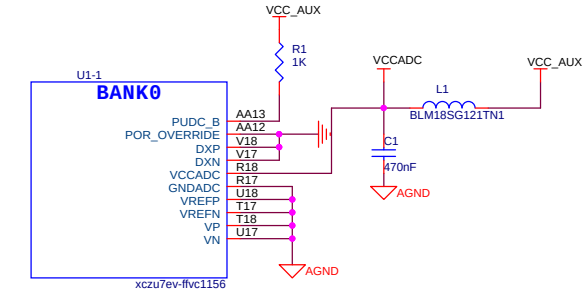
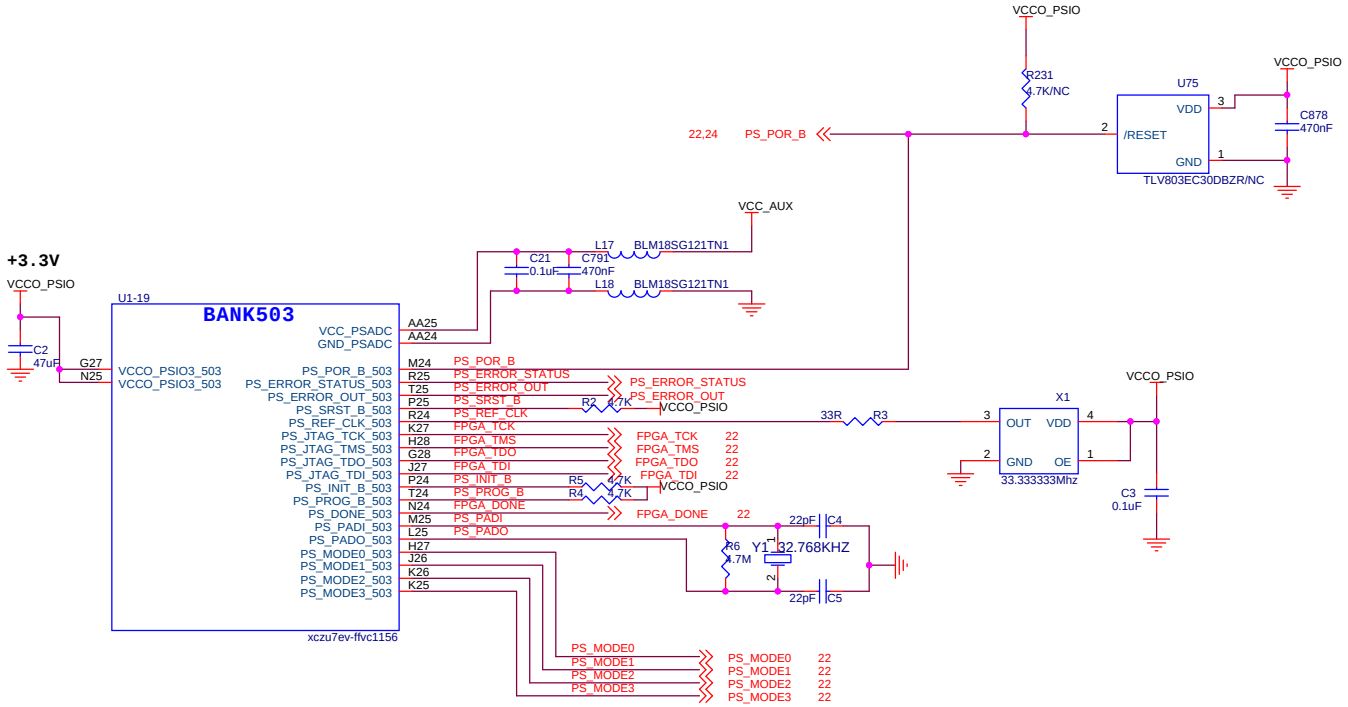
MODE[3:0]	BOOT MODE	Descritpion
0000	PS JTAG	PS JTAG Interface
0001	Quad_SPI(24b)	24-Bit addresssing(QSPI24)
0010	Quad_SPI(32b)	32-Bit addresssing(QSPI32)
0011	SD0(2.0)	SD2.0
0101	SD1(2.0)	SD2.0
0110	eMMC(1.8V)	eMMC version 4.5 at 1.8V
0111	USB0(2.0)	USB 2.0 only
1110	SD1 LS(3.0)	SD 3.0





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Title: Page02 Z7 Bank0 & BANK503

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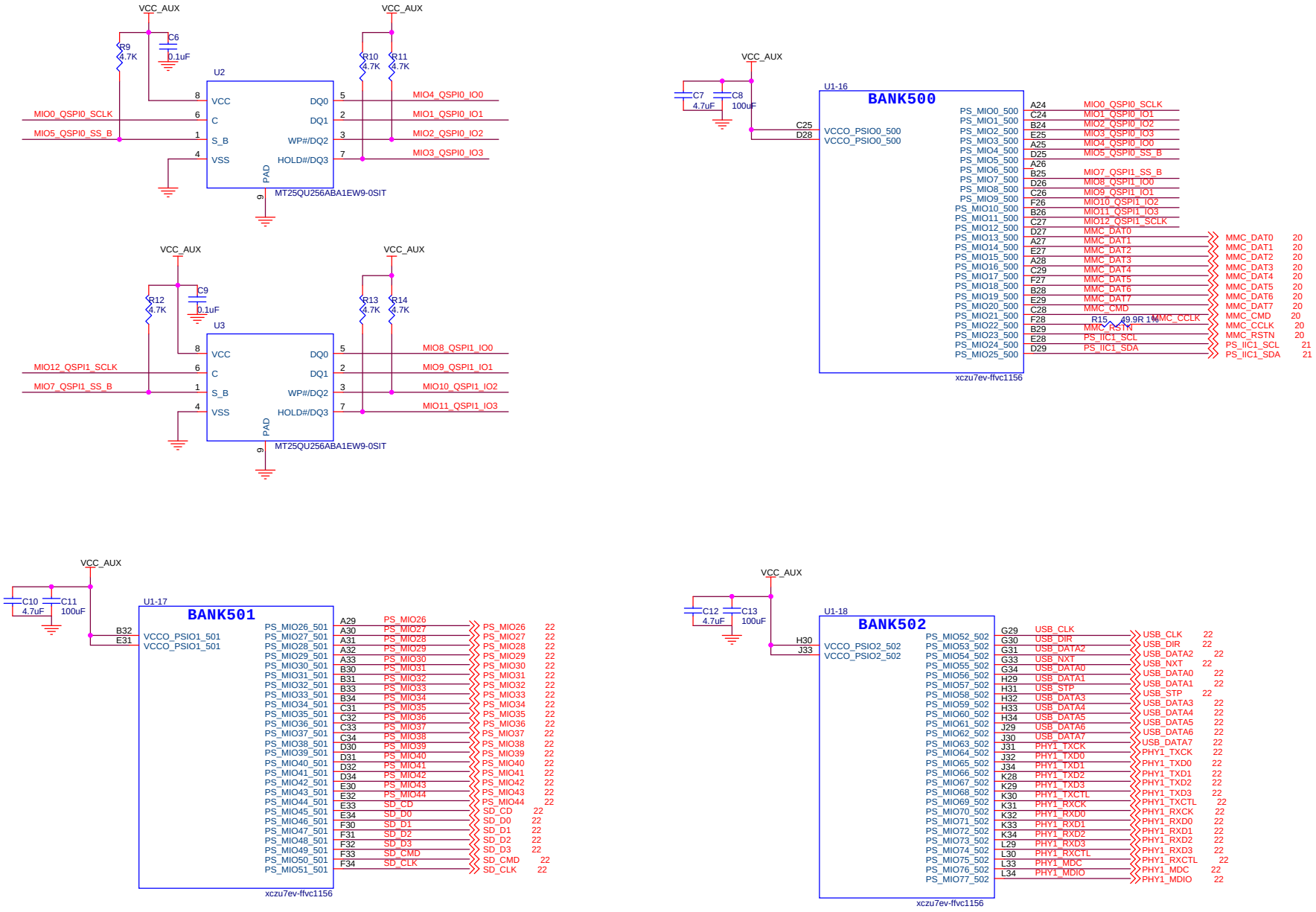

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Title	PAGE03 Z7 MIO-Config
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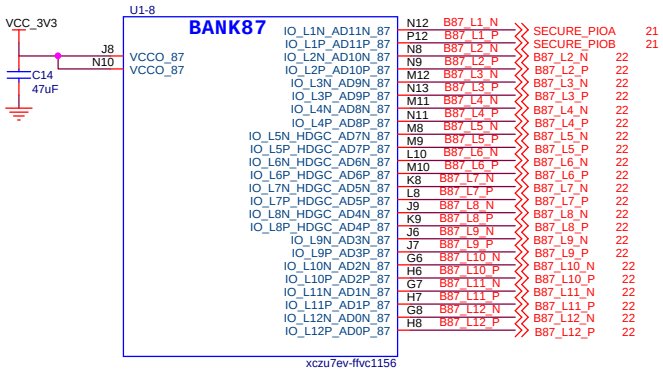
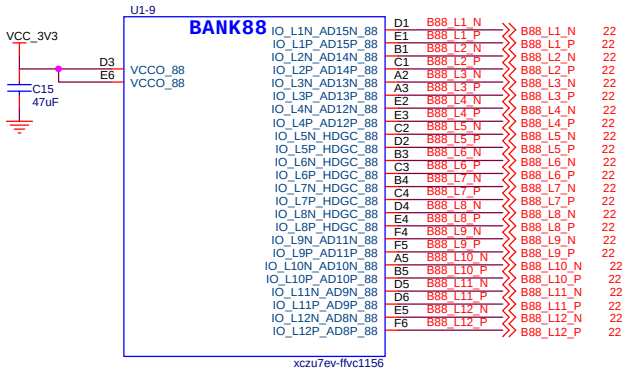
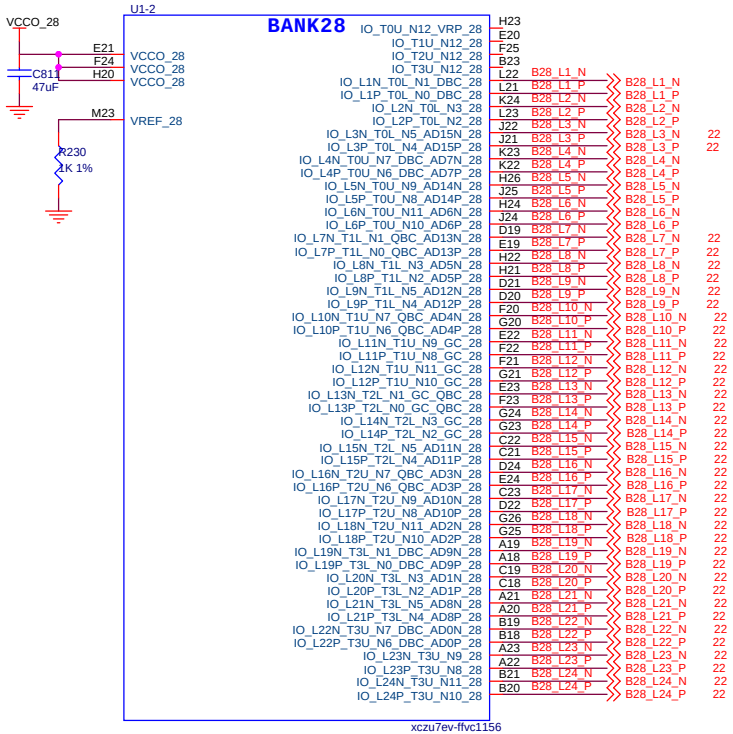




+1.8V



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Title: PAGE04 Z7 Bank28_87_88

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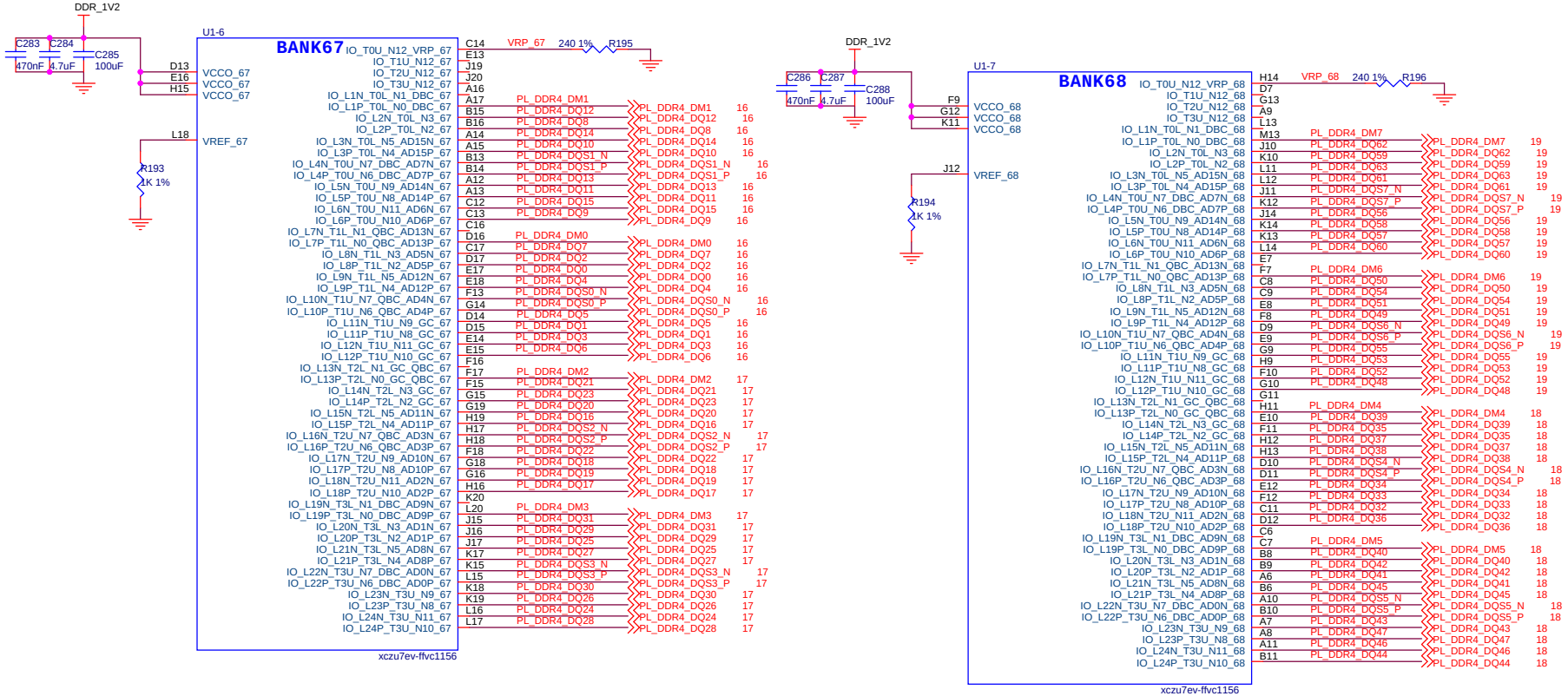

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Title	PAGE05 Z7 Bank67_68
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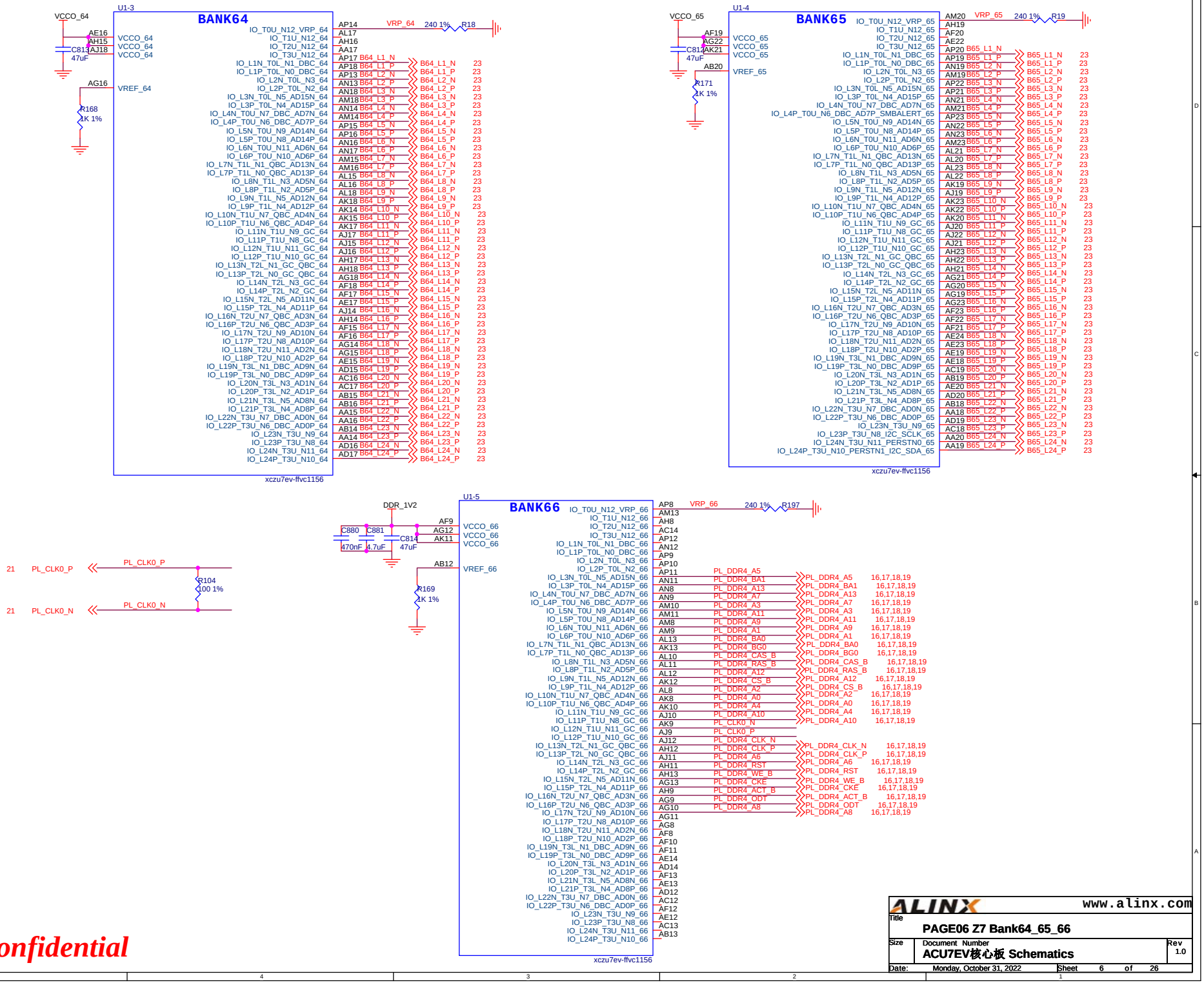
+1.8V
U1-3
BANK64
VCCO_64
VREF_64
xczu7ev-ffvc1156
+1.8V
U1-4
BANK65
VCCO_65
VREF_65
xczu7ev-ffvc1156
DDR_1V2
U1-5
BANK66
VCCO_66
VREF_66
xczu7ev-ffvc1156
PL_CLK0_P
PL_CLK0_N
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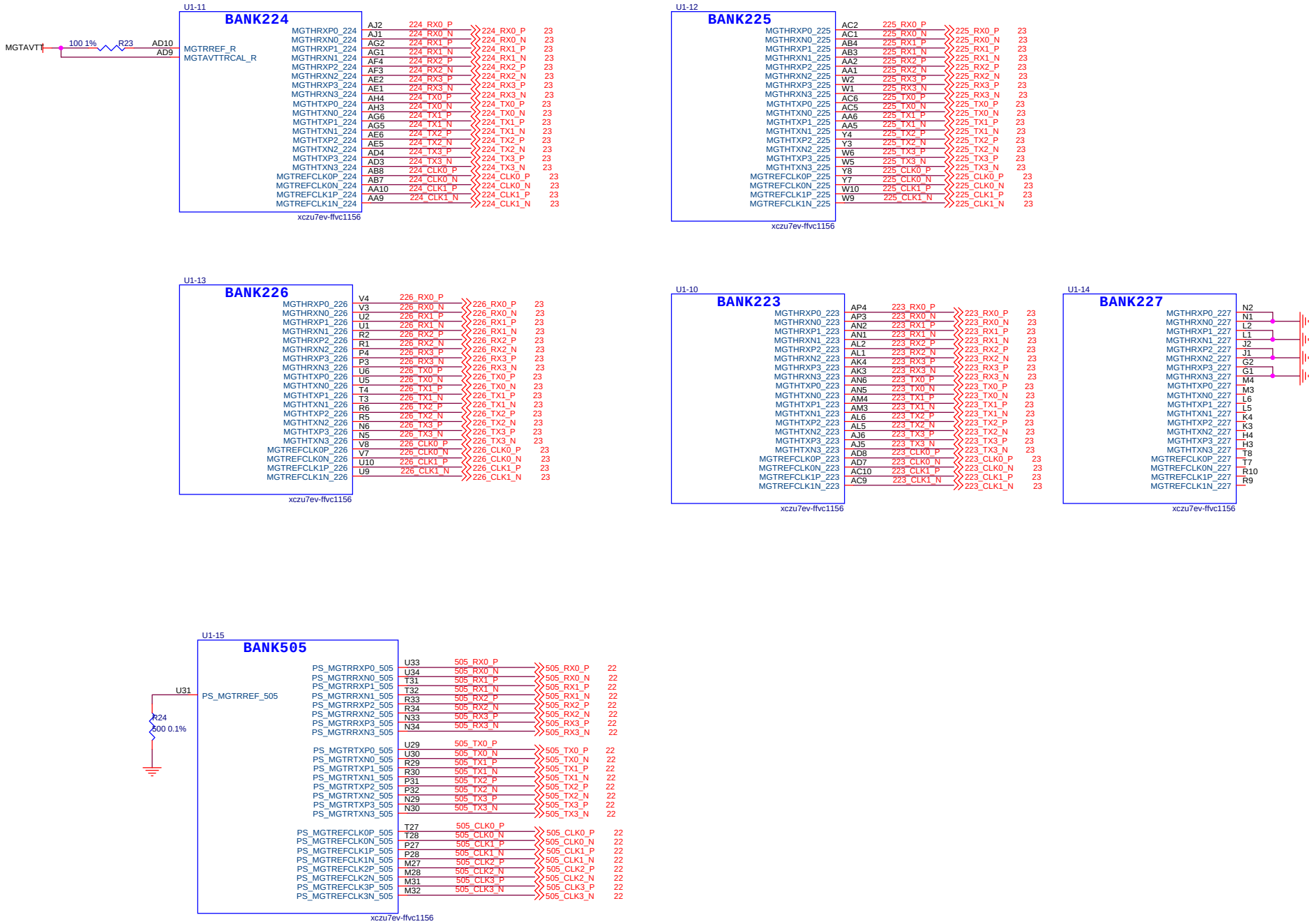

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Title: PAGE07 Z7 Bank505

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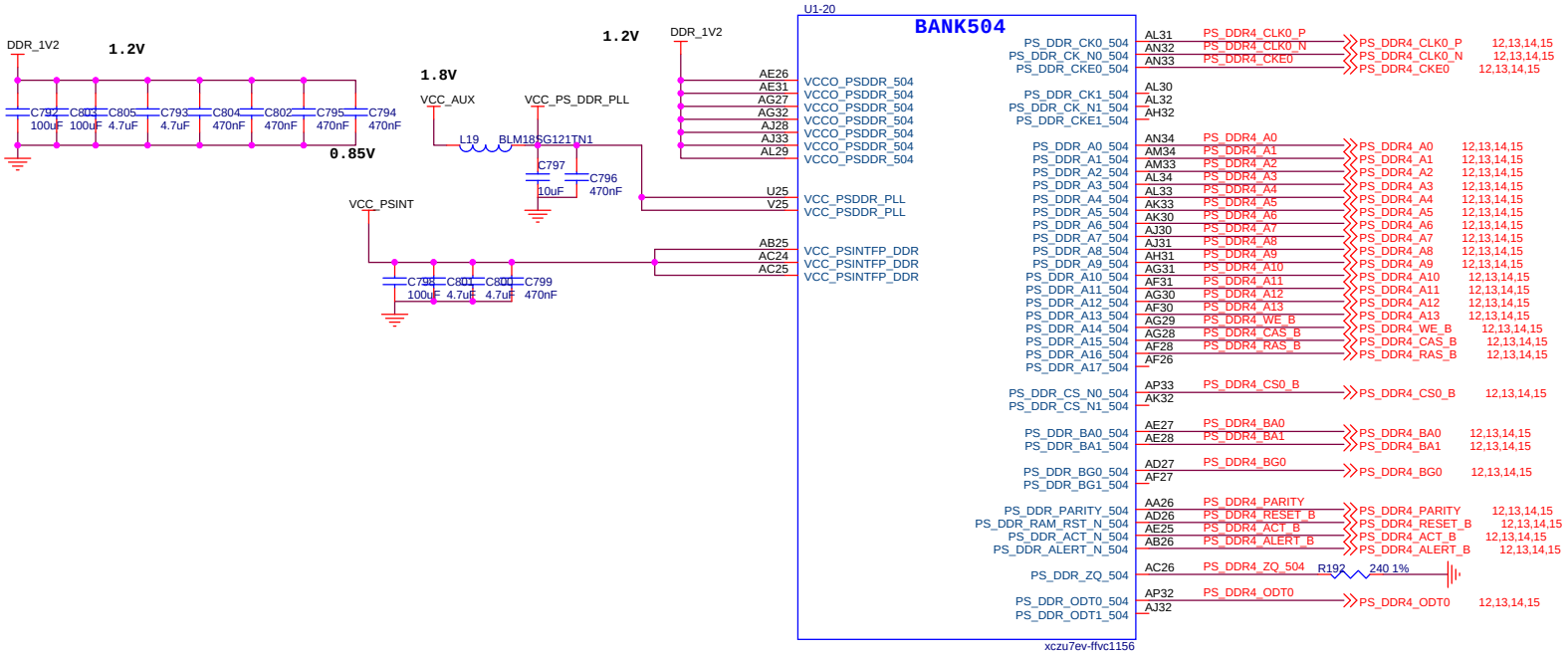

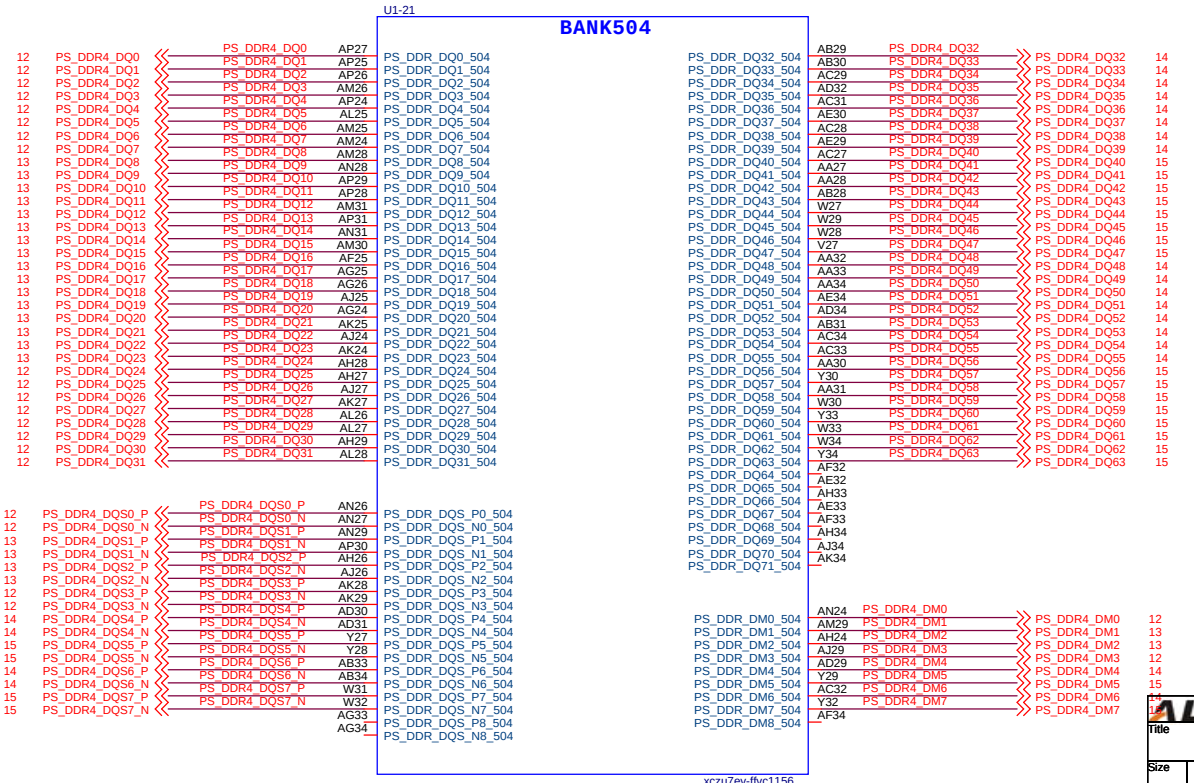

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Title: PAGE08 Z7 Bank504

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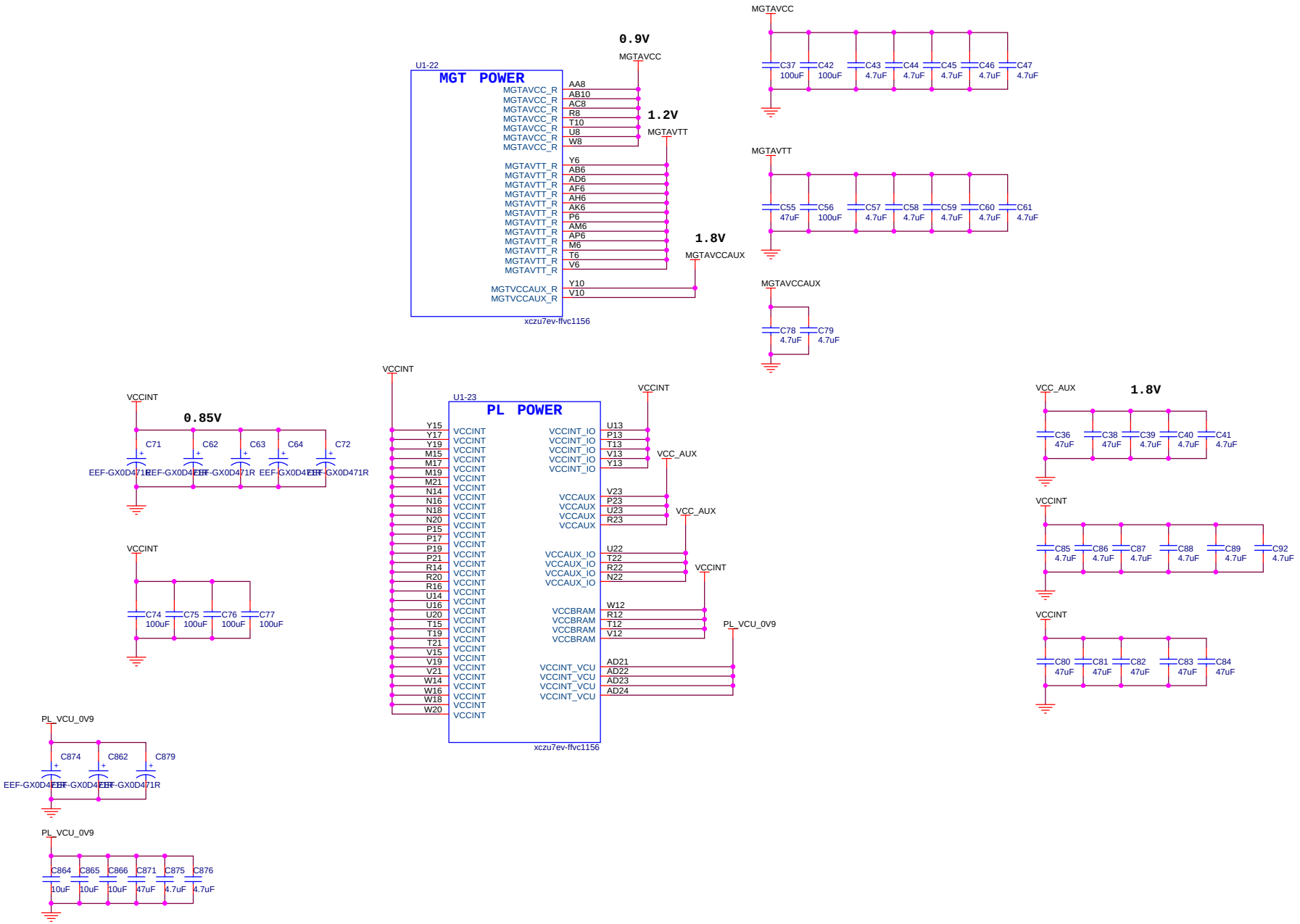
POWER ON: VCCINT/VCCINT_IO/VCCBRAM(+0.85V)->VCCAUX/VCCAUX_IO(+1.8V)->VCCO(+3.3V, +1.8V)



If all of the Quads in a power supply group are not used, the associated power pins can be left unconnected or tied to GND

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Title	PAGE09 Z7 PL Power1
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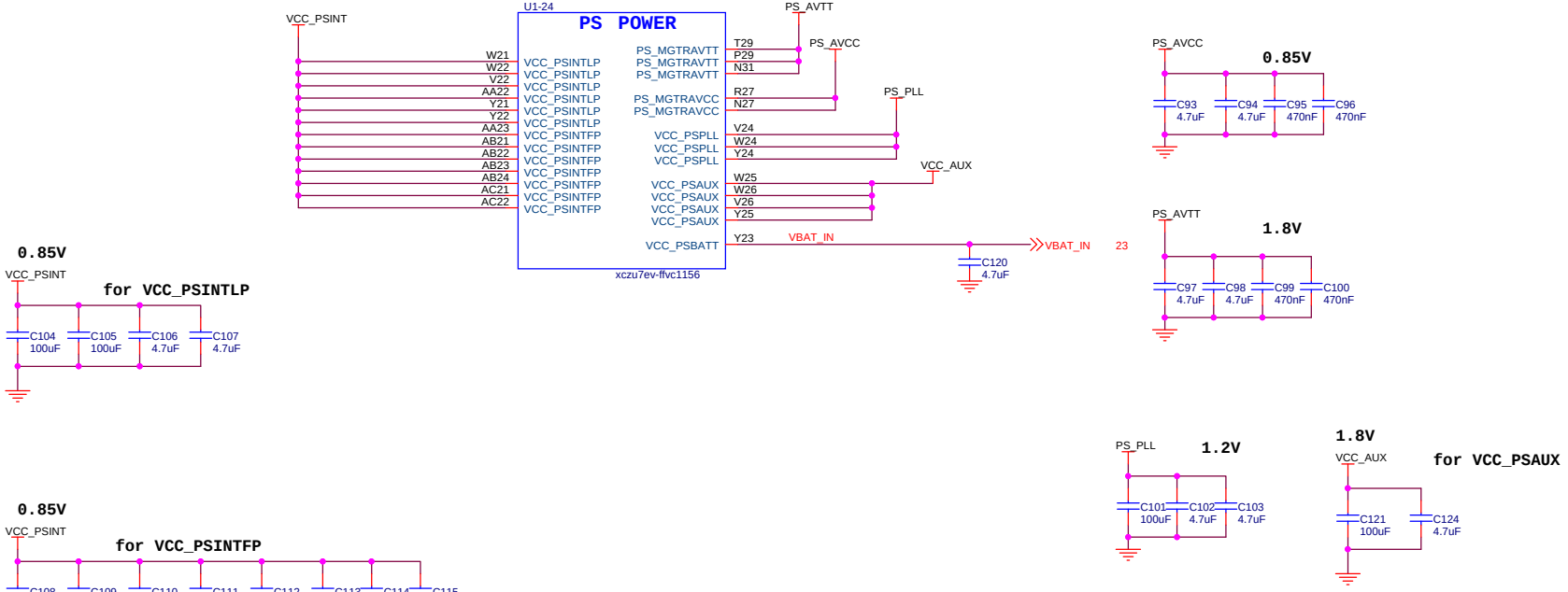
POWER ON: VCC_PSINTFP/VCC_PSINTFP_DDR(+0.85V)->VPS_MGTRAVCC(+0.9V),VCC_PSDDR_PLL(+1.8V)->VPS_MGTRAVTT(+1.8V),VCCO_PSDDR()

POWER ON: VCC_PSINTLP(+0.85V)->VCC_PSAUX(+1.8V),VCC_PSADC(+1.8V),VCC_PSPLL(+1.2V)->VCCO_PSIO(+1.8V)



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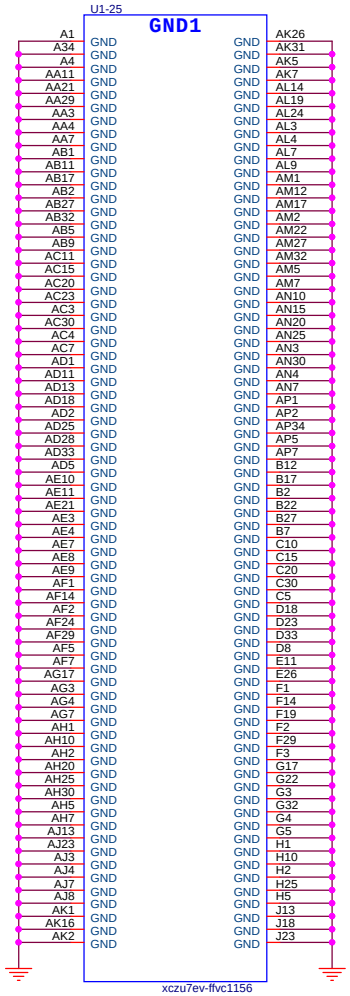

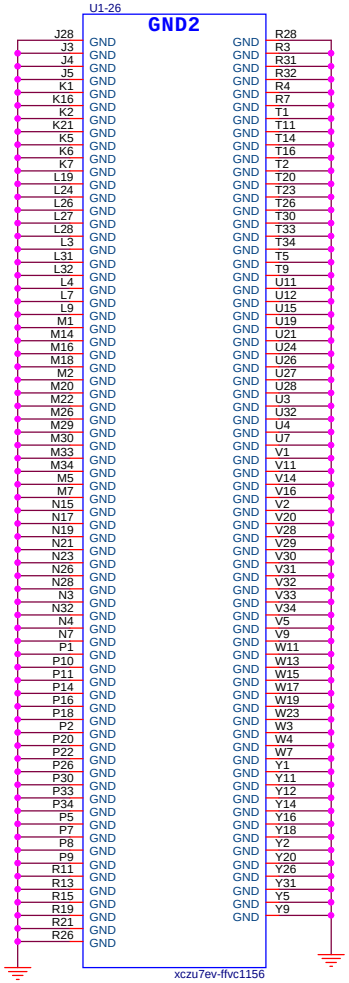

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Title: PAGE11 Z7 GND

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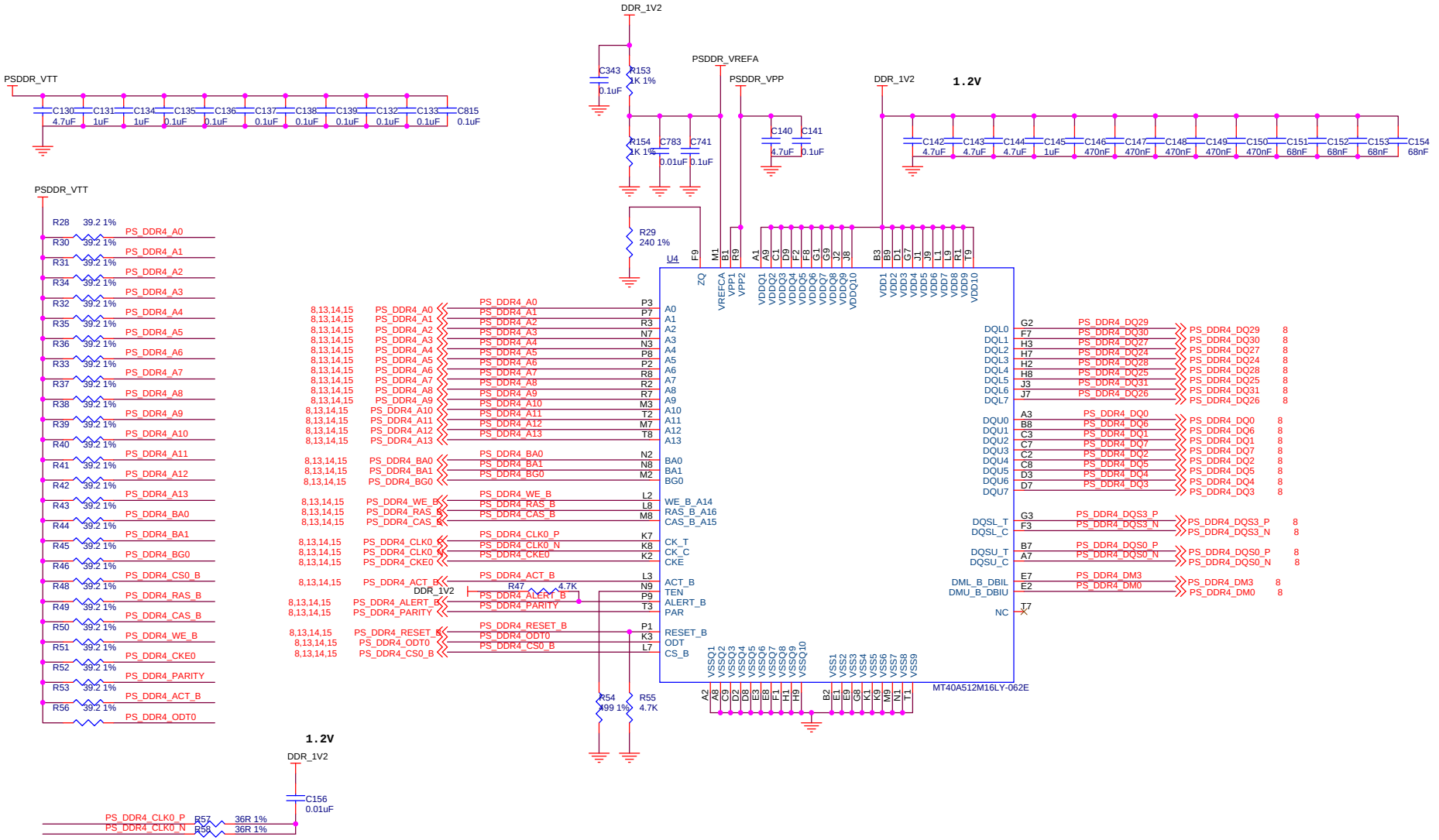

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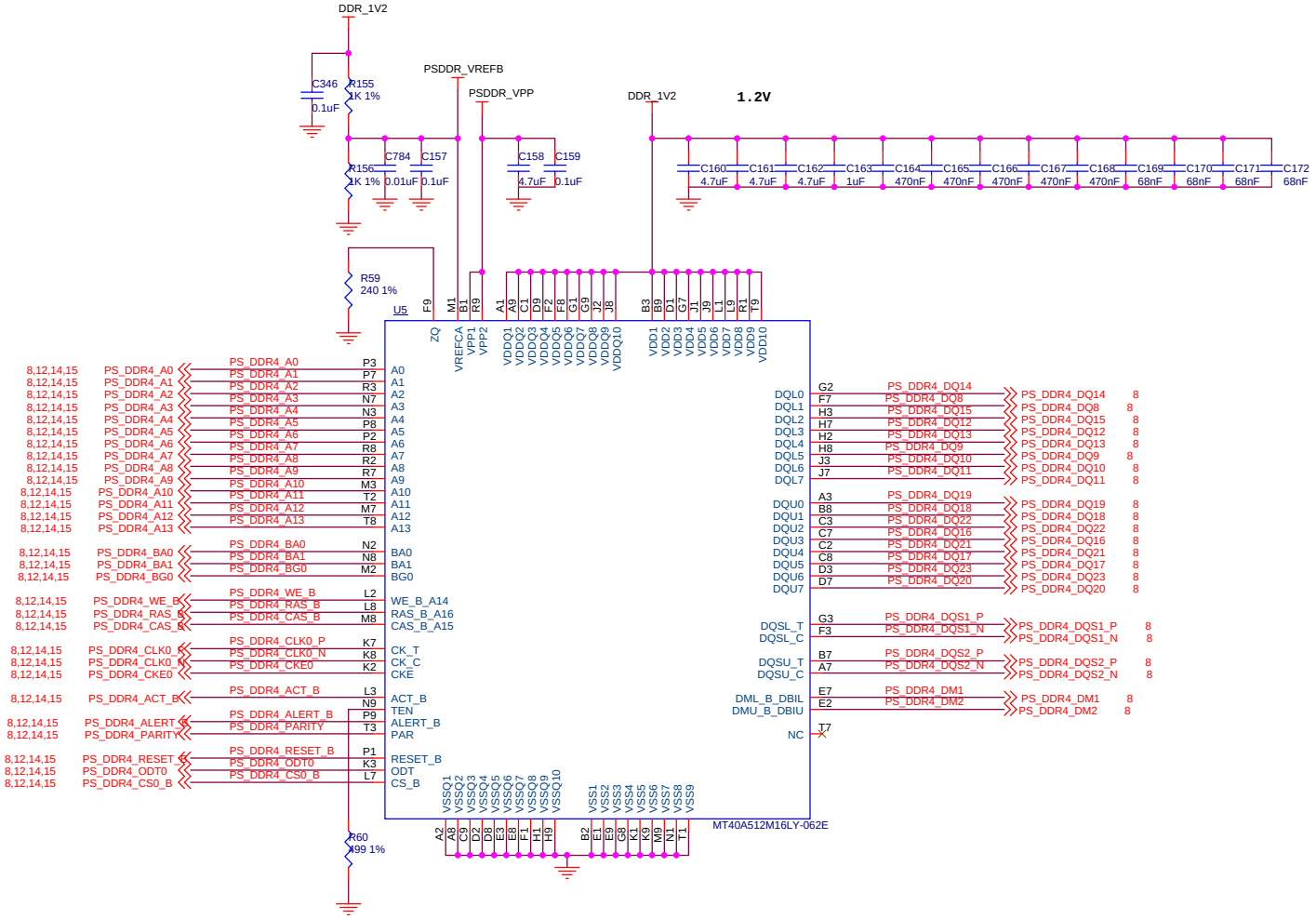

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Title	PAGE13 PS_DDR4_2
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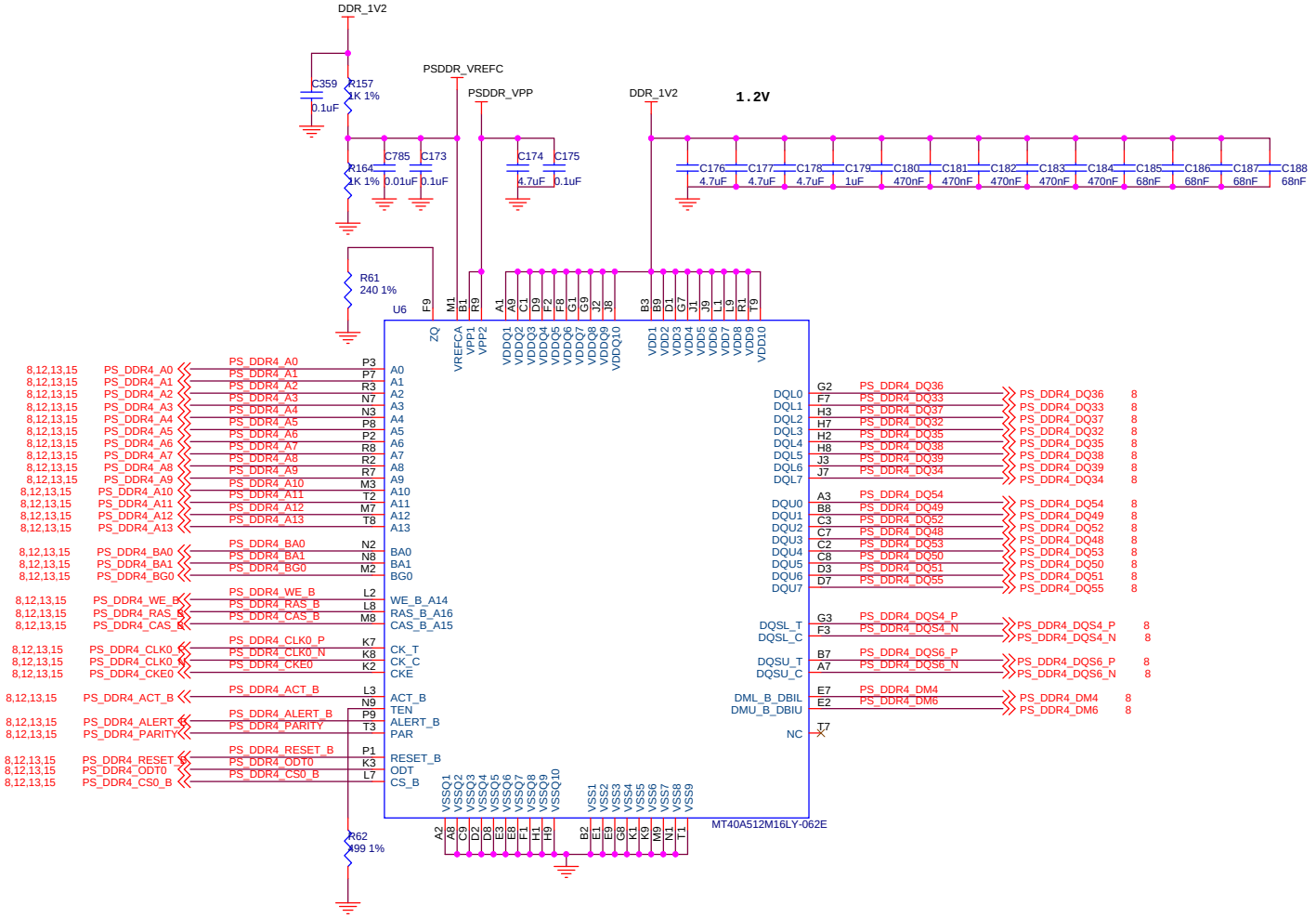

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Title: PAGE14 PS_DDR4_3

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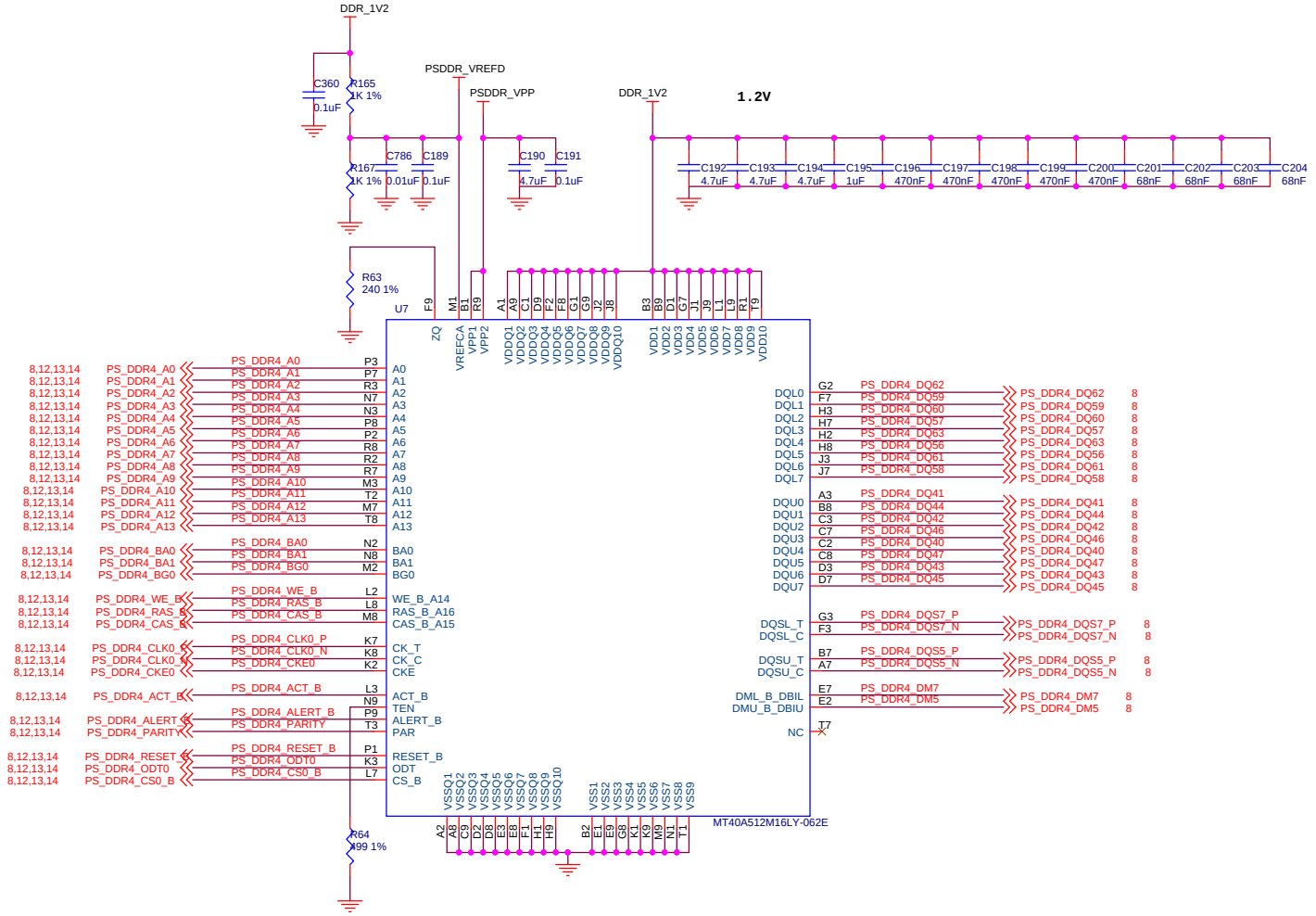

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Title: PAGE15 PS_DDR4_4

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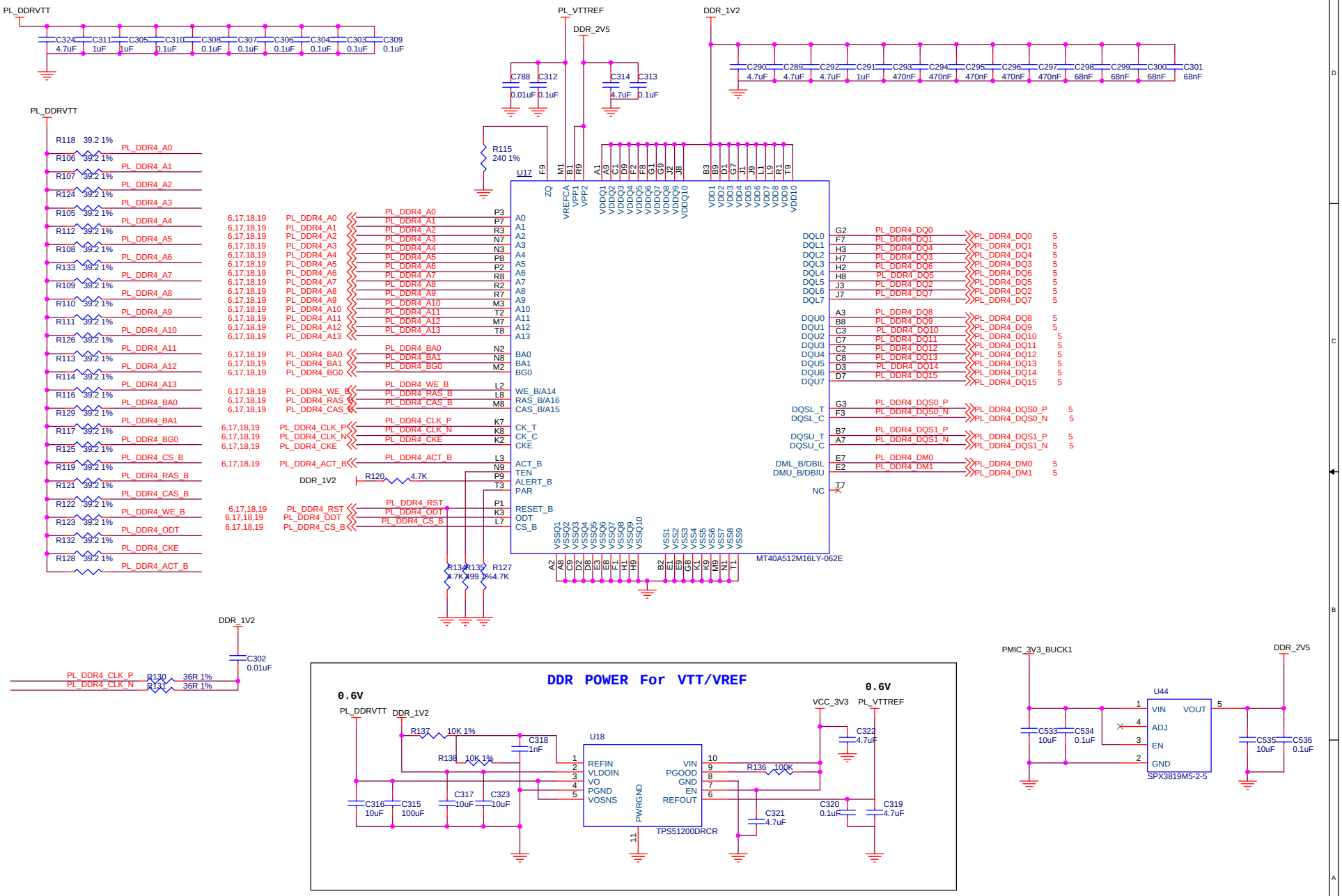

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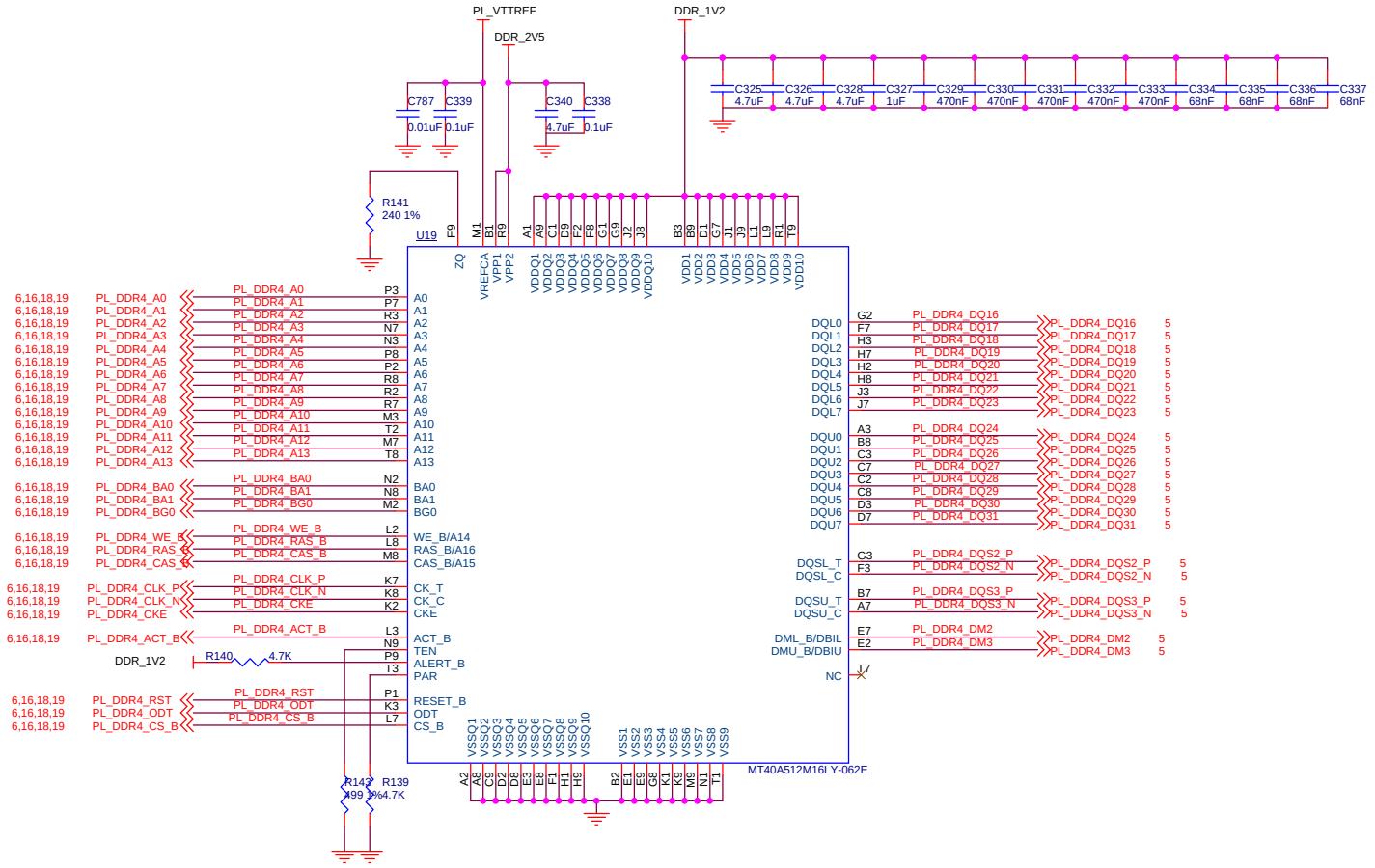

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Title: PAGE17 PL_DDR4_2

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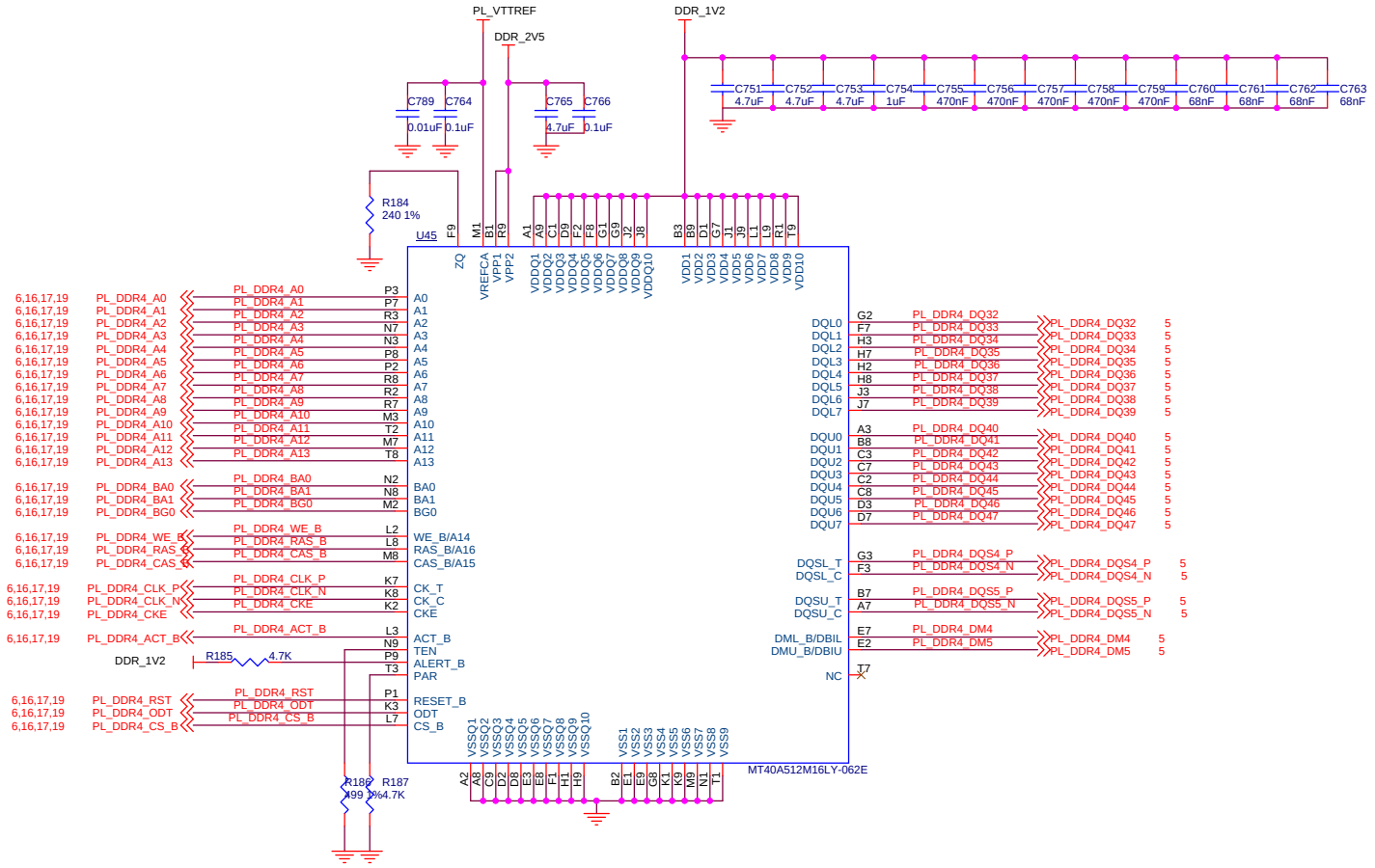

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Title: PAGE18 PL_DDR4_3

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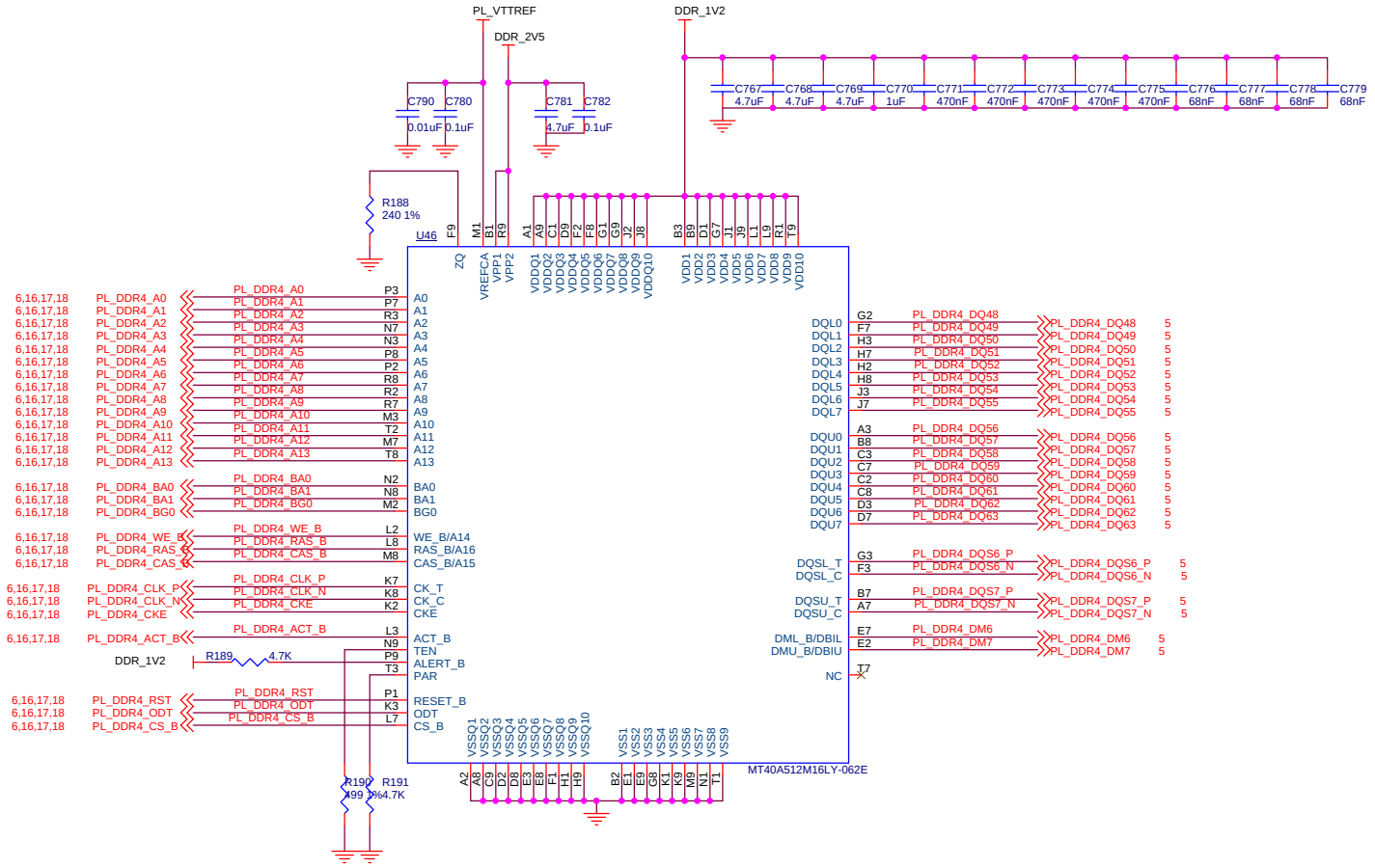

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Title: PAGE19 PL_DDR4_4

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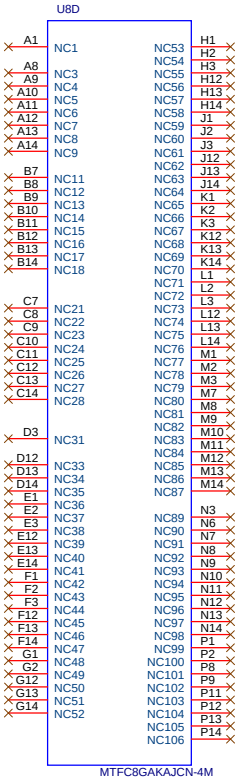

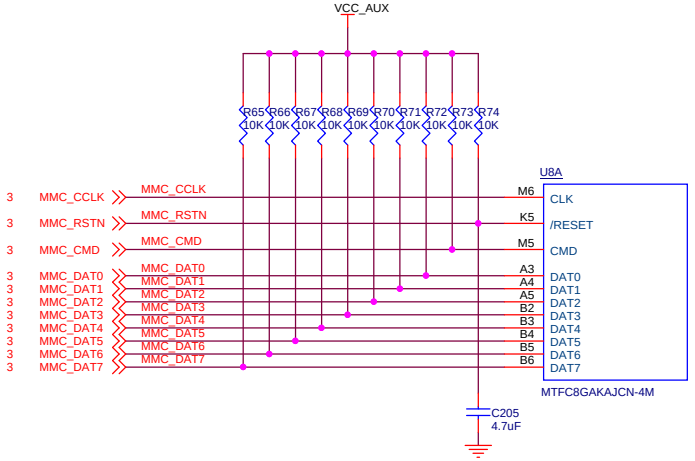

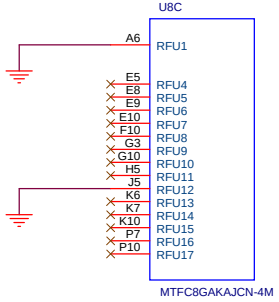

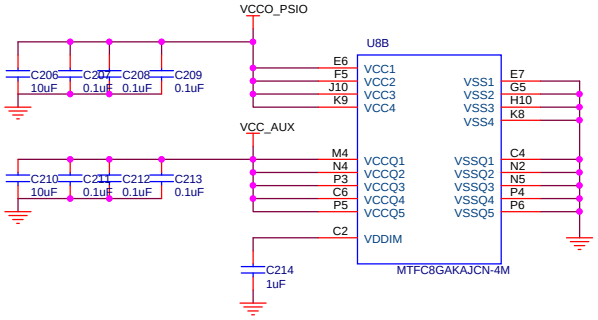

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Title	PAGE20 eMMC	
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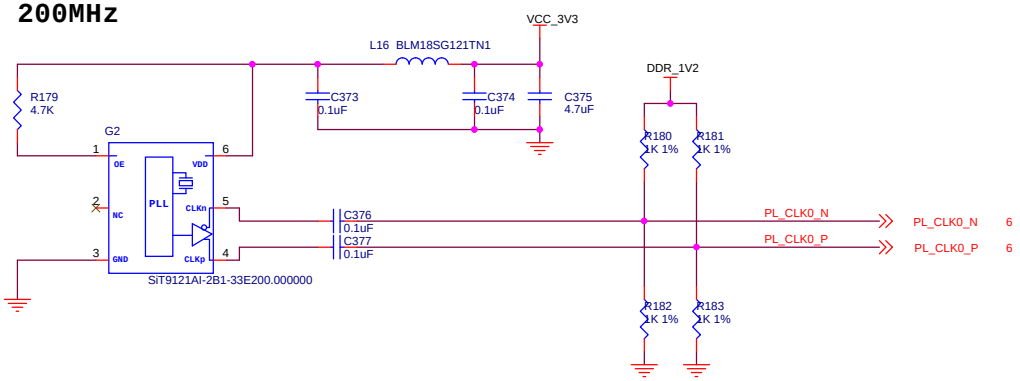
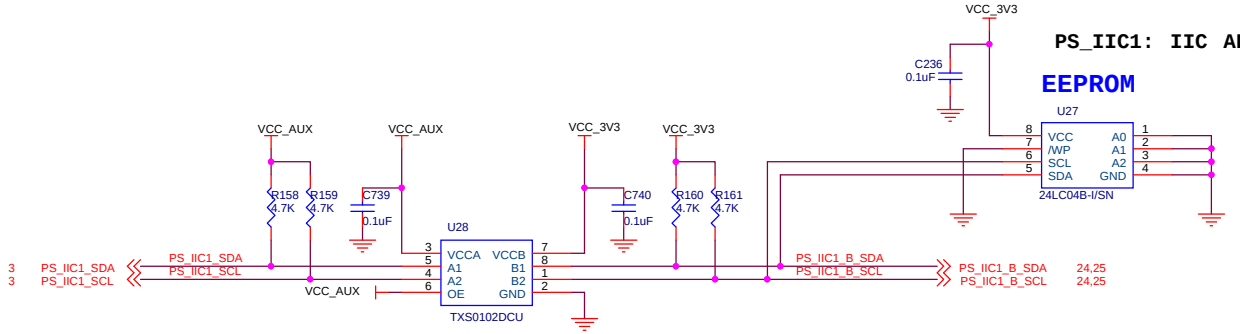
PL SYSTEM CLOCK

200MHz

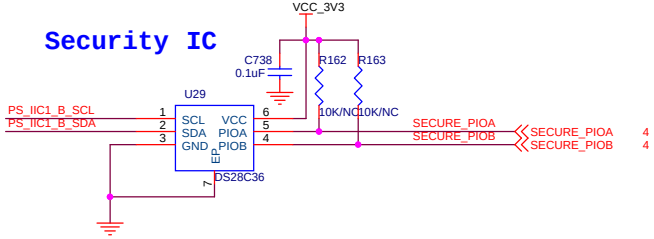


PS_IIC1: IIC ADDRESS IS 0x50

EEPROM



Security IC



PS_IIC1: IIC ADDRESS IS 0x1B

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Title	PAGE21 CLOCK & SECURITY
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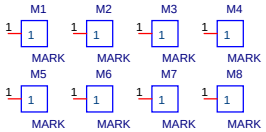
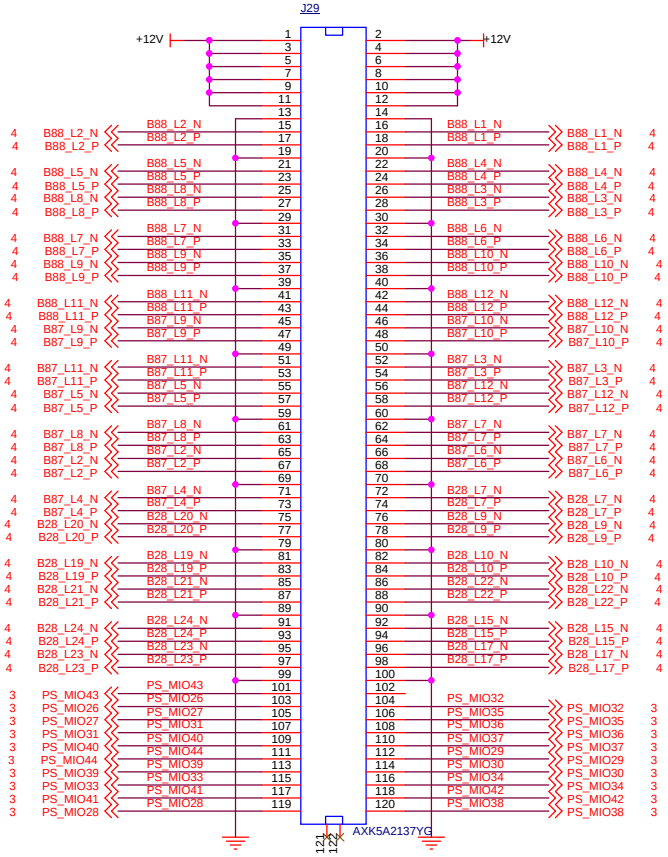
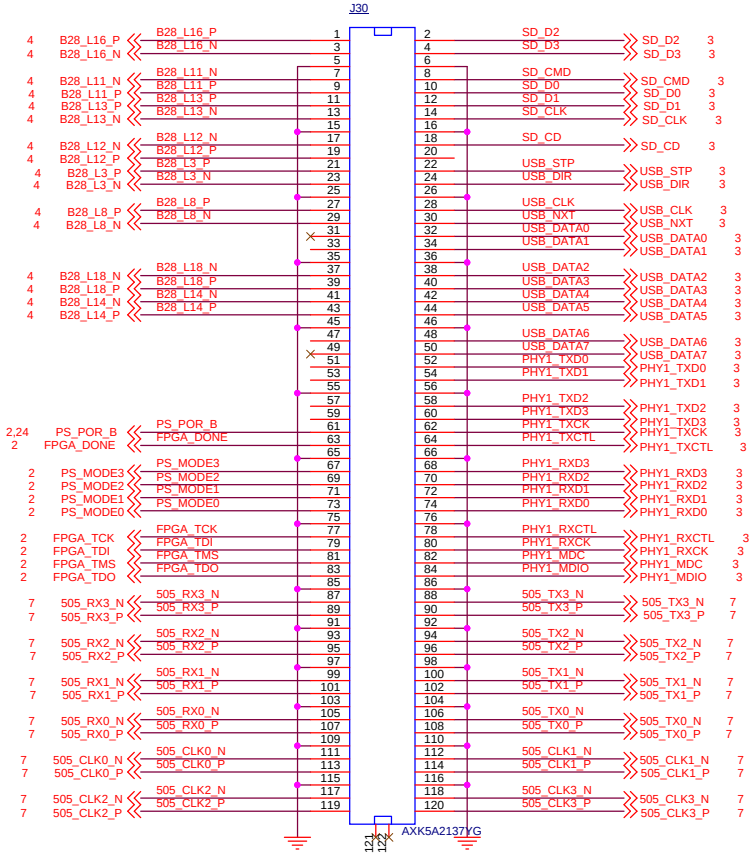
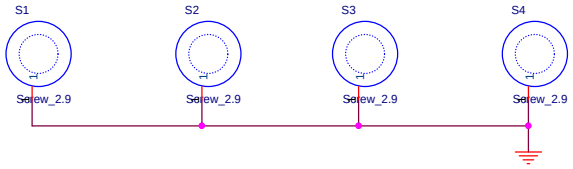


BANK28 IO Voltage is 1.8V Stardard
BANK87,88 IO Voltage is 3.3V Stardard

MIO/SD/USB/ETH IO Voltage is 1.8V Stardard







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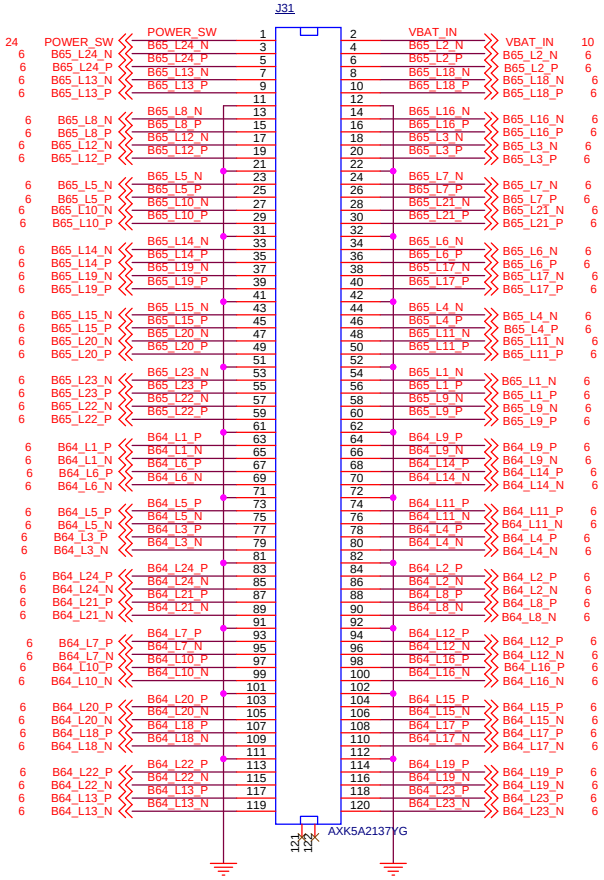
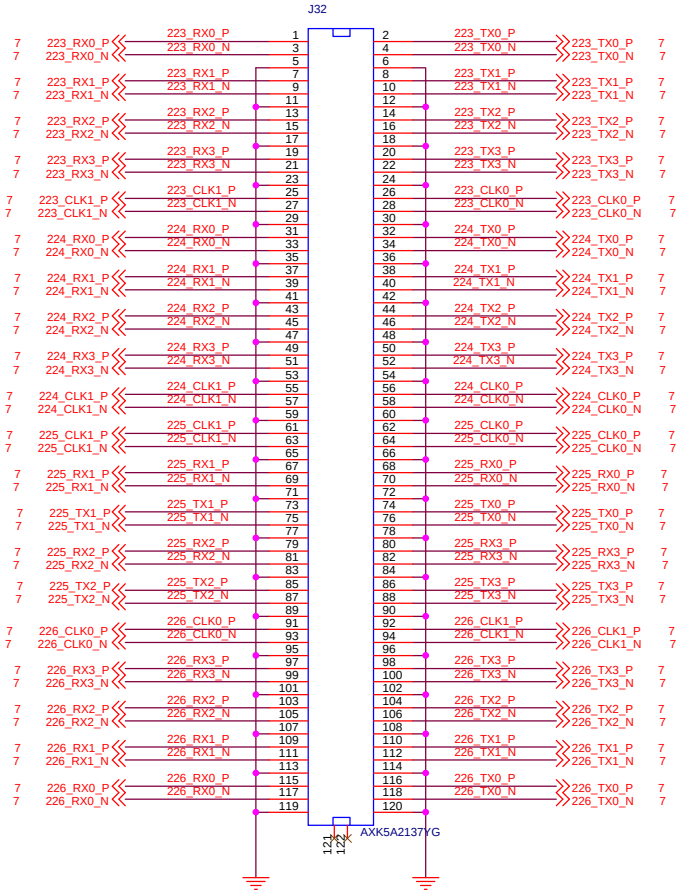
BANK65,66 IO Voltage is 1.8V Standard





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Title	PAGE23 Connector_2	
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CTL3=1

VCC_PSINT (BUCK2:0.85V) → VCCINT (U42:0.85V) → PMIC1_3V3_BUCK1 (BUCK1:3.3V) → MGTAVCC (BUCK4:0.9V) → MGTAVTT/PS_PLL (BUCK3:1.2V) → VCC_AUX/MGTAVTT (BUCK5:1.8V) → VCCO_PSIO (SWA1:3.3V) → PMIC1_BUCK6_1V2 (BUCK6:1.2V) → DIMM_VTT/DIMM_VPP (VTT_LDO:0.6V) (LDOA1:2.5V) → Power GOOD (GPO3)

GPO1=1 (PMIC1_BUCK2_PG)

CTL4=1 (PMIC1_VCCINT_PG)

GPO4=1 (PMIC1_BUCK4_PG)

not use

GPO1-----BUCK2_PG
GPO4-----BUCK4_PG
GPO3-----Power_PG

CTL1=1&CTL2=0-------BUCK6=1.2V
CTL3-------PS_FP_PWR_EN_LS
CTL4-------enable BUCK1
CTL5=1&CTL2=0------VTT_LDO=0.6V
CTL6=0-------BUCK2=0.85V

0.2A 2V5

MAX 1.8A 0V6
0.6A 1V5
0.6A 1V2
3.3V
1.8V

0.85V
1.2V 3A
0V9 3A
1.8V 3A
1.2V 6A

U12 TPS6508640RSKR

U13 U14 U15 CSD87381P

U76 U77 U78 SPX3819M5-1-8

Title: PAGE24 PMIC POWER

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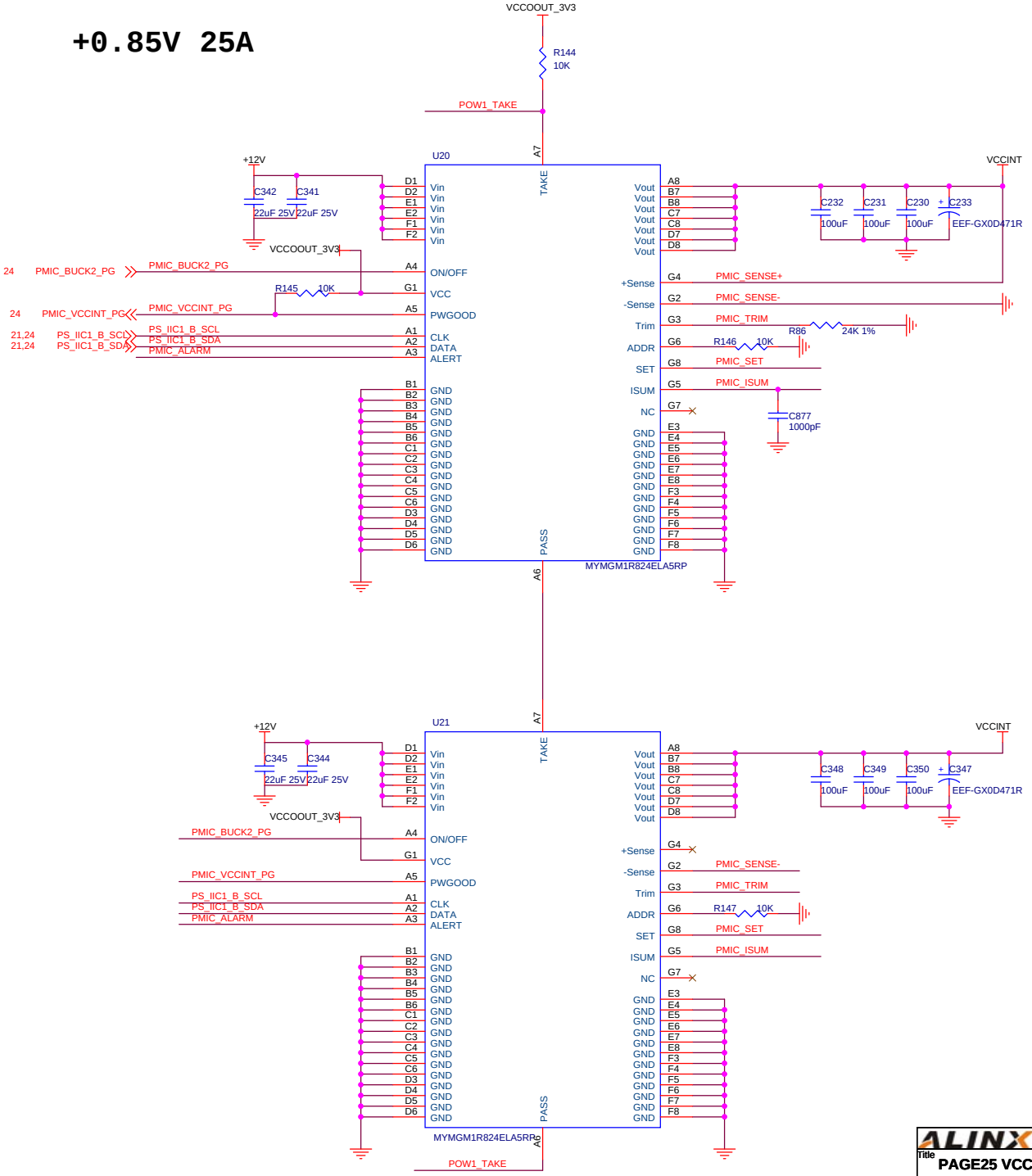
+0.85V 25A



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Title	PAGE25 VCCINT POWER
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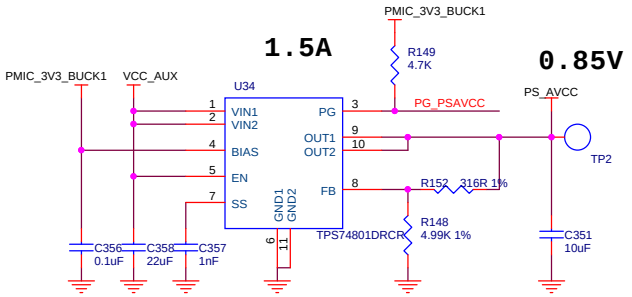
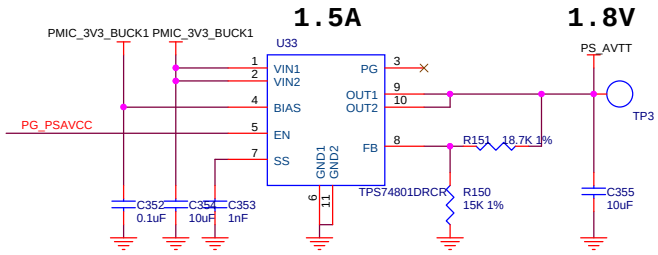
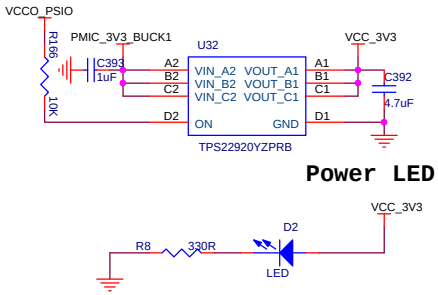
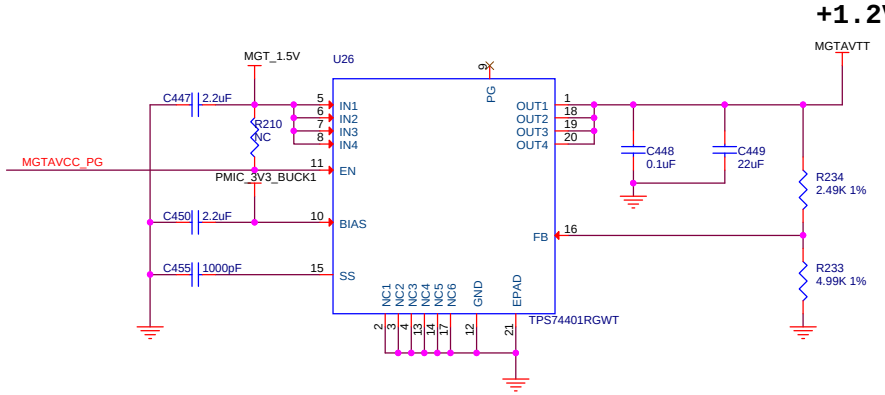
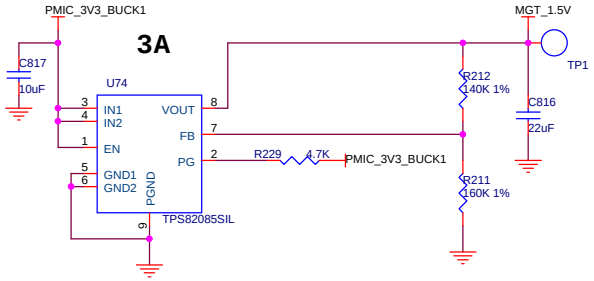


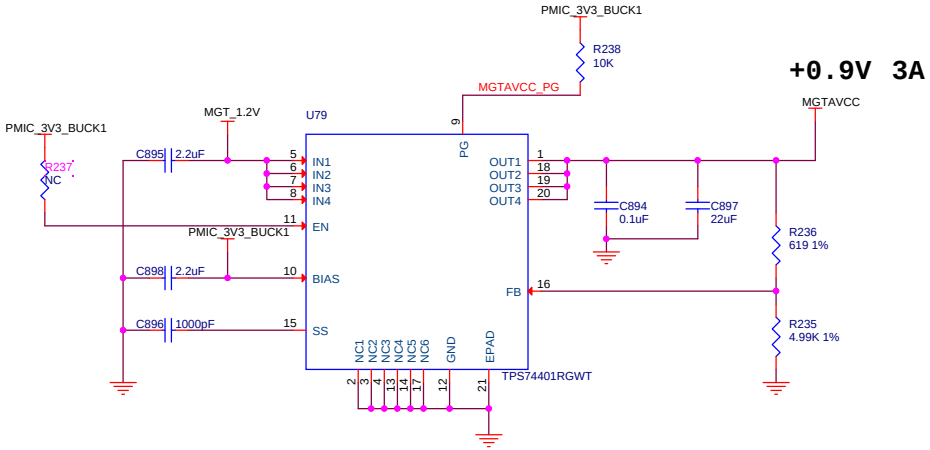


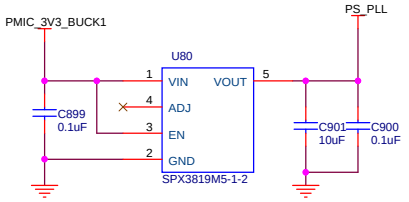






Vout=0.8 x (1 + R1/R2)





Vout=0.8 x (1 + R1/R2)

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