ZYNQ7000 FPGA Development Board AX7021 User Manual

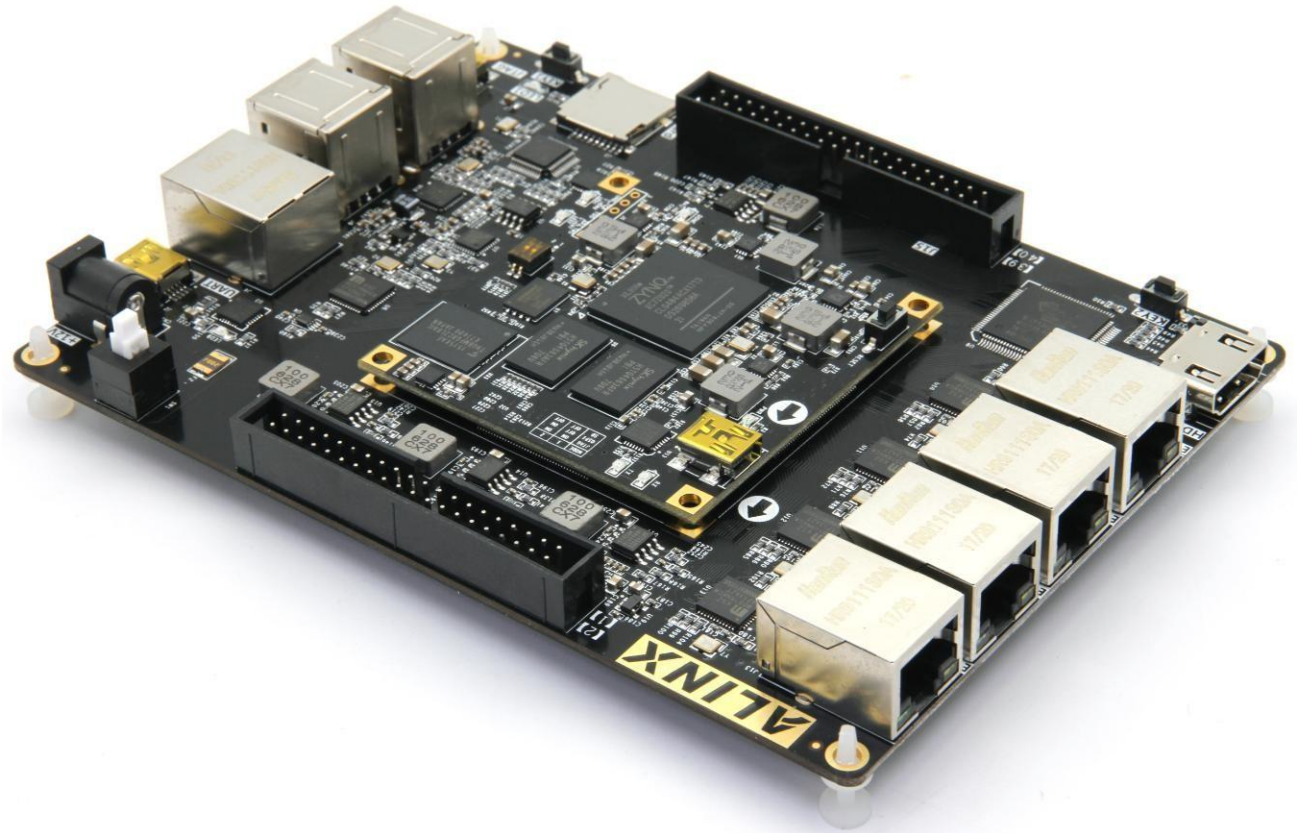
Version Record

Version	Date	Release By	Description
Rev 1.0	2019-03-27	Rachel Zhou	First Release
Rev 1.1	2020-09-21	Rachel Zhou	Correct the corresponding pins of B34_L15_N/P.

Table of Contents

This ZYNQ7000 FPGA development platform adopts the core board + carrier board mode, which is convenient for users to use the core board for secondary development. The core board uses XILINX's Zynq7000 SOC chip solution, which combines dual-core ARM Cortex-A9 and FPGA programmable logic on a single chip using ARM+FPGA SOC technology. In addition, the core board contains 2 pieces of 1GB high-speed DDR3 SDRAM chip, 1 piece 32GB eMMC memory chip and 1 piece 256Mb QSPI FLASH chip.

In the design of the carrier board, the user has extended a wealth of peripheral interfaces, such as 5-port Gigabit Ethernet interfaces, 4-port USB2.0 HOST interfaces, 1-port HDMI output interface, Uart serial port communication interface, SD card holder, 40-pin carrier header, etc. It meets the requirements of users for various Ethernet high-speed data exchange, data storage, video transmission processing and industrial control. It is a "professional" ZYNQ development platform. For high-speed Ethernet data transmission and exchange, the pre-validation and post-application of data processing is possible. This product is very suitable for students, engineers and other groups engaged in ZYNQ development.



Part 1: FPGA Development Board Introduction

Here, a brief introduction to the AX7021 ZYNQ FPGA development platform.

The entire structure of the development board, the core board + carrier board mode design. A high-speed inter-board connector is used between the core board and the carrier board.

The core board is mainly composed of the minimum system of ZYNQ7020 + 2 DDR3 + eMMC + QSPI FLASH. It undertakes the high-speed data processing and storage function of the ZYNQ system. The data width between the ZYNQ7020 and the two DDR3s is 32 bits, and the two DDR3 capacities up to 1GB. The 32GB eMMC FLASH memory chip and 256Mb QSPI FLASH are used to statically store the ZYNQ operating system, file system and user data. Users can select different startup modes through the DIP switch on the core board. The ZYNQ7020 uses Xilinx's Zynq7000 series of chips, model number XC7Z020-2CLG484I. The ZYNQ7020 chip can be divided into processor system part Processor System (PS) and programmable logic part Programmable Logic (PL).

The carrier board expands the rich peripheral interface for the core board, including 5 Gigabit Ethernet interfaces, 4-port USB2.0 HOST interfaces, 1-port HDMI output interface, 1-port SD Card interface, 1-port UART USB serial port interface, 1-port SD Card interface, 2-port 40-pin carrier headers and some button LEDs.

Figure 1-1-1 is the block diagram of the FPGA development board AX7021:

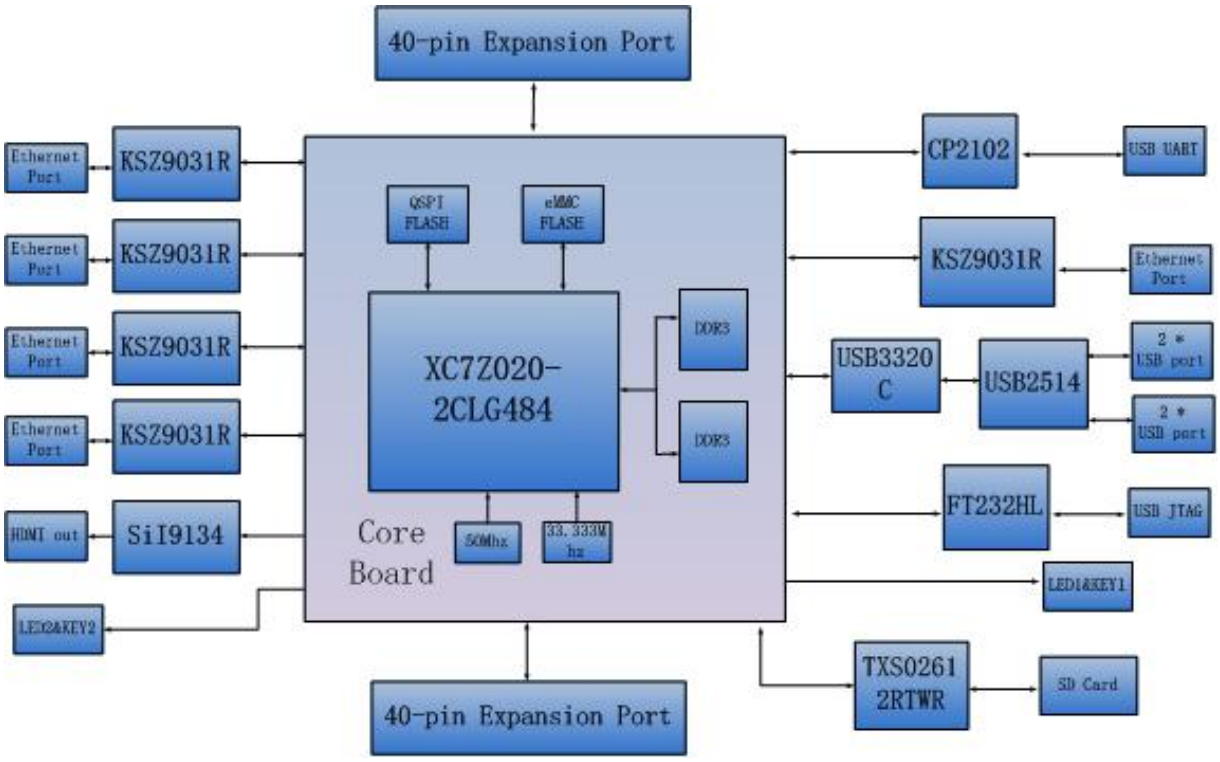


Figure 1-1-1: The block diagram of AX7021

The interfaces and features included in the development board.

➢ ZYNQ7000 Core Board

It consists of XC7Z020+1GB DDR3+32GB eMMC FLASH + 256Mb QSPI FLASH. In addition, two crystal oscillators provide clocks, one is 33.3333MHz for PS system and the other is 50MHz for PL logic.

➢ Gigabit Ethernet Interface

5 channels 10/100M/1000M Ethernet RJ45 interface for Ethernet data exchange with computers or other network devices. The network interface chip uses Micrel's KSZ9031 industrial grade GPHY chip, one Ethernet connection to the PS end of the ZYNQ chip, and four Ethernet connections to the PL end of the ZYNQ chip.

➢ HDMI Output Display

One HDMI output interface uses SIL9134 HDMI encoding chip of Silion Image Corporation, which supports up to 1080P@60Hz output and supports 3D output.

➢ USB Interface

1 JTAG debug interface, using MINI USB interface, users can debug and download ZYNQ system through USB cable and onboard JTAG circuit.

➢ LED Light

9 LEDs, include 6 on the core board and 3 on the extension board. There are 1 power indicator, 1 DONE configuration indicator, 2 user indicators and 2 serial port transceiver indicators on the core board. There are 1 power indicator and 2 user indicators on the extension board.

➢ Button

3 buttons, 1 reset button on the core board, and 2 user buttons on the extension board.

Part 2: AC7021 Core Board

2.1 Introduction

The AC7021 (core board model, the same below) core board is an FPGA development board based on the Zynq chip XC7Z020-2CLG484I of the XILINX ZYNQ7000 series. The ZYNQ chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. The ZYNQ FPGA chip contains a wide range of programmable logic cells, DSP and internal RAM.

The core board uses two SK Hynix DDR3 chips (H5TQ4G63AFR-PBI), each with a 4Gbit DDR capacity; two DDR chips form a 32-bit data bus width, and the read and write data clock frequency between ZYNQ FPGA and DDR3 is up to 533Mhz; such a configuration can meet the system's high bandwidth data processing needs

In order to connect to the carrier board, the four board-to-board connectors of the core board extend the USB interface of the PS side, the Gigabit Ethernet interface, the SD card interface and other remaining MIO ports. As well as almost all IO ports (198) of BANK13, BANK33, BAN34 and BANK35 on the PL side, the level of IO of BANK33 and BANK34 can be modified by replacing the

LDO chip on the core board to meet the requirements of users with different level interfaces. For users who need a lot of IOs, this core board will be a good choice. Moreover, the IOs connection part, the routing between the ZYNQ FPGA chip and the interface is equal length and differential processing. The core board size is only 2.36 inch* 2.36 inch, which is very suitable for secondary development.

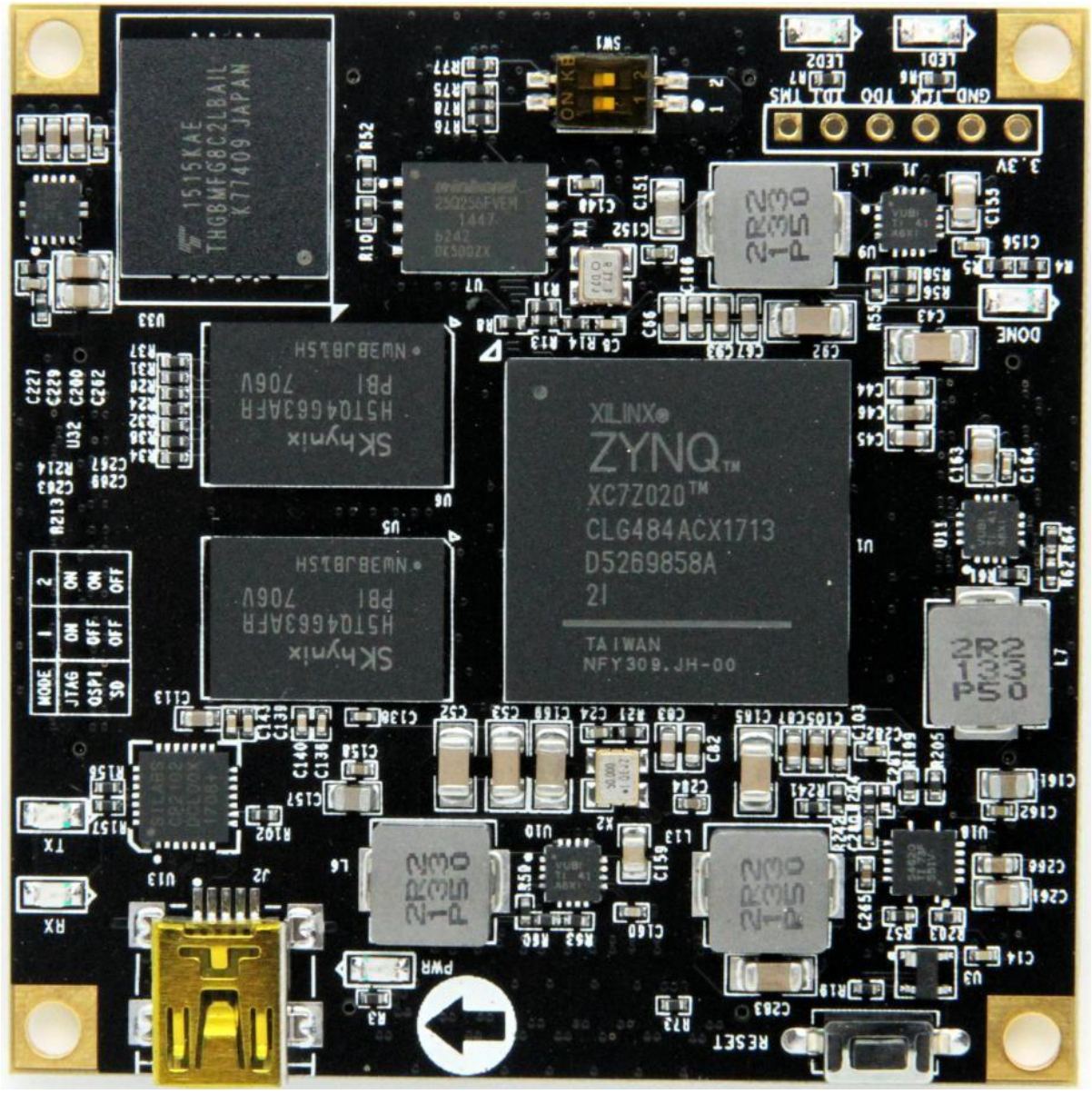


Figure 2-2-1: AC7021Core board Front View

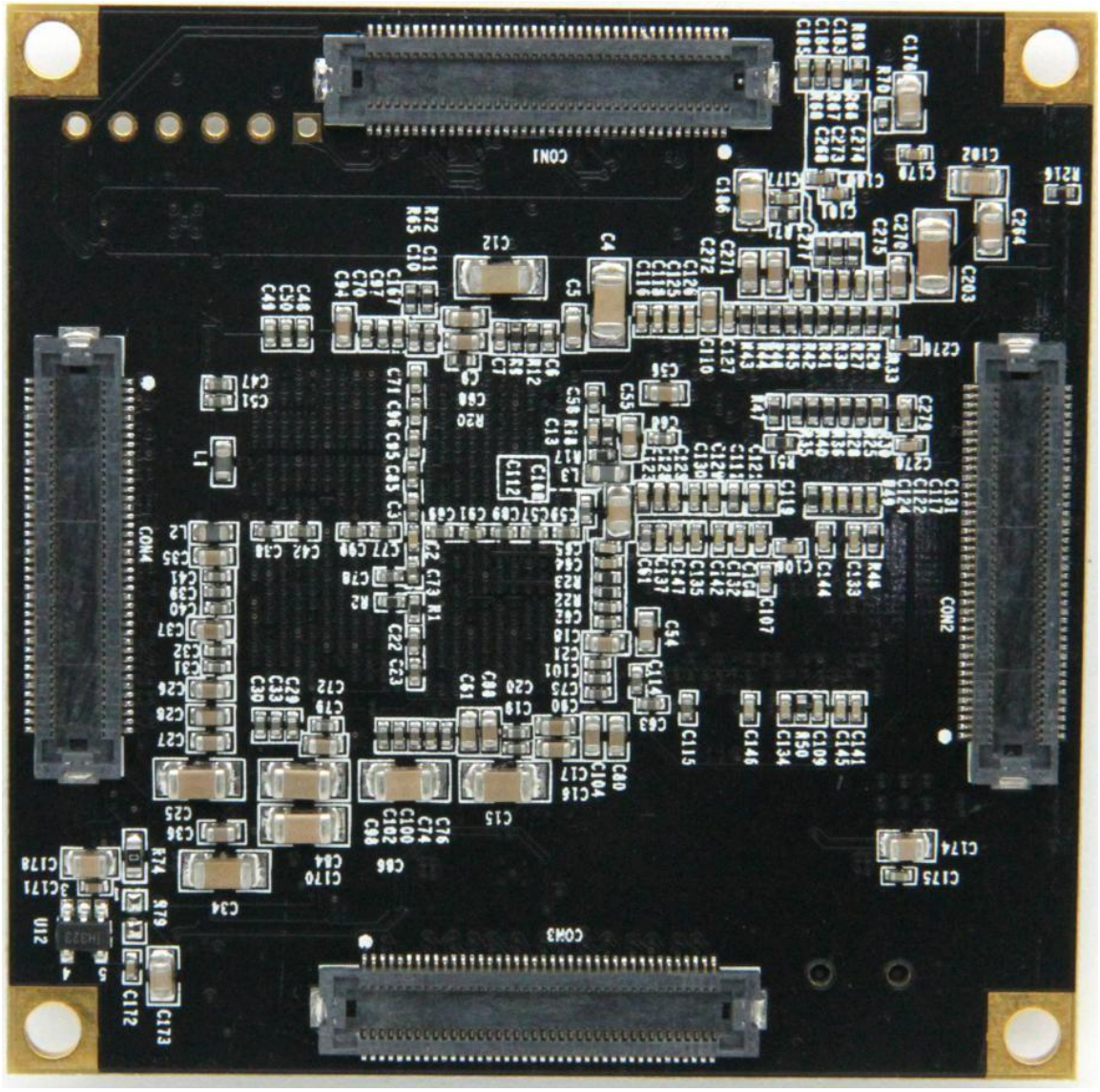


Figure 2-2-2:AC7021 core board rear view

2.2 ZYQN Chip

The development board uses Xilinx's Zynq7000 series chip, model XC7Z020-2CLG484I. The chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO, etc. The PS can operate independently and start up at power up or reset. Figure 2-2-3 detailed the Overall Block Diagram of the ZYNQ7000 Chip.

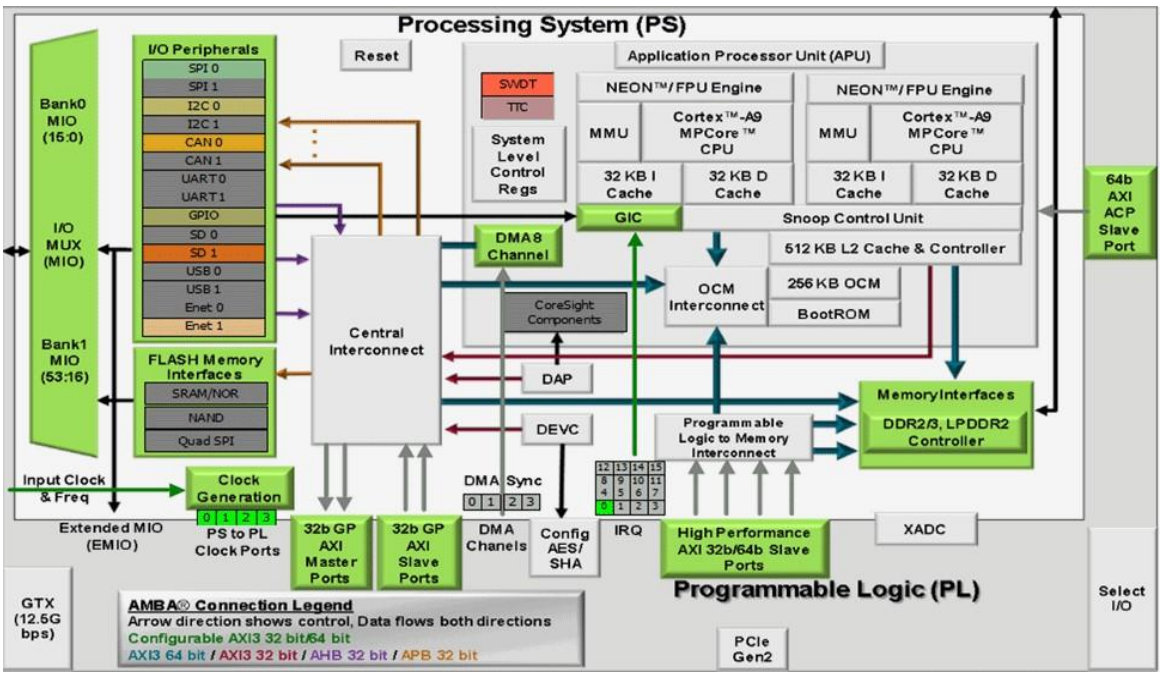


Figure 2-2-3: Overall Block Diagram of the ZYNQ7000 Chip

The main parameters of the PS system part are as follows:

- ARM dual-core CortexA9-based application processor, ARM-v7 architecture, up to 1GHz
- 32KB level 1 instruction and data cache per CPU, 512KB level 2 cache 2 CPU shares
- On-chip boot ROM and 256KB on-chip RAM
- External storage interface, support 16/32 bit DDR2, DDR3 interface
- Two Gigabit NIC support: divergent-aggregate DMA, GMII, RGMII, SGMII interface
- Two USB2.0 OTG interfaces, each supporting up to 12 nodes
- Two CAN2.0B bus interfaces
- Two SD card, SDIO, MMC compatible controllers
- 2 SPIs, 2 UARTs, 2 I2C interfaces
- 4 groups of 32bit GPIO, 54 (32+22) as PS system IO, 64 connected to PL
- High bandwidth connection within PS and PS to PL

The main parameters of the PL logic part are as follows:

- LogicCells: 85K
- Look-up-tables (LUTs):53,200
- Flip-flops:106,400
- 18x25MACCs：220;
- BlockRAM：4.9Mb
- Two AD converters for on-chip voltage, temperature sensing and up to 17 external differential input channels, 1MBPS

XC7Z020-2CLG484I chip speed grade is -2, industrial grade, package is BGA484, pin pitch is 0.024 inch, the specific chip model definition of ZYNQ7000 series is shown in Figure 2-2-4

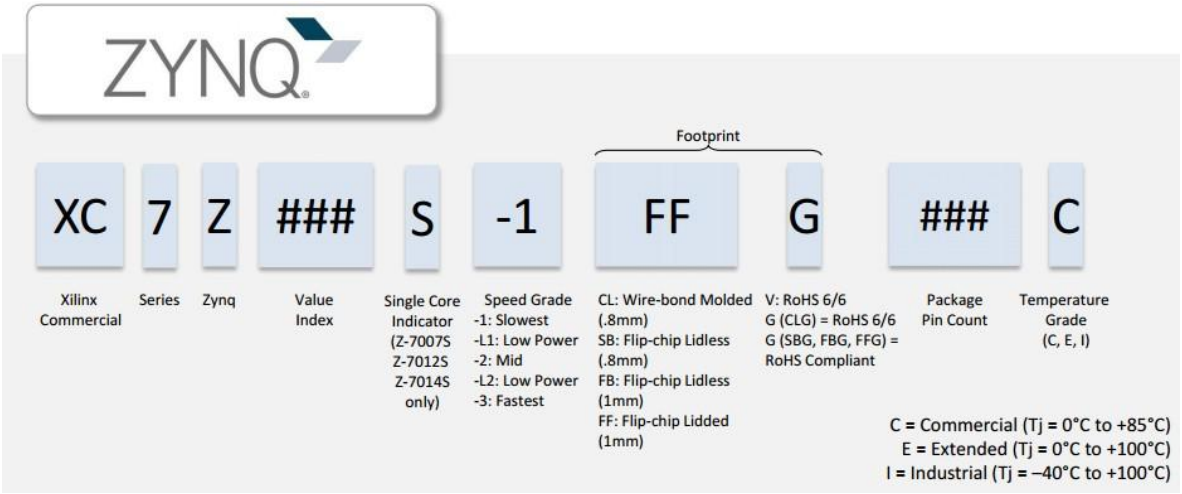


Figure 2-2-4: The Specific Chip Model Definition of ZYNQ7000 Series

Figure 2-2-5: TheXC7Z020 chip used on the Core Board

2.3 DDR3 DRAM

The AC7021 core board is equipped with two SK Hynix DDR3 SDRAM chips (1GB total), model H5TQ4G63AFR-PBI. The bus width of DDR3 SDRAM is 32 bits in total. DDR3 SDRAM has a maximum operating speed of 533MHz (data rate 1066Mbps). The DDR3 memory system is directly connected to the memory interface of the BANK 502 of the ZYNQ Processing System (PS). The specific configuration of DDR3 SDRAM is shown in Table 2-3-1

Bit Number	Chip Model	Capacity	Factory
U5,U6	H5TQ4G63AFR-PBI	256M x 16bit	SK Hynix

Table 2-3-1: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

The hardware connection of DDR3 DRAM is shown in Figure 2-3-1:

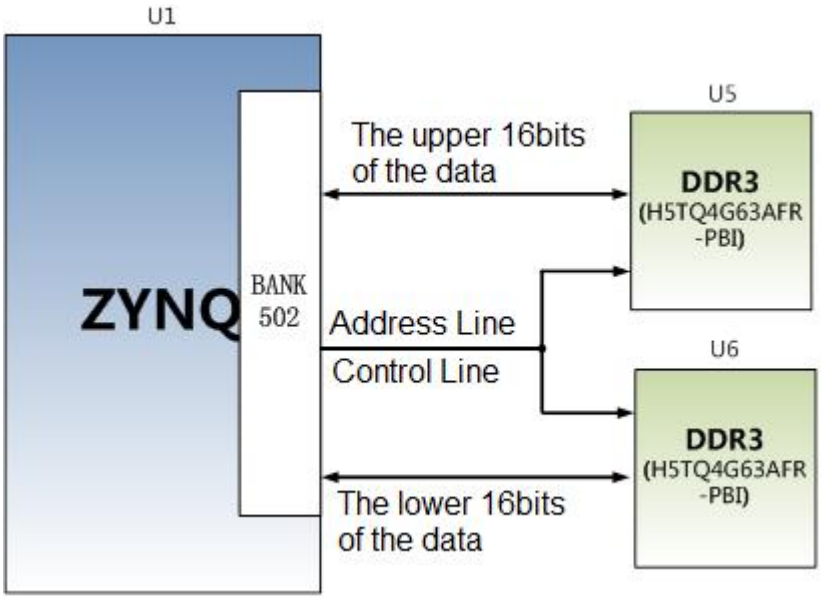


Figure 2-3-1: The Schematic part of DDR3 DRAM

Figure 2-3-2: DDR3 DRAM on the Core Board

DDR3 DRAM Pin Assignment

Signal Name	ZYNQ Pin Name	Pin Number
DDR3_DQS0_P	PS_DDR_DQS_P0_502	C2
DDR3_DQS0_N	PS_DDR_DQS_N0_502	D2
DDR3_DQS1_P	PS_DDR_DQS_P1_502	H2
DDR3_DQS1_N	PS_DDR_DQS_N1_502	J2
DDR3_DQS2_P	PS_DDR_DQS_P2_502	N2
DDR3_DQS2_N	PS_DDR_DQS_N2_502	P2
DDR3_DQS3_P	PS_DDR_DQS_P3_502	V2
DDR3_DQS4_N	PS_DDR_DQS_N3_502	W2
DDR3_D0	PS_DDR_DQ0_502	D1
DDR3_D1	PS_DDR_DQ1_502	C3
DDR3_D2	PS_DDR_DQ2_502	B2
DDR3_D3	PS_DDR_DQ3_502	D3
DDR3_D4	PS_DDR_DQ4_502	E3
DDR3_D5	PS_DDR_DQ5_502	E1
DDR3_D6	PS_DDR_DQ6_502	F2
DDR3_D7	PS_DDR_DQ7_502	F1
DDR3_D8	PS_DDR_DQ8_502	G2
DDR3_D9	PS_DDR_DQ9_502	G1
DDR3_D10	PS_DDR_DQ10_502	L1
DDR3_D11	PS_DDR_DQ11_502	L2
DDR3_D12	PS_DDR_DQ12_502	L3
DDR3_D13	PS_DDR_DQ13_502	K1
DDR3_D14	PS_DDR_DQ14_502	J1
DDR3_D15	PS_DDR_DQ15_502	K3
DDR3_D16	PS_DDR_DQ16_502	M1
DDR3_D17	PS_DDR_DQ17_502	T3
DDR3_D18	PS_DDR_DQ18_502	N3
DDR3_D19	PS_DDR_DQ19_502	T1
DDR3_D20	PS_DDR_DQ20_502	R3
DDR3_D21	PS_DDR_DQ21_502	T2
DDR3_D22	PS_DDR_DQ22_502	M2
DDR3_D23	PS_DDR_DQ23_502	R1
DDR3_D24	PS_DDR_DQ24_502	AA3
DDR3_D25	PS_DDR_DQ25_502	U1
DDR3_D26	PS_DDR_DQ26_502	AA1
DDR3_D27	PS_DDR_DQ27_502	U2
DDR3_D28	PS_DDR_DQ28_502	W1
DDR3_D29	PS_DDR_DQ29_502	Y3
DDR3_D30	PS_DDR_DQ30_502	W3
DDR3_D31	PS_DDR_DQ31_502	Y1
DDR3_DM0	PS_DDR_DM0_502	B1
DDR3_DM1	PS_DDR_DM1_502	H3
DDR3_DM2	PS_DDR_DM2_502	P1
DDR3_DM3	PS_DDR_DM3_502	AA2
DDR3_A0	PS_DDR_A0_502	M4
DDR3_A1	PS_DDR_A1_502	M5
DDR3_A2	PS_DDR_A2_502	K4
DDR3_A3	PS_DDR_A3_502	L4
DDR3_A4	PS_DDR_A4_502	K6
DDR3_A5	PS_DDR_A5_502	K5
DDR3_A6	PS_DDR_A6_502	J7
DDR3_A7	PS_DDR_A7_502	J6
DDR3_A8	PS_DDR_A8_502	J5

DDR3_A9	PS_DDR_A9_502	H5
DDR3_A10	PS_DDR_A10_502	J3
DDR3_A11	PS_DDR_A11_502	G5
DDR3_A12	PS_DDR_A12_502	H4
DDR3_A13	PS_DDR_A13_502	F4
DDR3_A14	PS_DDR_A14_502	G4
DDR3_BA0	PS_DDR_BA0_502	L7
DDR3_BA1	PS_DDR_BA1_502	L6
DDR3_BA2	PS_DDR_BA2_502	M6
DDR3_S0	PS_DDR_CS_B_502	P6
DDR3_RAS	PS_DDR_RAS_B_502	R5
DDR3_CAS	PS_DDR_CAS_B_502	P3
DDR3_WE	PS_DDR_WE_B_502	R4
DDR3_ODT	PS_DDR_ODT_502	P5
DDR3_RESET	PS_DDR_DRST_B_502	F3
DDR3_CLK0_P	PS_DDR_CKP_502	N4
DDR3_CLK0_N	PS_DDR_CKN_502	N5
DDR3_CKE	PS_DDR_CKE_502	V3

Table 2-3-2: DDR3 DRAM Pin Assignment

2.4 QSPI Flash

The core board is equipped with a 256MBit Quad-SPI FLASH chip, model W25Q256FVEI, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 2-4-1.

Position	Model	Capacity	Factory
U7	W25Q256FVEI	32M Byte	Winbond

Table 2-4-1: QSPI FLASH Specification

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 2-4-1 shows the QSPI Flash in the schematic.

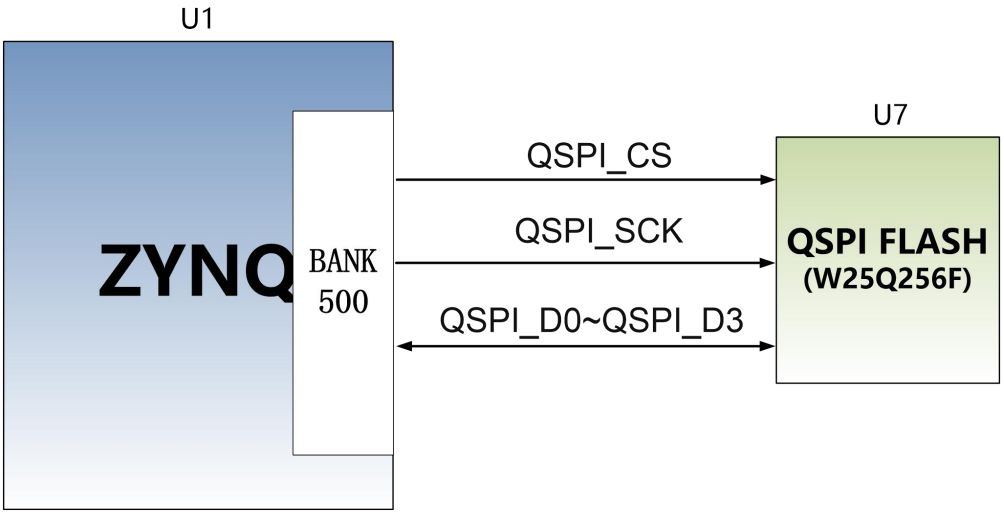


Figure 2-4-1: QSPI Flash in the schematic

Figure 2-4-2: QSPI Flash on the Core Board

Pin Assignment of QSPI Flash

Signal Name	ZYNQ Pin Name	Pin Number
QSPI_SCK	PS_MIO6_500	A4
QSPI_CS	PS_MIO1_500	A1
QSPI_D0	PS_MIO2_500	A2
QSPI_D1	PS_MIO3_500	F6
QSPI_D2	PS_MIO4_500	E4
QSPI_D3	PS_MIO5_500	A3

Table 2-4-2: Pin Assignment of QSPI FLASH

2.5 eMMC Flash

The core board is equipped with a large capacity 32GB eMMC FLASH chip, model THGBMFG8C2LBAIL, which supports the JEDEC e-MMC V5.0 standard HS-MMC interface with level support of 1.8V or 3.3V. The data width of the eMMC FLASH and ZYNQ connections is 4 bits. Due to the large capacity and

non-volatile nature of eMMC FLASH, it can be used as a large-capacity storage device for the ZYNQ system, such as ARM-based applications, system files, and other user data files. The specific models and related parameters of eMMC FLASH are shown in Table 2-5-1：

Position	Model	Capacity	Factory
U33	THGBMFG8C2LBAIL	32G Byte	TOSHIBA

Table 2-5-1: eMMC FLASH Specification

eMMC FLASH is connected to the GPIO port of the BANK501 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the SD interface. Figure 2-5-1 shows the eMMC Flash in the schematic.

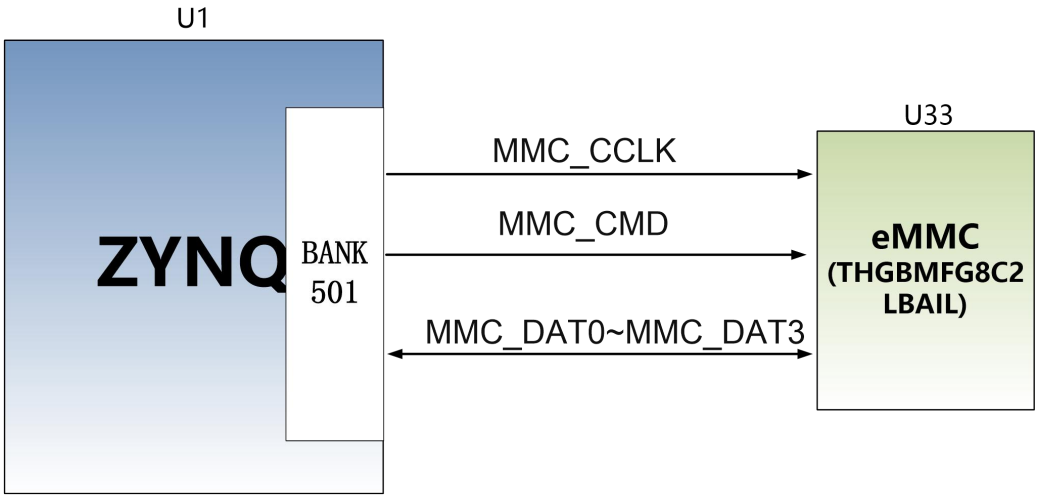


Figure 2-5-1: eMMC Flash in the Schematic

Figure 2-5-2: eMMC Flash on the Core Board

Pin Assignment of eMMC Flash

Signal Name	ZYNQ Pin Name	Pin Number
MMC_CCLK	PS_MIO48_501	D11
MMC_CMD	PS_MIO47_501	B10
MMC_D0	PS_MIO46_501	D12
MMC_D1	PS_MIO49_501	C14
MMC_D2	PS_MIO50_501	D13
MMC_D3	PS_MIO51_501	C10

Table 2-5-2: Pin Assignment of eMMC FLASH

2.6 Clock configuration

The AC7021 core board provides active clocks for the PS system and the PL logic sections, respectively, so that the PS system and the PL logic can work independently.

PS system clock source

The ZYNQ chip provides a 33.333 MHz clock input to the PS section through the X1 crystal on the development board. The input of the clock is connected to the pins of PS_CLK_500 of the BANK500 of the ZYNQ chip. The schematic diagram is shown in Figure 2-6-1:

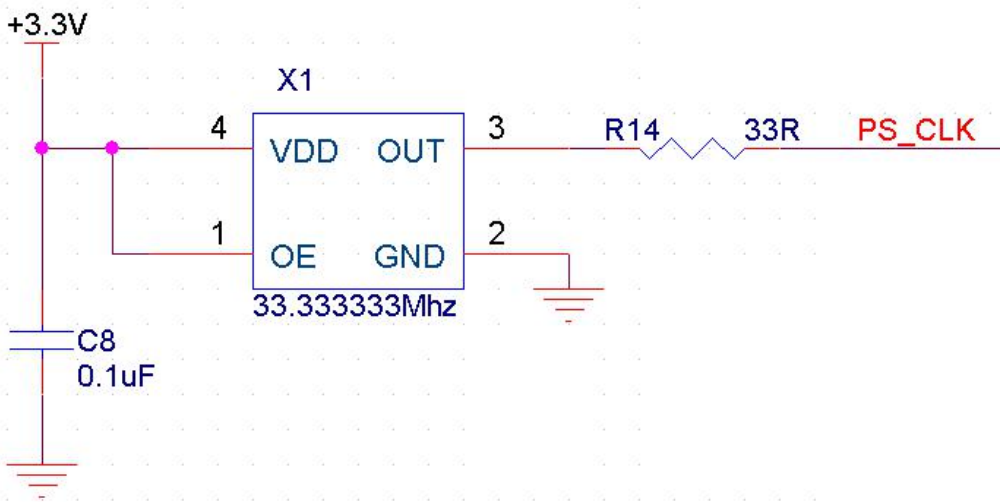


Figure 2-6-1: Active crystal oscillator to the PS section

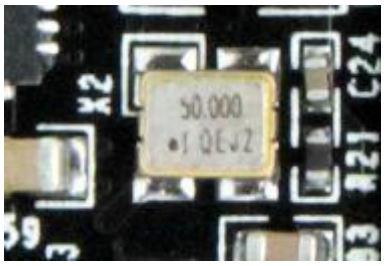


Figure 2-6-2: 33.333Mhz active Crystal Oscillator on the Core Board

PS Clock pin assignment:

Signal Name	Pin
PS_CLK_500	F7

Table 2-6-1: PS Clock pin assignment

PL system clock source

The AC7021 core board provides a single-ended 50MHz PL system clock source with 3.3V power supply. The crystal output is connected to the global clock (MRCC) of the FPGA BANK13, which can be used to drive user logic within the FPGA. The schematic diagram of the clock source is shown in Figure 2-6-3:

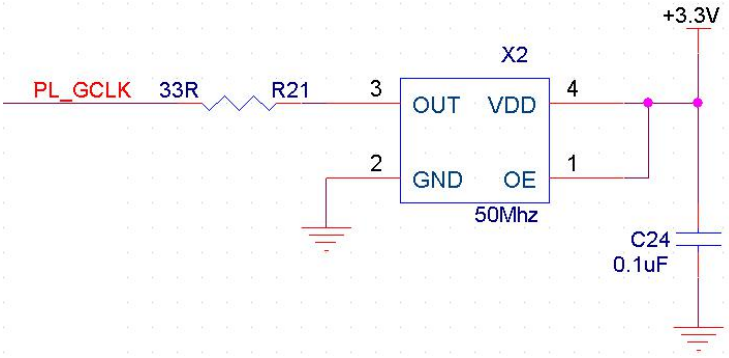


Figure 2-6-3: PL system clock source

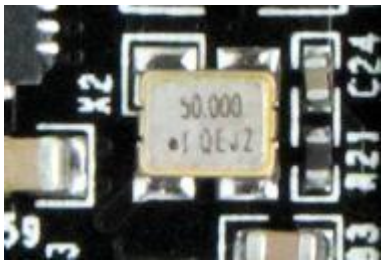


Figure 2-6-4: 50Mhz active crystal oscillator on the Core Board

PL Clock pin assignment:

Signal Name	Pin
PL_GCLK	Y9

Table 2-6-2: PL Clock pin assignment

2.7 USB to serial port

For the AC7021 core board to work and debug separately, we have a Uart to USB interface for the core board. Used for separate power supply and debugging of the core board. The conversion chip uses the USB-UART chip of Silicon Labs CP2102GM. The USB interface uses the MINI USB interface. It

can be connected to the USB port of the upper PC with a USB cable for separate power supply and serial data communication of the core board.

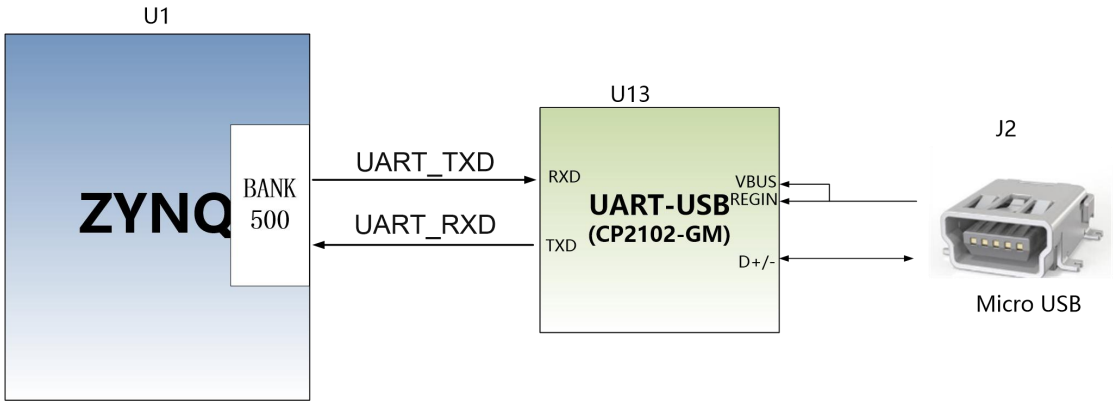


Figure 2-7-1: USB to Serial Port

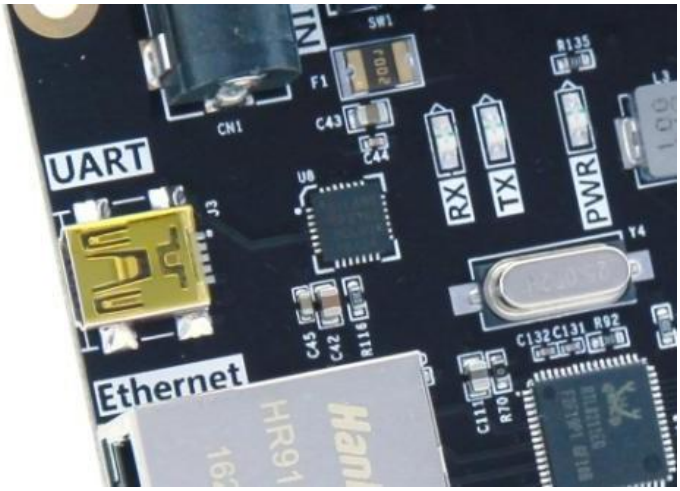


Figure 2-7-2: USB to Serial Port on the Core Board

At the same time, two LED indicators are set on the serial port signal, and the LEDs on the PCB are printed as RX and TX LEDs (D5 and D6). The RX and TX LEDs indicate whether the serial port has data received or sent, as shown in the Figure 2-7-3 below.

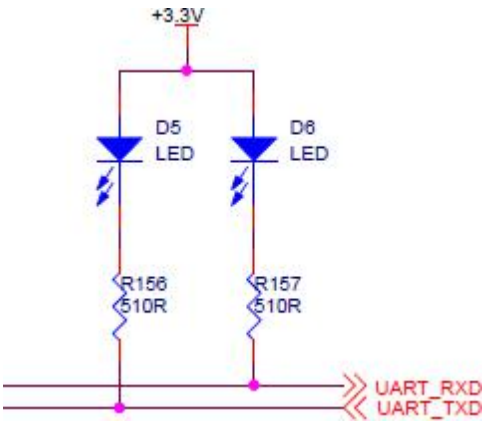


Figure 2-7-3: USB to serial port signal indicator

Uart Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
UART_RXD	PS_MIO14_500	B6	Uart data output
UART_TXD	PS_MIO15_500	E6	Uart data input

Table 2-7-1: Uart Pin Assignment

2.8 LED

There are 6 red LED lights on the AC7021 core board, one of which is the power indicator light (PWR), one is the configuration LED light (DONE), two are the user LED lights (LED1~LED2), and the other two are the UART transmit and receive indicators (TX, RX). When the core board is powered, the power indicator will illuminate; when the FPGA is configured, the configuration LED will illuminate. Two user LED lights are connected to the MIO of the PS, one is connected to the IO of the PL, the user can control the lighting and off by the program, when the IO voltage connected to the user LED light is high, the user LED light is off. When the connection IO voltage is low, the user LED will be illuminated. The schematic diagram of the LED light hardware connection is shown in Figure 2-8-1:

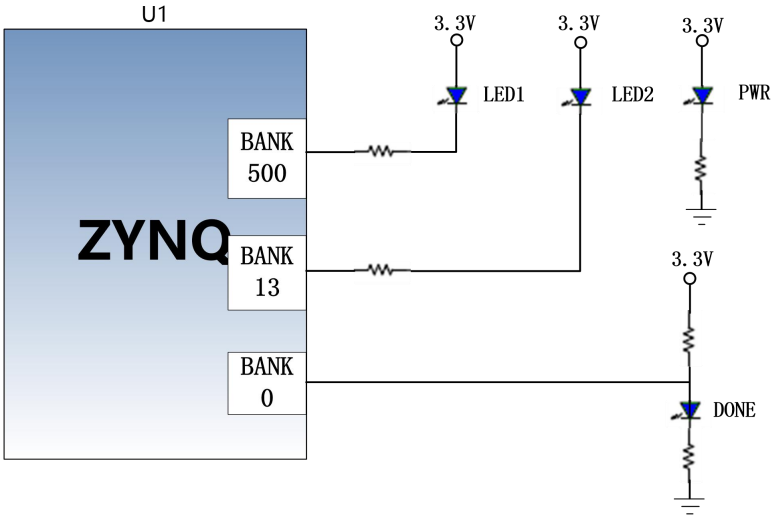


Figure 2-8-1: The schematic diagram of the LED light hardware connection

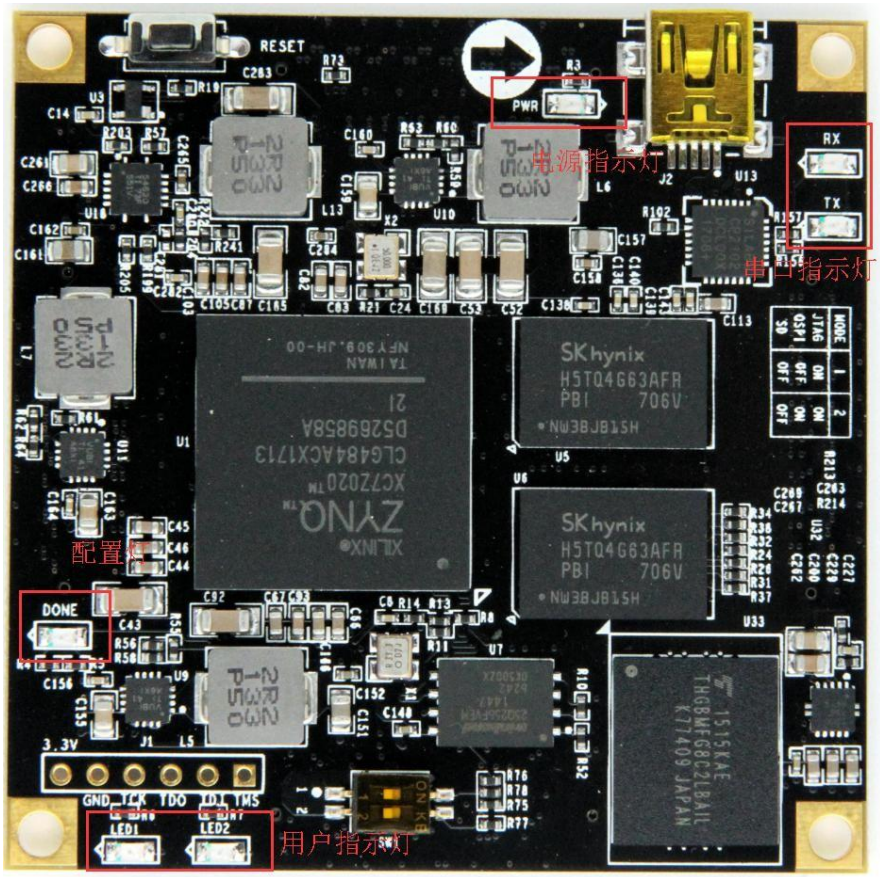


Figure 2-8-2: The LEDs on the Core Board

LED Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
MIO0_LED	PS_MIO0_500	G6	User LED1
PL_LED	IO_0_13	R7	User LED2

Table 2-8-1: LED Pin Assignment

2.9 Reset button

The AC7021 has a reset button RESET and circuitry on the core board. The reset signal is connected to the PS reset pin of the ZYNQ chip. The reset button can be used by the user to reset the ZYNQ system. When the reset button is pressed, the reset chip will generate a low level reset signal to the ZYNQ chip. The schematic diagram of the reset button and reset chip connection is shown in Figure 2-9-1:

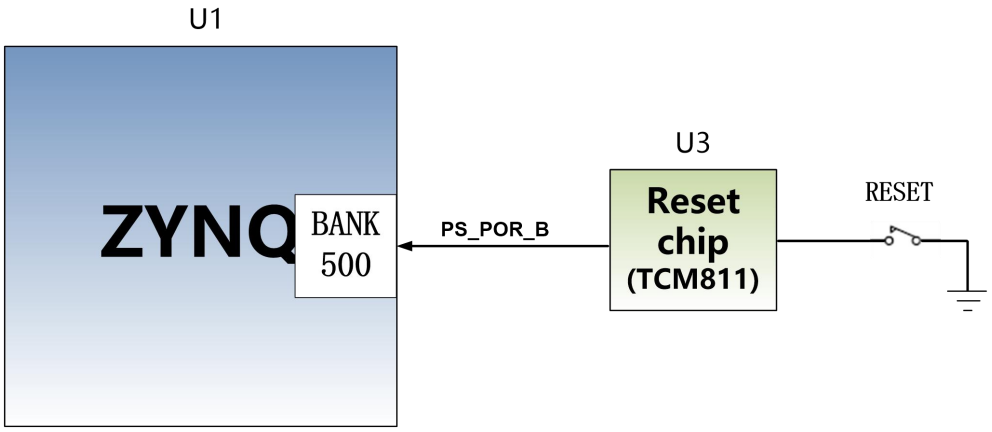


Figure 2-9-1: Reset button connection diagram

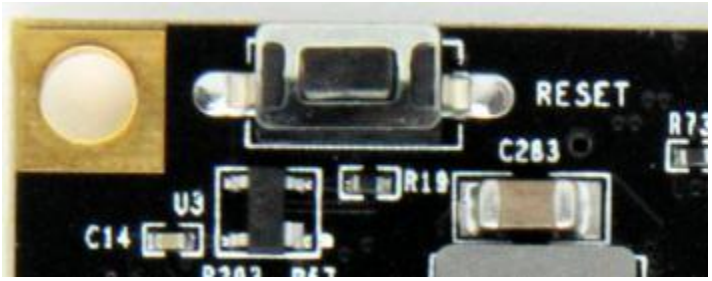


Figure 2-9-2: Reset Button on the Core Board

Reset Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PS_POR_B	PS_POR_B_500	B5	Reset Key

Table 2-9-1: Reset Pin Assignment

2.10 JTAGE Interface

The JTAG test socket J1 is reserved on the AC7021 core board for separate JTAG download and debugging of the core board. Figure 2-10-1 is the schematic part of the JTAG port, which involves TMS, TDI, TDO, TCK, GND. , +3.3V these six signals.

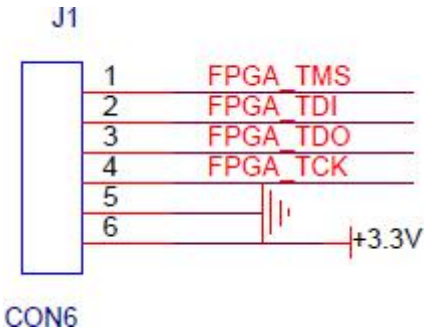


Figure 2-10-1: JTAG interface part of the core board schematic

The JTAG interface J1 on the core board uses a 6-pin 2.54mm pitch single-row test hole. If you need to use the JTAG connection to debug on the core board, you need to solder a 6-pin single-row pin header. Figure 2-10-2 shows the physical map of the JTAG interface on the development board.

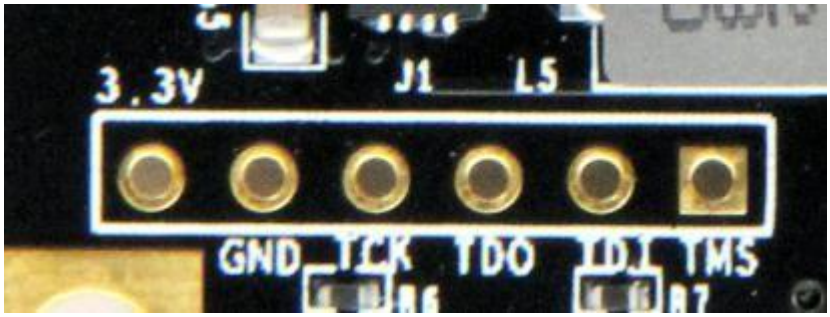


Figure 2-10-2: JTAG interface on the core board

2.11 DIP switch configuration

The AC7021 has a 2-digit DIP switch SW1 on the core board to configure the ZYNQ system's startup mode. The AC7021 system development platform supports three startup modes. The three startup modes are JTAG debug mode, QSPI FLASH and SD card boot mode. After the XC7Z020 chip is powered up, it will detect the level of the MIO port (MIO5 and MIO4) to determine which startup mode. Users can select different startup modes through the DIP switch SW1 on the core board. The SW1 startup mode configuration is shown in Table 2-11-1

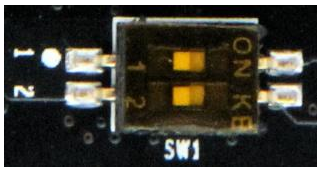
SW1	Position（1，2）	MIO5,MIO4 Level	Startup mode
	ON、ON	0、0	JTAG
	OFF、OFF	1、1	SD Card
	OFF、ON	1、0	QSPI FLASH

Table 2-11-1: The SW1 Startup Mode Configuration

2.12 Power

The AC7021 core board is powered by DC5V. It is powered by the Mini USB interface when it is used alone. It is powered by the extension board when the backplane is connected. Please be careful not to supply power to the Mini

USB and the extension board at the same time to avoid damage. The power supply design on the core board is shown in Figure 2-12-1.

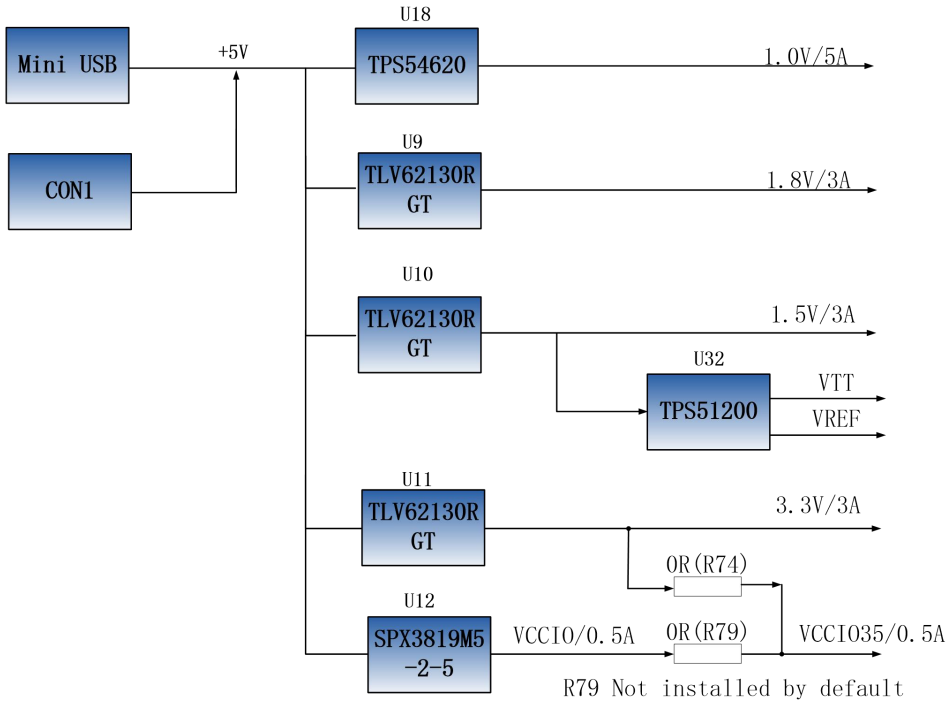


Figure 2-12-1: The Power Supply Design on the Core Board

The development board is powered by +5V, and is converted into +1.0V, +1.8V, +1.5V, +3.3V four-way power supply through four-way DC/DC power supply core TPS54620TLV62130RGT. The output current of +1.0V can be as high as 5A, and the other three output current are 3A. The VCCIO 2.5V power supply is generated by one LDO SPX3819M5-2-5. The VCCIO 2.5V power supply is mainly reserved for the BANK power supply of the BANK33 of the FPGA. The user can select the power supply of BANK33 and BANK34 through two 0 ohm resistors (R74, R79). By default, the R74 on the development board is installed, and the resistor of R79 is not installed, so the power supply of BANK33 and BANK34 is +3.3V. The user can replace the resistor so that the IO of the BANK33, 34 outputs a voltage standard of 2.5V. 1.5V generates the VTT and VREF voltages required by DDR3 through TI's TPS51200. The functions of each power distribution are shown in the following Table 2-12-1:

Power	Function
+1.0V	ZYNQ PS and PL section core voltage
+1.8V	ZYNQ PS and PL partial auxiliary voltage, BANK501 IO voltage, eMMC
+3.3V	ZCNQ Bank0, Bank500, Bank13, Bank35, VCCIO,QSIP FLASH, Clock Crystal
+1.5V	DDR3, ZYNQ Bank501
VREF,VTT（+0.75V	DDR3
VCCIO(+2.5V)	Reserved for ZYNQ Bank33,Bank 34

Table 2-12-1: The Functions of Each Power Distribution

Because the power supply of ZYNQ FPGA has the power-on sequence requirement, in the circuit design, we have designed according to the power requirements of the chip, and the power-on is +1.0V->+1.8V->(+1.5 V, +3.3V, VCCIO). The circuit design ensures the normal operation of the chip. The power supply on the core board detailed as Figure 2-12-2 below

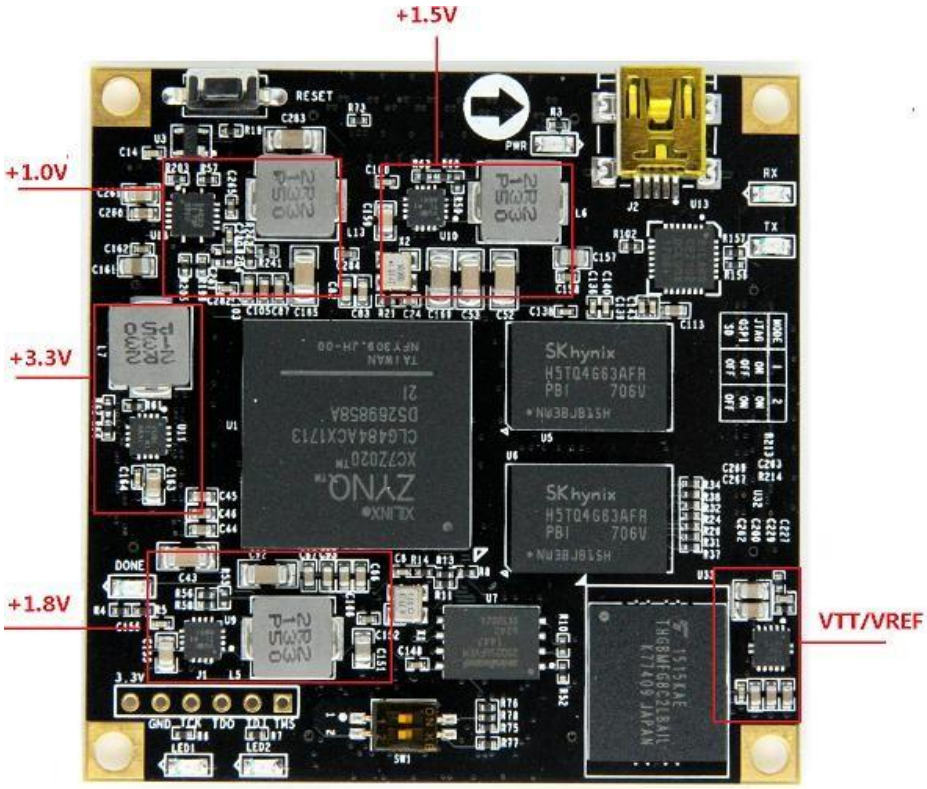


Figure 2-12-2: The Power Supply on the Core Board

2.13 Structure diagram

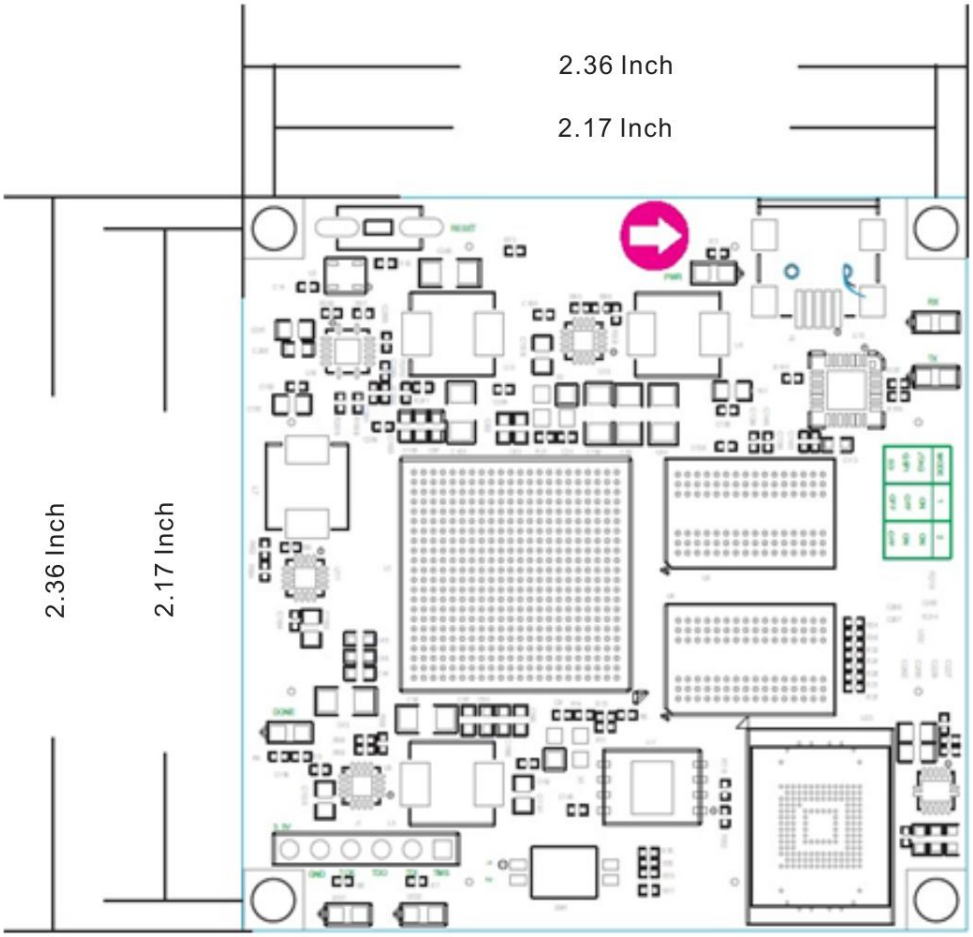


Figure 2-13-1: The Structure diagram （Top View）

2.14 Connector pin definition

The core board expands four high-speed carrier ports, and uses four 80Pin inter-board connectors (CON1~CON4) to connect with the backplane. The PIN pitch of the connector is 0.5mm. Among them, CON1 is connected to the power input, the MIO signal of the PS and the JTAG signal, and CON2~CON4 are connected to the IO signals of BANK13, BANK33, BANK34, BANK35 of PL. The IO levels of BANK33 and BANK34 can be changed by changing the level of the LDO chip (U12) on the board. The default is 3.3V. Pin assignment detailed as Table 2-14-1, Table 2-14-2, Table 2-14-3, Table 2-14-4:

CON1 Pin	Signal Name	ZYNQ Pin	CON1 Pin	Signal Name	ZYNQ Pin
1	+5V	-	2	+5V	-
3	+5V	-	4	+5V	-
5	+5V	-	6	+5V	-
7	+5V	-	8	+5V	-
9	GND	-	10	GND	-
11	PS_MIO13	A6	12	ETH_TXD0	E9
13	PS_MIO12	C5	14	ETH_TXD1	A7
15	-	-	16	ETH_TXD2	E10
17	-	-	18	ETH_TXD3	A8
19	GND	-	20	GND	-
21	-	-	22	ETH_TXCK	D6
23	-	-	24	ETH_TXCTL	F11
25	-	-	26	ETH_RXD3	A13
27	-	-	28	ETH_RXD2	F12
29	GND	-	30	GND	-
31	PS_MIO7	D5	32	ETH_RXD1	B7
33	PS_MIO8	E5	34	ETH_RXD0	E11
35	PS_MIO9	C4	36	ETH_RXCTL	D7
37	PS_MIO11	B4	38	ETH_RXCK	A14
39	GND	-	40	GND	-
41	-	-	42	ETH_MDC	D10
43	-	-	44	ETH_MDIO	C12
45	-	-	46	OTG_STP	A11
47	-	-	48	OTG_DIR	E8
49	GND	-	50	GND	-
51	XADC_VP	L11	52	OTG_CLK	A9
53	XADC_VN	M12	54	OTG_NXT	F9
55	-	-	56	OTG_DATA0	C7
57	PS_MIO10	G7	58	OTG_DATA1	G13
59	GND	-	60	GND	-
61	SD_CLK	E14	62	OTG_DATA2	B12

63	SD_D1	B11	64	OTG_DATA3	F14
65	SD_D0	D8	66	OTG_DATA4	A12
67	SD_CMD	C8	68	OTG_DATA5	B14
69	GND	-	70	GND	-
71	SD_D3	B9	72	OTG_DATA6	F13
73	SD_D2	E13	74	OTG_DATA7	C13
75	-	-	76	-	-
77	FPGA_TMS	G12	78	FPGA_TCK	G11
79	FPGA_TDO	G14	80	FPGA_TDI	H13

Table 2-14-1: Pin Assignment of CON1

CON2 Pin	Singal Name	ZYNQ Pin	CON2 Pin	Singal Name	ZYNQ Pin
1	B13_L1_N	V9	2	B33_L4_N	W21
3	B13_L1_P	V10	4	B33_L4_P	W20
5	B33_L10_P	AB19	6	B33_L3_N	W22
7	B33_L10_N	AB20	8	B33_L3_P	V22
9	GND	-	10	GND	-
11	B13_L4_N	W12	12	B33_L2_N	U22
13	B13_L4_P	V12	14	B33_L2_P	T22
15	B34_L6_N	M16	16	B13_L5_N	U11
17	B34_L6_P	M15	18	B13_L5_P	U12
19	GND	-	20	GND	-
21	B13_L12_N	Y8	22	B33_IO25	U14
23	B13_IO25	U7	24	B34_IO25	R15
25	B13_L23_N	W7	26	B13_L6_P	U10
27	B13_L23_P	V7	28	B13_L6_N	U9
29	GND	-	30	GND	-
31	B13_L13_N	Y5	32	B13_L19_N	T6
33	B13_L13_P	Y6	34	B13_L19_P	R6
35	B13_L24_N	W5	36	B13_L22_P	U6
37	B13_L24_P	W6	38	B13_L22_N	U5

39	GND	-	40	GND	-
41	B33_L11_P	Y19	42	B13_L20_P	T4
43	B33_L11_N	AA19	44	B13_L20_N	U4
45	B33_L5_P	U20	46	B13_L3_P	W11
47	B33_L5_N	V20	48	B13_L3_N	W10
49	GND	-	50	GND	-
51	B33_L1_P	T21	52	B13_L10_P	Y11
53	B33_L1_N	U21	54	B13_L10_N	Y10
55	B13_L7_P	AA12	56	B13_L2_P	V8
57	B13_L7_N	AB12	58	B13_L2_N	W8
59	GND	-	60	GND	-
61	B13_L8_N	AB11	62	B13_L14_P	AA7
63	B13_L8_P	AA11	64	B13_L14_N	AA6
65	B13_L9_N	AB9	66	B13_L16_P	AB5
67	B13_L9_P	AB10	68	B13_L16_N	AB4
69	GND	-	70	GND	-
71	B13_L11_N	AA8	72	B13_L18_N	AA4
73	B13_L11_P	AA9	74	B13_L18_P	Y4
75	B13_L17_N	AB6	76	B13_L15_N	AB1
77	B13_L17_P	AB7	78	B13_L15_P	AB2
79	B13_L21_N	V4	80	B13_L21_P	V5

Table 2-14-2: Pin Assignment of CON2

CON3 Pin	Signal Name	ZYNQ Pin	CON3 Pin	Signal Name	ZYNQ Pin
1	B34_L2_P	J16	2	B34_L12_N	L19
3	B34_L2_N	J17	4	B34_L12_P	L18
5	B34_L11_P	K19	6	B34_L10_N	L22
7	B34_L11_N	K20	8	B34_L10_P	L21
9	GND	-	10	GND	-
11	B34_L7_P	J18	12	B34_L3_N	L16
13	B34_L7_N	K18	14	B34_L3_P	K16

15	B34_L1_P	J15	16	B34_L15_N	M22
17	B34_L1_N	K15	18	B34_L15_P	M21
19	GND	-	20	GND	-
21	B34_L17_P	R20	22	B34_L16_P	N22
23	B34_L17_N	R21	24	B34_L16_N	P22
25	B34_L14_N	N20	26	B34_L20_N	P18
27	B34_L14_P	N19	28	B34_L20_P	P17
29	GND	-	30	GND	-
31	B34_L5_N	N18	32	B34_L13_P	M19
33	B34_L5_P	N17	34	B34_L13_N	M20
35	B33_L9_P	Y20	36	B34_L21_N	T17
37	B33_L9_N	Y21	38	B34_L21_P	T16
39	GND	-	40	GND	-
41	B33_L8_P	AA21	42	B33_L6_N	V19
43	B33_L8_N	AB21	44	B33_L6_P	V18
45	B33_L12_N	AA18	46	B33_L16_P	U17
47	B33_L12_P	Y18	48	B33_L16_N	V17
49	GND	-	50	GND	-
51	B33_L13_P	W17	52	B33_L17_N	AB17
53	B33_L13_N	W18	54	B33_L17_P	AA17
55	B33_L18_N	AB16	56	B33_L7_P	AA22
57	B33_L18_P	AA16	58	B33_L7_N	AB22
59	GND	-	60	GND	-
61	B33_L21_N	Y15	62	B33_L19_N	V15
63	B33_L21_P	W15	64	B33_L19_P	V14
65	B33_L24_P	AB14	66	B33_L15_N	U16
67	B33_L24_N	AB15	68	B33_L15_P	U15
69	GND	-	70	GND	-
71	B33_L23_N	AA13	72	B33_L14_P	W16
73	B33_L23_P	Y13	74	B33_L14_N	Y16
75	B33_L20_N	W13	76	B33_L22_P	Y14
77	B33_L20_P	V13	78	B33_L22_N	AA14

79	B34_IO0	H15	80	B33_IO0	U19

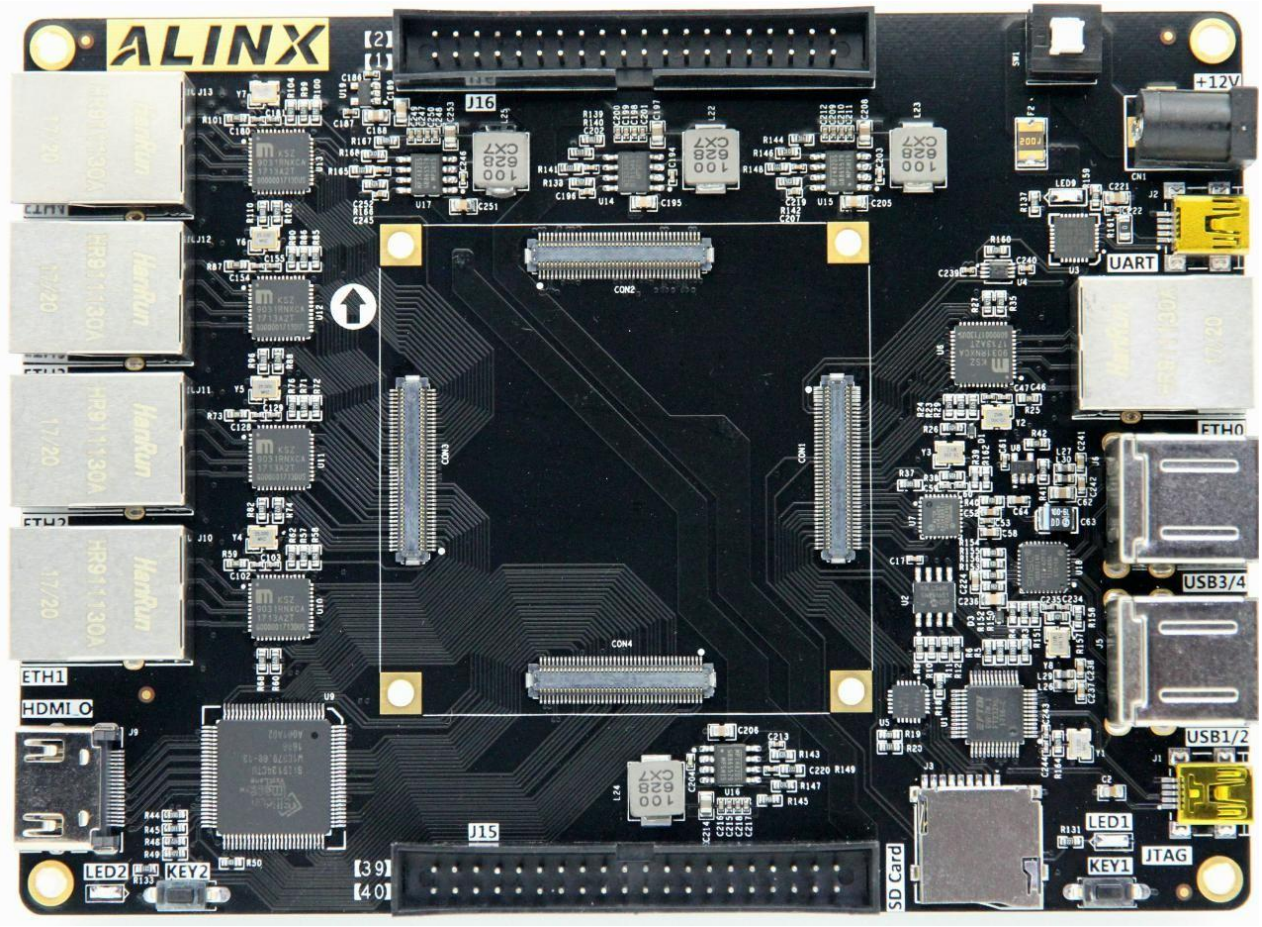
Table 2-14-3: Pin Assignment of CON3

CON4 Pin	Signal Name	ZYNQ Pin	CON4 Pin	Signal Name	ZYNQ Pin
1	B35_L7_N	B15	2	B35_L9_P	A16
3	B35_L7_P	C15	4	B35_L9_N	A17
5	B35_L8_P	B16	6	B35_L10_P	A18
7	B35_L8_N	B17	8	B35_L10_N	A19
9	GND	-	10	GND	-
11	B35_L11_N	C18	12	B35_L15_P	A21
13	B35_L11_P	C17	14	B35_L15_N	A22
15	B35_L13_N	B20	16	B35_L18_N	B22
17	B35_L13_P	B19	18	B35_L18_P	B21
19	GND	-	20	GND	-
21	B35_L14_N	C20	22	B35_L16_N	C22
23	B35_L14_P	D20	24	B35_L16_P	D22
25	B35_L12_P	D18	26	B35_L17_N	D21
27	B35_L12_N	C19	28	B35_L17_P	E21
29	GND	-	30	GND	-
31	B35_L2_N	D17	32	B35_L23_N	F22
33	B35_L2_P	D16	34	B35_L23_P	F21
35	B35_L1_N	E16	36	B35_L22_N	G21
37	B35_L1_P	F16	38	B35_L22_P	G20
39	GND	-	40	GND	-
41	B35_L21_P	E19	42	B34_L8_N	J22
43	B35_L21_N	F19	44	B34_L8_P	J21
45	B35_L24_P	H22	46	B35_L20_N	F19
47	B35_L24_N	G22	48	B35_L20_P	G19
49	GND	-	50	GND	-
51	B35_L6_P	G17	52	B35_L19_N	H20
53	B35_L6_N	F17	54	B35_L19_P	H19
55	B35_L4_P	G15	56	B34_L9_P	J20

57	B35_L4_N	G16	58	B34_L9_N	K21
59	GND	-	60	GND	-
61	B35_L3_N	D15	62	B35_IO25	H18
63	B35_L3_P	E15	64	B35_IO0	H17
65	B34_L24_N	R16	66	B34_L4_P	L17
67	B34_L24_P	P16	68	B34_L4_N	M17
69	GND	-	70	GND	-
71	B34_L23_P	R18	72	B34_L18_N	P21
73	B34_L23_N	T18	74	B34_L18_P	P20
75	B35_L5_P	F18	76	B34_L22_P	R19
77	B35_L5_N	E18	78	B34_L22_N	T19
79	B34_L19_P	N15	80	B34_L19_N	P15

Table 2-14-4: Pin Assignment of CON4

Part 3: Carrier Board



3.1 Carrier Board Introduction

Through the previous function introduction, we can understand the function of the carrier board.

- 5 ports 10/100M/1000M Ethernet RJ-45 interface
- 1 port HDMI output display interface
- 4 ports USB HOST interface
- 1 port USB Uart communication interface
- 1 port SD card interface
- 2 ports 40-pin carrier port
- JTAG debug interface
- 2 independent buttons
- 2 user LED lights

3.2 Gigabit Ethernet interface

The AX7021 has five Gigabit Ethernet interfaces on the carrier board, one of which is the connected PS system side. The Ethernet interface is connected to the logical IO port of the PL. The 4-port Gigabit Ethernet interface connected to the PL side needs to be mounted to ZYNQ's AXI bus system by call IP program.

The Ethernet chip uses Micrel's KSZ9031RNX Ethernet PHY chip to provide network communication services to users. The Ethernet PHY chip on the PS side is connected to the GPIO interface of the PSNK501 of the PS side of ZYNQ. The Ethernet PHY chip on the PL side is connected to the IO of BANK33 and BANK34. The KSZ9031RNX chip supports 10/100/1000 Mbps network transmission rate and data communication with the MAC layer of the Zynq7000 system through the RGMII interface. KSZ9031RNX supports MDI/MDX adaptation, various speed adaptive, Master/Slave adaptation, MDIO bus for PHY register management.

After power-on, the KSZ9031RNX detects the level status of some specific IOs to determine their working mode. Table 3-2-1 describes the default settings after the GPHY chip is powered on.

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address 011
CLK125_EN	Enable 125Mhz clock output selection	Enable
LED_MODE	LED light mode configuration	Single LED light mode
MODE0~MODE3	Link adaptation and full duplex configuration	10/100/1000 adaptive, compatible with full-duplex, half-duplex

Table 3-2-1: Default setting after power-on of the KS GPHY chip

When the network is connected to Gigabit Ethernet, the data transmission of ZYNQ and PHY chip KSZ9031RNX is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising edge and falling samples of the clock.

When the network is connected to 100M Ethernet, the data transmission of

ZYNQ and PHY chip KSZ9031RNX is communicated through the RMII bus, and the transmission clock is 25Mhz. Data is sampled on the rising edge and falling samples of the clock. Figure 3-2-1 and Figure 3-2-2 detailed the connection of the ZYNQ chip end Ethernet PHY chip:

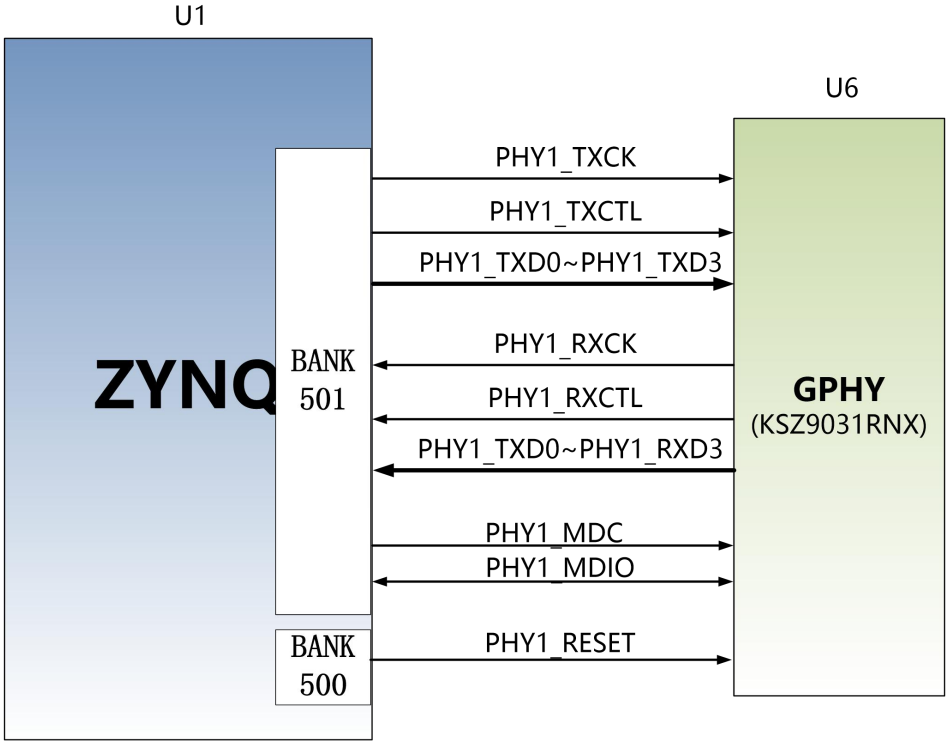


Figure 3-2-1: The connection of the ZYNQ PS end and PHY chip

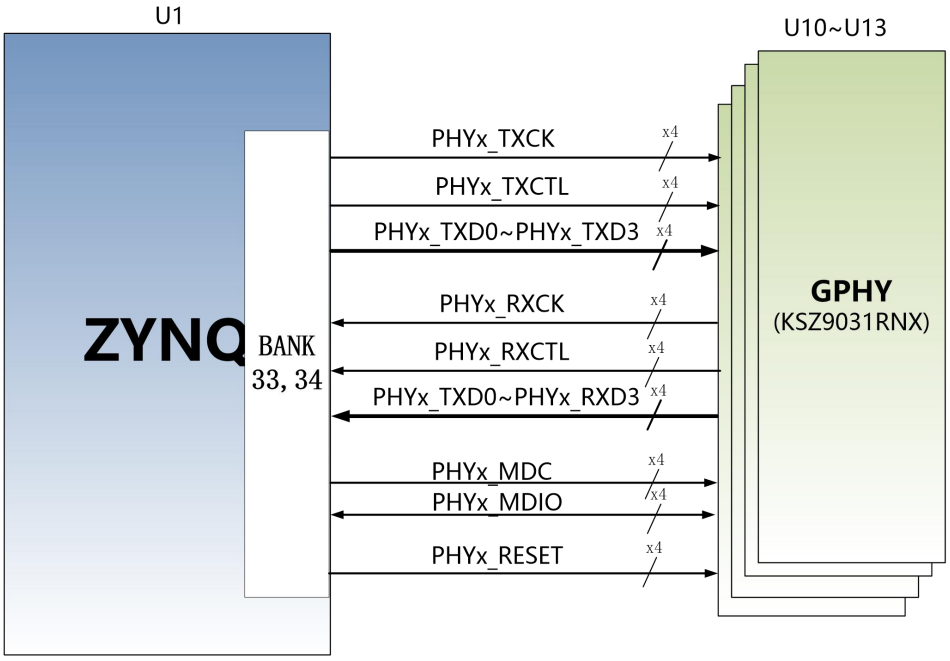


Figure 3-2-2: The connection of the 4 ZYNQ PL end and PHY chip

Figure 3-2-3: PS side Ethernet GPHY port on Carrier board

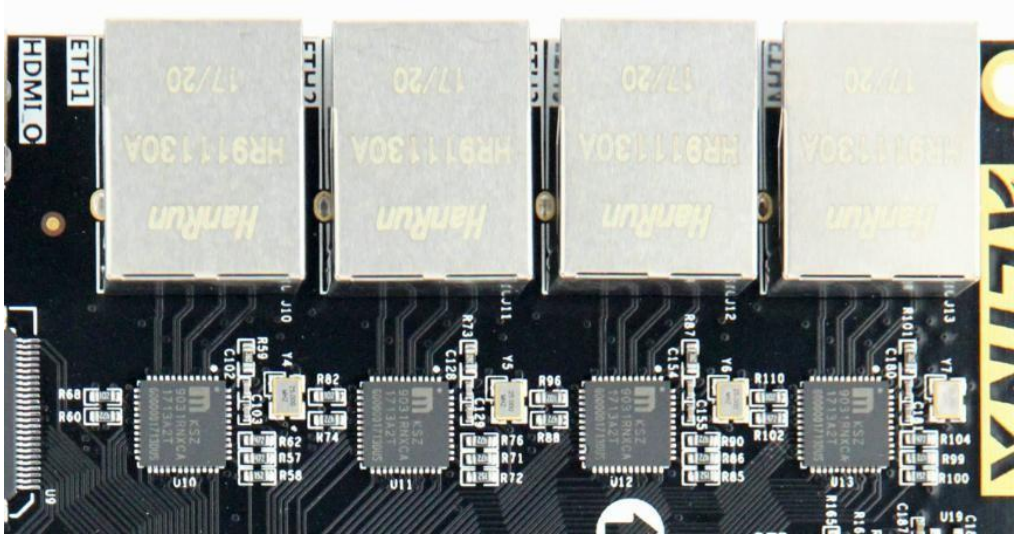


Figure 2-3-4: 4 PS side Ethernet GPHY port on the carrier port

ETH0(PS) Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PHY1_TXCK	PS_MIO16_501	D6	RGMII Transmit clock
PHY1_TXD0	PS_MIO17_501	E9	Transmit data bit 0
PHY1_TXD1	PS_MIO18_501	A7	Transmit data bit1
PHY1_TXD2	PS_MIO19_501	E10	Transmit data bit2
PHY1_TXD3	PS_MIO20_501	A8	Transmit data bit3
PHY1_TXCTL	PS_MIO21_501	F11	Transmit enable signal
PHY1_RXCK	PS_MIO22_501	A14	RGMII Receive clock
PHY1_RXD0	PS_MIO23_501	E11	Receive data Bit0
PHY1_RXD1	PS_MIO24_501	B7	Receive data Bit1
PHY1_RXD2	PS_MIO25_501	F12	Receive data Bit2
PHY1_RXD3	PS_MIO26_501	A13	Receive data Bit3
PHY1_RXCTL	PS_MIO27_501	D7	Receive data valid signal
PHY1_MDC	PS_MIO52_501	D10	MDIO Management clock
PHY1_MDIO	PS_MIO53_501	C12	MDIO Management clock

ETH1(PL) Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PHY2_TXCK	B34_L17_N	R21	RGMII Send clock
PHY2_TXD0	B34_L5_P	N17	Send data bit 0
PHY2_TXD1	B34_L5_N	N18	Send data bit1
PHY2_TXD2	B34_L14_P	N19	Send data bit2
PHY2_TXD3	B34_L14_N	N20	Send data bit3
PHY2_TXCTL	B34_L17_P	R20	Send enable signal
PHY2_RXCK	B34_L11_P	K19	RGMII Receive clock
PHY2_RXD0	B34_L7_P	J18	Receive data Bit0
PHY2_RXD1	B34_L7_N	K18	Receive data Bit1
PHY2_RXD2	B34_L1_P	J15	Receive data Bit2
PHY2_RXD3	B34_L1_N	K15	Receive data Bit3
PHY2_RXCTL	B34_L11_N	K20	Receive data valid signal
PHY2_MDC	B34_L2_N	J17	MDIO Management clock
PHY2_MDIO	B34_L2_P	J16	MDIO Management data

ETH2(PL) Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PHY3_TXCK	B34_L3_P	K16	RGMII Send clock
PHY3_TXD0	B34_L12_P	L18	Send data bit 0
PHY3_TXD1	B34_L10_N	L22	Send data bit1
PHY3_TXD2	B34_L10_P	L21	Send data bit2
PHY3_TXD3	B34_L3_N	L16	Send data bit3
PHY3_TXCTL	B34_L15_N	M22	Send enable signal
PHY3_RXCK	B34_L13_P	M19	RGMII Receive clock
PHY3_RXD0	B34_L20_N	P18	Receive data Bit0
PHY3_RXD1	B34_L16_N	P22	Receive data Bit1
PHY3_RXD2	B34_L16_P	N22	Receive data Bit2
PHY3_RXD3	B34_L15_P	M21	Receive data Bit3
PHY3_RXCTL	B34_L20_P	P17	Receive data valid signal
PHY3_MDC	B34_L13_N	M20	MDIO Management clock
PHY3_MDIO	B34_L21_N	T17	MDIO Management data

ETH3(PL) Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PHY4_TXCK	B33_L17_P	AA17	RGMII Send clock
PHY4_TXD0	B33_L6_P	V18	Send data bit 0
PHY4_TXD1	B33_L16_P	U17	Send data bit1
PHY4_TXD2	B33_L16_N	V17	Send data bit2
PHY4_TXD3	B33_L17_N	AB17	Send data bit3
PHY4_TXCTL	B33_L7_P	AA22	Send enable signal
PHY4_RXCK	B33_L14_P	W16	RGMII Receive clock
PHY4_RXD0	B33_L15_N	U16	Receive data Bit0
PHY4_RXD1	B33_L19_P	V14	Receive data Bit1
PHY4_RXD2	B33_L19_N	V15	Receive data Bit2
PHY4_RXD3	B33_L7_N	AB22	Receive data Bit3
PHY4_RXCTL	B33_L15_P	U15	Receive data valid signal
PHY4_MDC	B33_L14_N	Y16	MDIO Management clock
PHY4_MDIO	B33_L22_P	Y14	MDIO Management data

ETH4(PL) Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PHY5_TXCK	B33_L24_N	AB15	RGMII Send clock
PHY5_TXD0	B33_L20_P	V13	Send data bit 0
PHY5_TXD1	B33_L20_N	W13	Send data bit1
PHY5_TXD2	B33_L23_P	Y13	Send data bit2
PHY5_TXD3	B33_L23_N	AA13	Send data bit3
PHY5_TXCTL	B33_L24_P	AB14	Send enable signal
PHY5_RXCK	B33_L13_P	W17	RGMII Receive clock
PHY5_RXD0	B33_L18_N	AB16	Receive data Bit0
PHY5_RXD1	B33_L18_P	AA16	Receive data Bit1
PHY5_RXD2	B33_L21_N	Y15	Receive data Bit2
PHY5_RXD3	B33_L21_P	W15	Receive data Bit3
PHY5_RXCTL	B33_L13_N	W18	Receive data valid signal
PHY5_MDC	B33_L12_P	Y18	MDIO Management clock
PHY5_MDIO	B33_L12_N	AA18	MDIO Management data

3.3 USB2.0 Host interface

There are 4 USB2.0 HOST interfaces on the AX7021 carrier board. The USB2.0 transceiver uses a 1.8V, high-speed USB3320C-EZK chip that supports the ULPI standard interface, and then expands the 4-port USB HOST interface through a USB HUB chip USB2514. ZYNQ's USB bus interface is connected to the USB3320C-EZK transceiver to achieve high-speed USB2.0 Host mode data communication. The USB3320C's USB data and control signals are connected to the IO port of the BANK501 on the PS side of the ZYNQ chip. The USB interface differential signal (DP/DM) is connected to the USB2514 chip to extend the four USB ports. Two 24MHz crystal oscillators provide system clocks for the USB3320C and USB2514 chips, respectively.

The USB interface is a flat USB interface (USB Type A), which allows users to connect different USB Slave peripherals (such as USB mouse and USB keyboard) at the same time. The carrier board also provides +5V power to each USB interface

The schematic diagram of the ZYNQ processor, USB3320C-EZK chip, USB2514 chip connection is shown as Figure 3-3-1

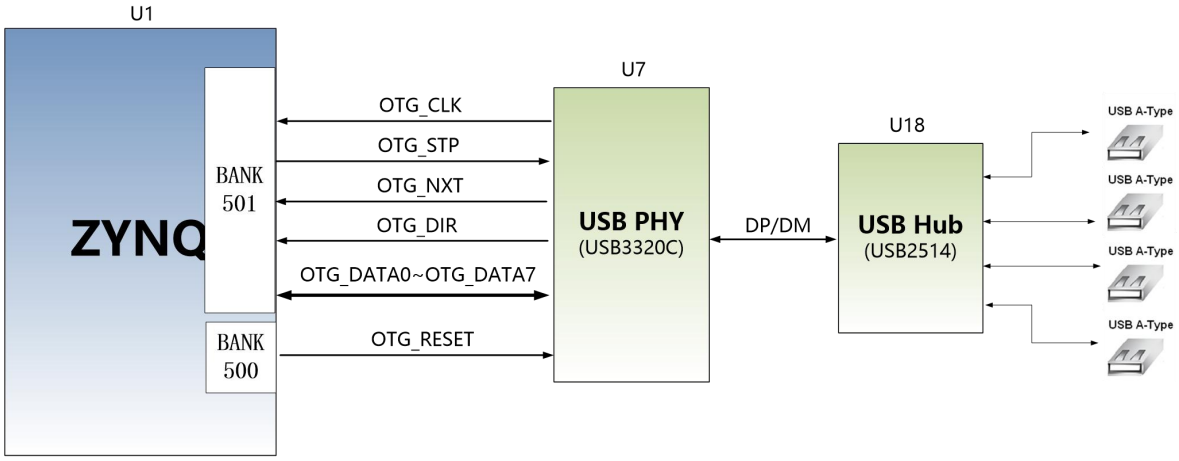


Figure 3-3-1: The connection between Zynq7000 and USB chip

Figure 3-3-2 shows the physical picture of the USB2.0 chip and interface, where the USB interface uses a dual USB interface.

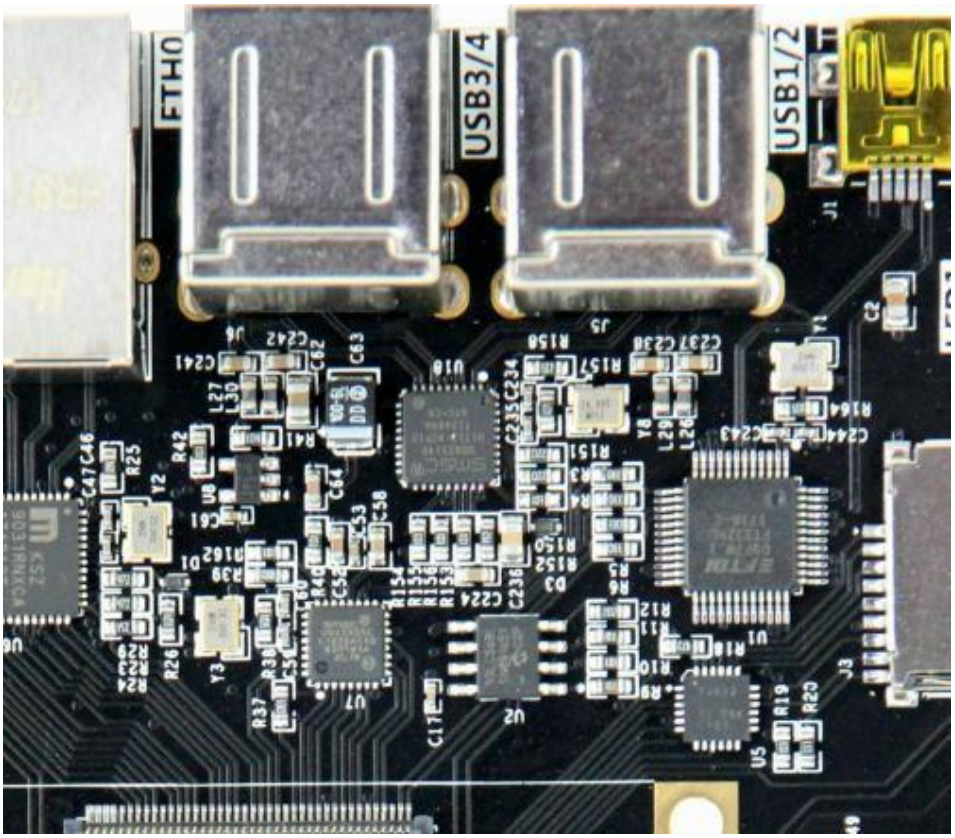


Figure 3-3-2: The USB2.0 on the Carrier Board

USB2.0 Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
OTG_DATA4	PS_MIO28_501	A12	USB data bit4
OTG_DIR	PS_MIO29_501	E8	USB data direction signal
OTG_STP	PS_MIO30_501	A11	USB stop signal
OTG_NXT	PS_MIO31_501	F9	USB next data signal

OTG_DATA0	PS_MIO32_501	C7	USB data bit0
OTG_DATA1	PS_MIO33_501	G13	USB data bit1
OTG_DATA2	PS_MIO34_501	B12	USB data bit2
OTG_DATA3	PS_MIO35_501	F14	USB data bit3
OTG_CLK	PS_MIO36_501	A9	USB clock signal
OTG_DATA5	PS_MIO37_501	B14	USB data bit5
OTG_DATA6	PS_MIO38_501	F13	USB data bit6
OTG_DATA7	PS_MIO39_501	C13	USB data bit7
OTG_RESETN	PS_MIO8_500	E5	USB reset signal

3.4 HDMI Output Interface

The HDMI output interface is implemented by Silion Image's SIL9134 HDMI (DVI) encoding chip, which supports up to 1080P@60Hz output and supports 3D output.

Among them, the SIL9134 video digital interface, audio digital interface and I2C configuration interface are connected with the BANK35 IO of the ZYNQ7000 PL part. The ZYNQ7000 system initializes and controls the SIL9134 through the I2C pin.

The hardware connection diagram of SIL9134 chip and ZYNQ7000 is shown in Figure 3-4-1.

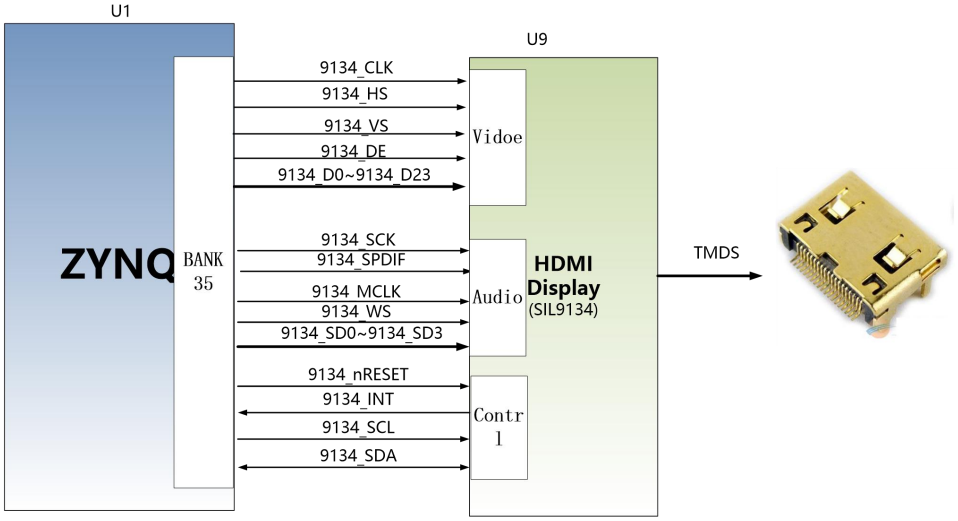


Figure3-4-1: The hardware connection of SIL9134 chip and ZYNQ7000

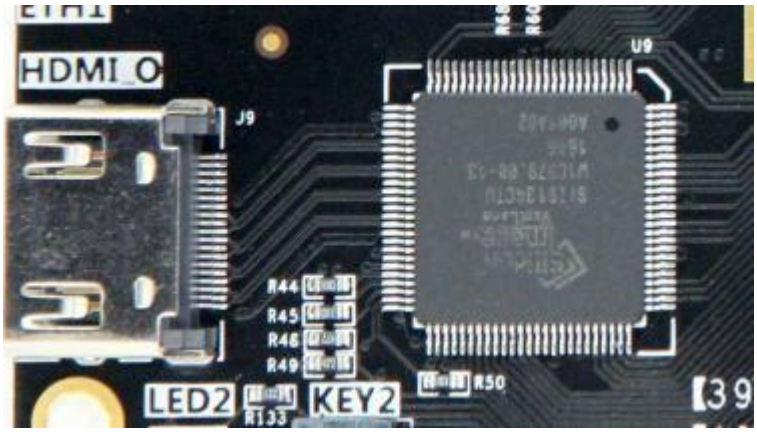


Figure3-4-2: The HDMI Interface on the Carrier Board

HDMI out Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
9134_CLK	B35_L4_N	G16	clock
9134_HS	B35_L21_P	E19	line synchronization
9134_VS	B35_L1_P	F16	column synchronization
9134_DE	B35_L21_N	E20	Signal valid
9134_D[0]	B35_L24_P	H22	Data0
9134_D[1]	B35_L24_N	G22	Data 1
9134_D[2]	B35_L6_P	G17	Data 2
9134_D[3]	B35_L6_N	F17	Data 3
9134_D[4]	B35_L4_P	G15	Data 4
9134_D[5]	B35_L3_N	D15	Data 5
9134_D[6]	B35_L3_P	E15	Data 6
9134_D[7]	B35_L5_P	F18	Data 7
9134_D[8]	B35_L5_N	E18	Data 8
9134_D[9]	B35_IO0	H17	Data 9
9134_D[10]	B35_IO25	H18	Data 10
9134_D[11]	B35_L19_P	H19	Data 11
9134_D[12]	B35_L19_N	H20	Data 12
9134_D[13]	B35_L20_P	G19	Data 13
9134_D[14]	B35_L20_N	F19	Data 14
9134_D[15]	B35_L22_P	G20	Data 15
9134_D[16]	B35_L22_N	G21	Data 16
9134_D[17]	B35_L23_P	F21	Data 17
9134_D[18]	B35_L23_N	F22	Data 18
9134_D[19]	B35_L17_P	E21	Data 19
9134_D[20]	B35_L17_N	D21	Data 20
9134_D[21]	B35_L16_P	D22	Data 21
9134_D[22]	B35_L16_N	C22	Data 22
9134_D[23]	B35_L18_P	B21	Data 23
9134_SCK	B35_L13_P	B19	Audio Interface I2S Clock
9134_SPDIF	B35_L1_N	E16	Audio S/PDIF input
9134_MCLK	B35_L2_P	D16	Audio input master clock
9134_WS	B35_L14_N	C20	Audio interface I2S word selection
9134_SD0	B35_L14_P	D20	Audio Interface I2S Data0
9134_SD1	B35_L12_P	D18	Audio Interface I2S Data1
9134_SD2	B35_L12_N	C19	Audio Interface I2S Data2

9134_SD3	B35_L2_N	D17	Audio Interface I2S Data3
9134_nRESET	B35_L11_P	C17	Reset signal
9134_INT	B35_L13_N	B20	Interrupt signal
9134_SCL	B35_L18_N	B22	IIC control clock
9134_SDA	B35_L15_N	A22	IIC Control data

3.5 USB to serial port

The AX7021 carrier board is also equipped with a serial port interface for overall debugging of the ZYNQ7000 system. The conversion chip uses the USB-UAR chip of Silicon Labs CP2102GM. The USB interface uses the MINI USB interface. It can be connected to the USB of the PC with a USB cable. The port performs separate power supply and serial data communication of the core board.

Figure 3-5-1 detailed the schematic diagram of the USB Uart circuit design.

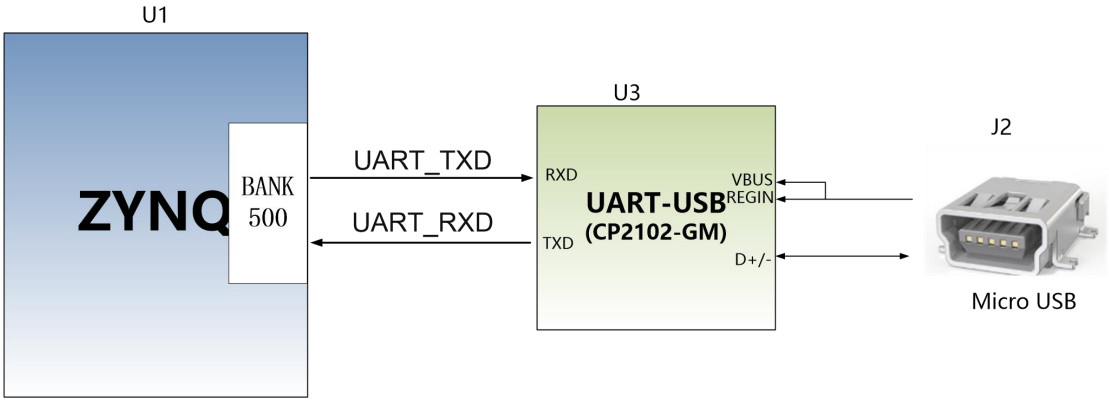


Figure 3-5-1: The Schematic Diagram of the USB Uart Circuit

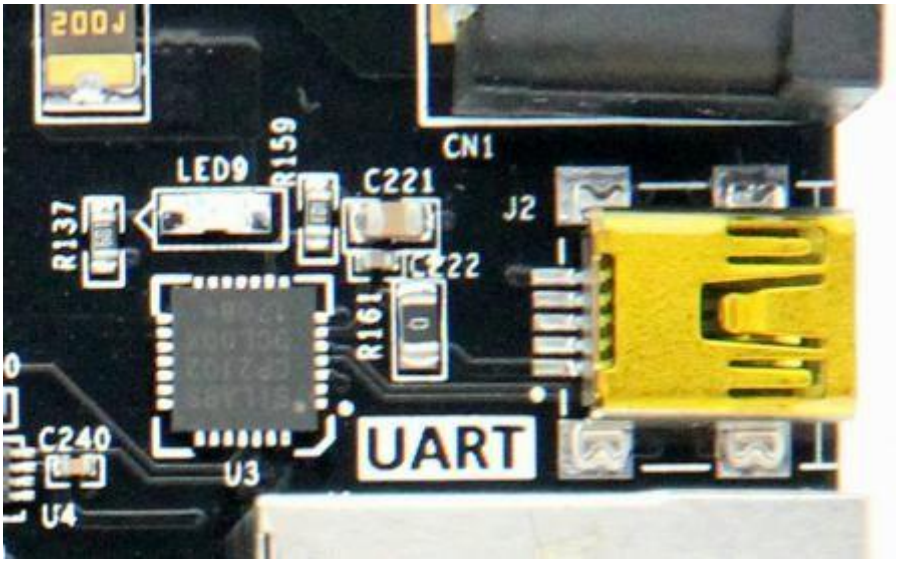


Figure 3-5-2: The UART on the Carrier Board

Uart Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
UART_RXD	PS_MIO13_500	A6	Uart data input
UART_TXD	PS_MIO12_500	C5	Uart data output

3.6 SD card slot

The AX7021 carrier board contains a Micro SD card interface to provide user access to the SD card memory, the BOOT program for the ZYNQ chip, the Linux operating system kernel, the file system and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of ZYNQ. Since the VCCMIO of the BANK is set to 1.8V, but the data level of the SD card is 3.3V, connected through the TXS02612 level shifter. The schematic of the Zynq7000 PS and SD card connector is shown in Figure 3-6-1

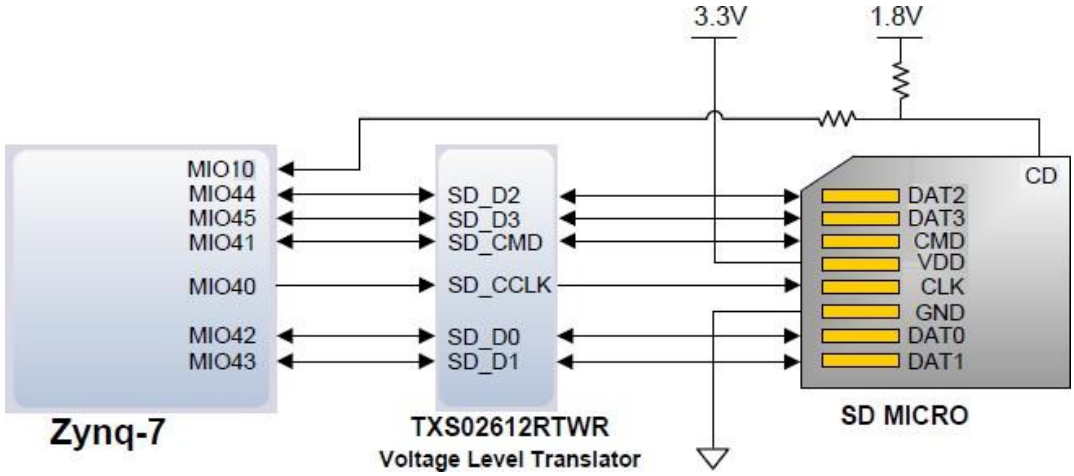


Figure 3-6-1: SD Card Connection Diagram

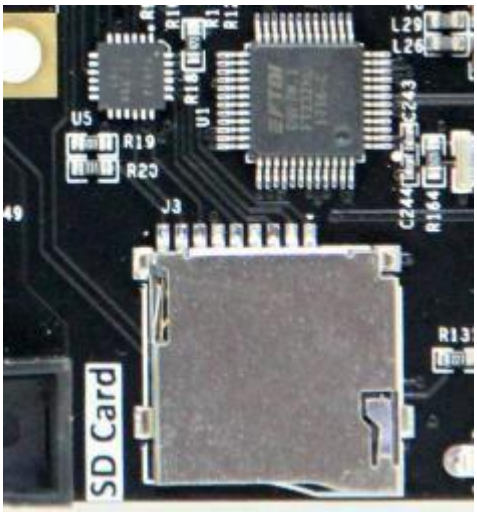


Figure 3-6-2: SD Card on the Carrier Board

Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
SD_CLK	PS_MIO40	E14	SD clock signal
SD_CMD	PS_MIO41	C8	SD command signal
SD_D0	PS_MIO42	D8	SD data0
SD_D1	PS_MIO43	B11	SD data1
SD_D2	PS_MIO44	E13	SD data2
SD_D3	PS_MIO45	B9	SD data3
SD_CD	PS_MIO10	G7	SD card insert signal

3.7 JTAG Interface

JTAG's download debug circuitry has been integrated on the AX7021 carrier board, so users do not need to purchase an additional Xilinx downloader. As long as a USB cable can be used for ZYNQ development and debug. The USB of PC and ZYNQ JTAG debug signals TCK, TDO, TMS, TDI are used for data communication via the FTDI USB bridge chip FT232HL on the development board. On the AX7021 development board, the JTAG interface is in the USB interface mode. Users can connect the PC and JTAG interface to the ZYNQ system debugging through the USB cable provided by us.

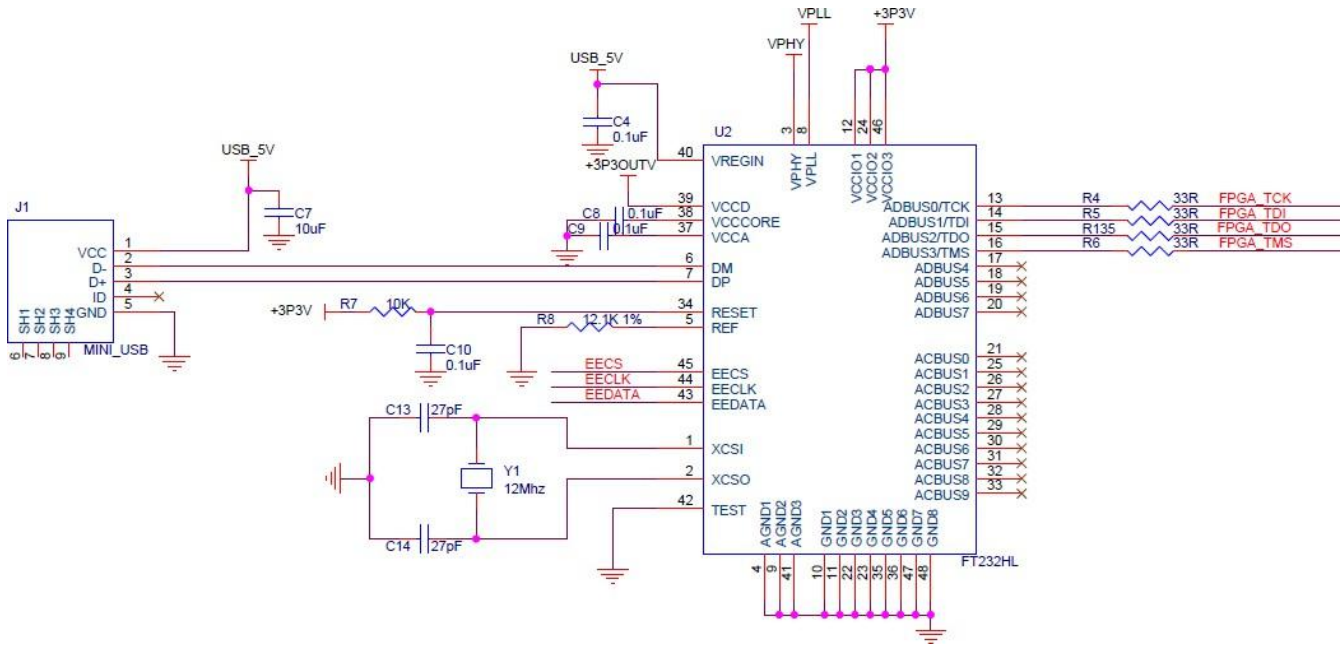


Figure 3-7-1: JTAG interface part of the schematic

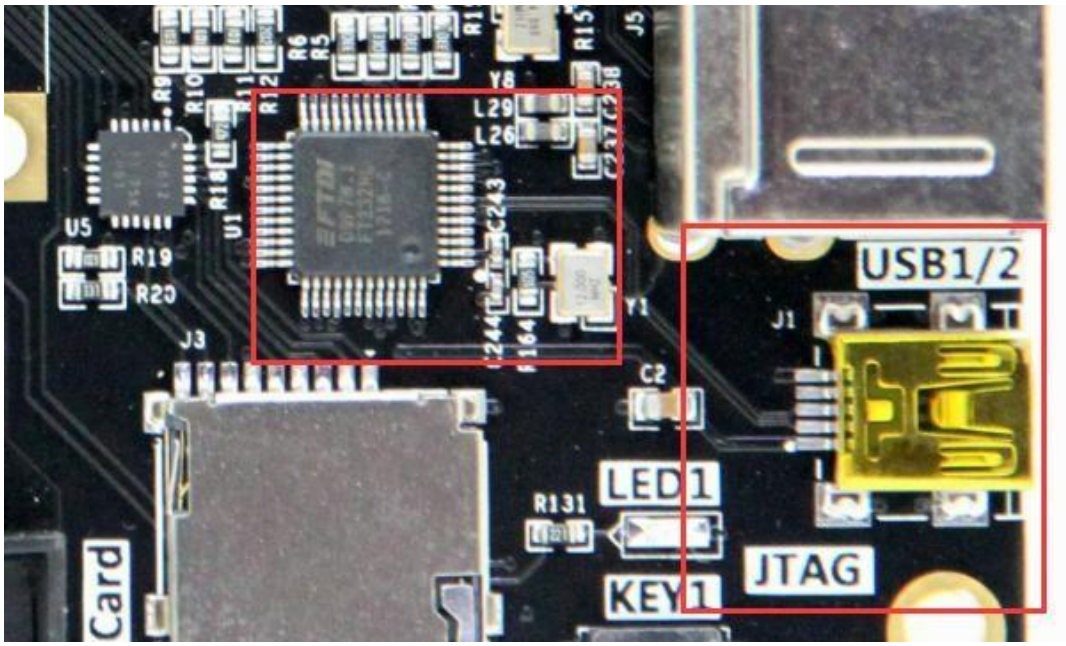


Figure 3-7-2: JTAG Interface on the Carrier Board

3.8 LED

The AX7021 has three red LEDs on the carrier board, one of which is the power indicator (PWR) and two of which are user LEDs (LED1~LED2). When the carrier board is powered, the power indicator will light up; two user LEDs are connected to the MIO of the PS, and one is connected to the IO of the PL. The user can control the light on and off by the program. When the IO voltage is high, the user LED is off, and when the connection IO voltage is low, the user LED is illuminated. The schematic diagram of the LED light hardware connection is shown in Figure 3-8-1:

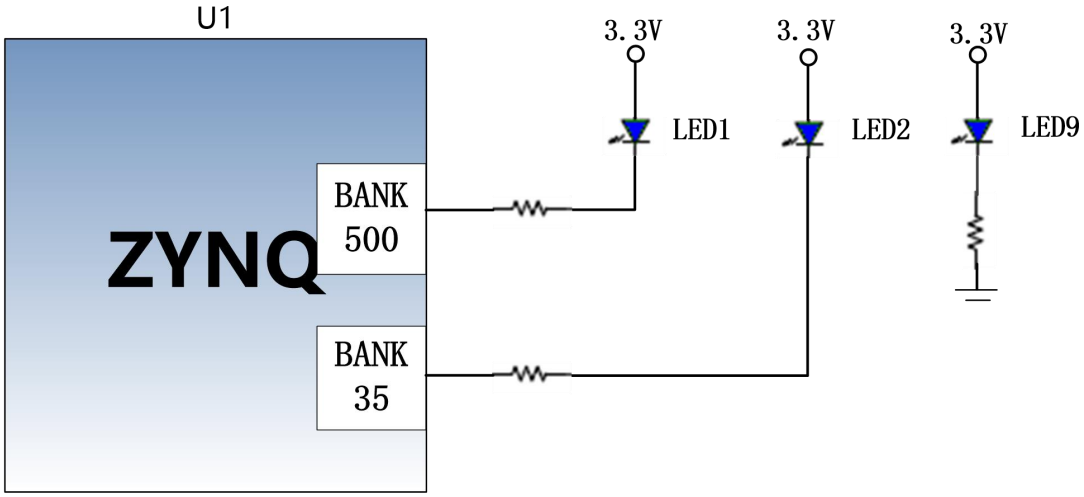


Figure 3-8-1: LED hardware connection Diagram on the Carrier Board

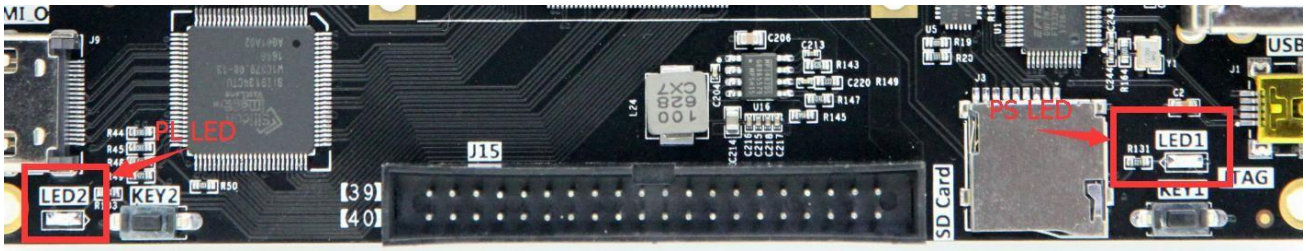


Figure 3-8-2: LED on the Carrier Board

Pin Assignment:

Signal Name	Pin Name	Pin Number	Remark
PS_LED	PS_MIO9_500	C4	PS LED
PL_LED	B35_L9_P	A16	PL LED

3.9 User Button

The AX7021 has two user buttons KEY1 and KEY2 on the carrier board. KEY1 is connected to the MIO pin of the ZYNQ chip PS, and KEY2 is connected to the IO pin of the ZYNQ chip PL. When the button is pressed, the signal is low, and the ZYNQ chip detects a low level to determine whether the button is pressed. The schematic diagram of the user button connection is shown in Figure 3-9-1:

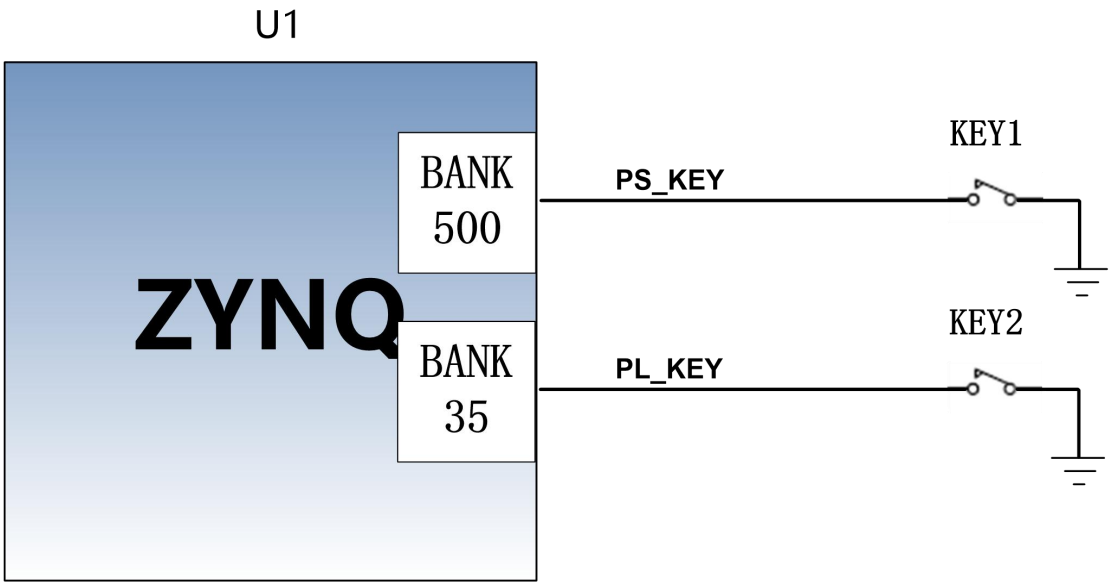


Figure 3-9-1: The Schematic Diagram of the User Button

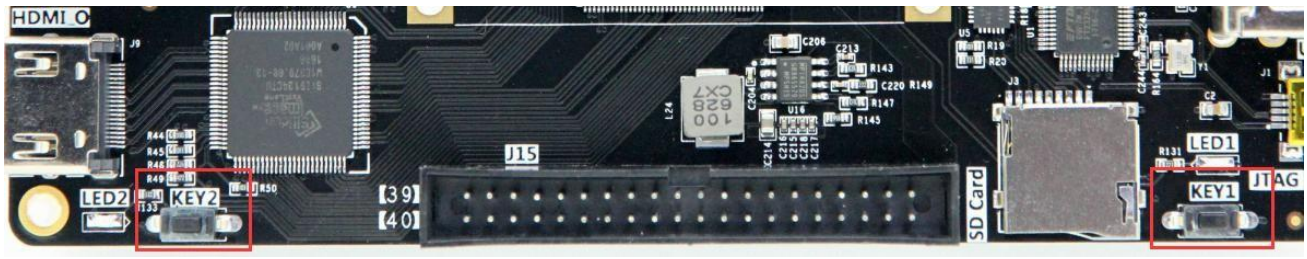


Figure 3-9-2: The User Button on the Carrier Board

Pin Assignment:

Pin	Signal Name	Pin Name	Pin Number
PS_KEY	PS_MIO11_500	B4	PS User Key
PL_KEY	B35_L9_N	A17	PL User Key

3.10 Extension Port

The AX7021 carrier board is reserved with two 2.54-mm standard 40-pin expansion ports J15 and J16 for connecting various modules of ALINX or external circuits designed by the user. The expansion port has 40 signals, of which 1 channel is 5V power supply. 2 channels are 3.3V power supplies, 3 Ground, 34 IOs. **Do not connect the IO directly to a 5V device to avoid burning the ZYNQ7000 chip. If you want to connect a 5V device, you need to connect a level shifting chip.**

A 33 ohm resistor is connected in series between the expansion port and the ZYNQ7000 connection to protect the ZYNQ7000 chip from external voltage or current. The circuit of the expansion port (J15) is shown in Figure 3-10-1.

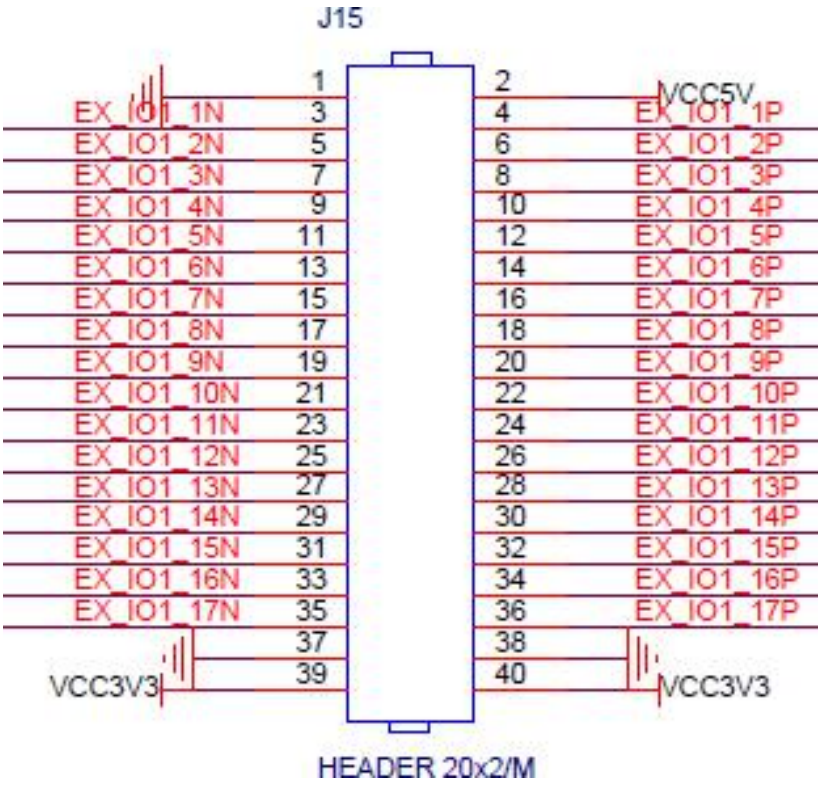


Figure 3-10-1: The Expansion Port J15 Schematic

Figure 3-10-2 shows the physical map of the J15 expansion port. Pin39 and Pin40 of the expansion port are indicated on the board.

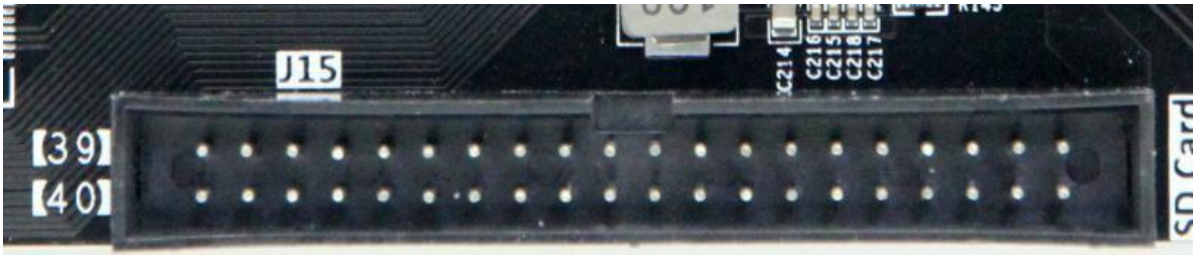


Figure 3-10-2: The J15 Expansion Port on the Carrier Board

J15 Pin Assignment:

Pin	Signal Name	Pin Name	Pin Number
1	GND	2	+5V（Input）
3	T21	4	U21
5	U20	6	V20
7	Y19	8	AA19
9	J21	10	J22
11	K21	12	J20
13	P16	14	R16
15	M17	16	L17
17	T18	18	R18
19	P20	20	P21

21	T19	22	R19
23	P15	24	N15
25	M16	26	M15
27	AB19	28	AB20
29	W22	30	V22
31	W21	32	W20
33	AA21	34	AB21
35	Y21	36	Y20
37	GND	38	GND
39	+3.3V	40	+3.3V（Output）

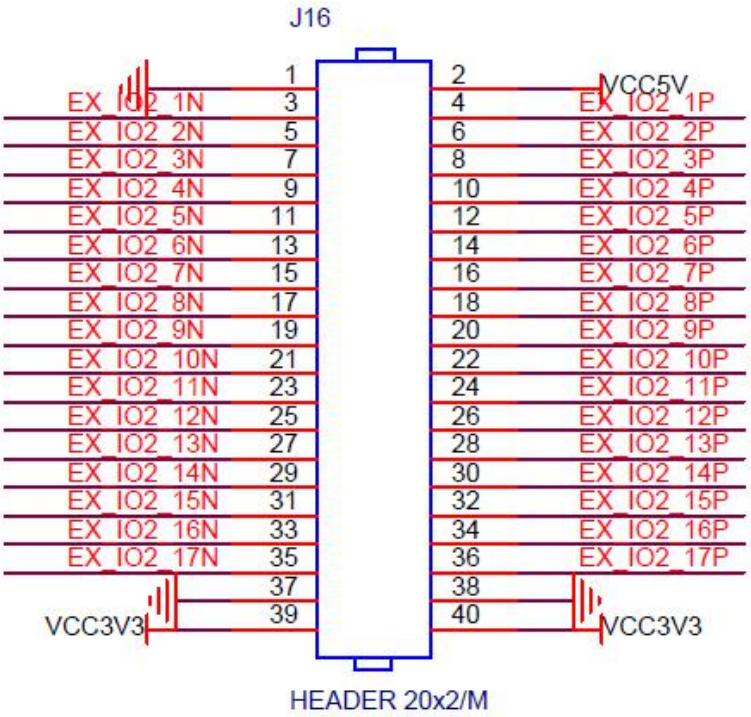


Figure 3-10-3: The Expansion Port J16 Schematic

Figure 3-10-4: The J16 Expansion Port on the Carrier Board

J16 Pin Assignment:

Pin	Signal Name	Pin Name	Pin Number
1	GND	2	+5V
3	V12	4	W12
5	U12	6	U11
7	U9	8	U10
9	T6	10	R6

11	U5	12	U6
13	U4	14	T4
15	W10	16	W11
17	Y10	18	Y11
19	W8	20	V8
21	AA6	22	AA7
23	AA11	24	AB11
25	AB4	26	AB5
27	AB1	28	AB2
29	Y4	30	AA4
31	AB10	32	AB9
33	AA9	34	AA8
35	AB7	36	AB6
37	GND	38	GND
39	+3.3V	40	+3.3V

3.11 Power Supply

The power supply input voltage of the development board is DC12V. The carrier board is converted into +5V, +1.2V, +3.3V and 1.8V four-way power supply through one DC/DC power chip MP2303 and three DC/DC power chip MP1482. Because the +5V power supply supplies power to the core board through the inter-board connector, the current output of the DC power supply is 3A, and the output current of the other three power supplies is 2A. In addition, there is an LDO chip on the board. The default output is 3.3V. If the BANK power of BANK33 and BANK34 of the core board is replaced with other voltage levels, the output of this LDO chip on the carrier board needs to be modified accordingly.

The power supply design on the carrier board is shown below

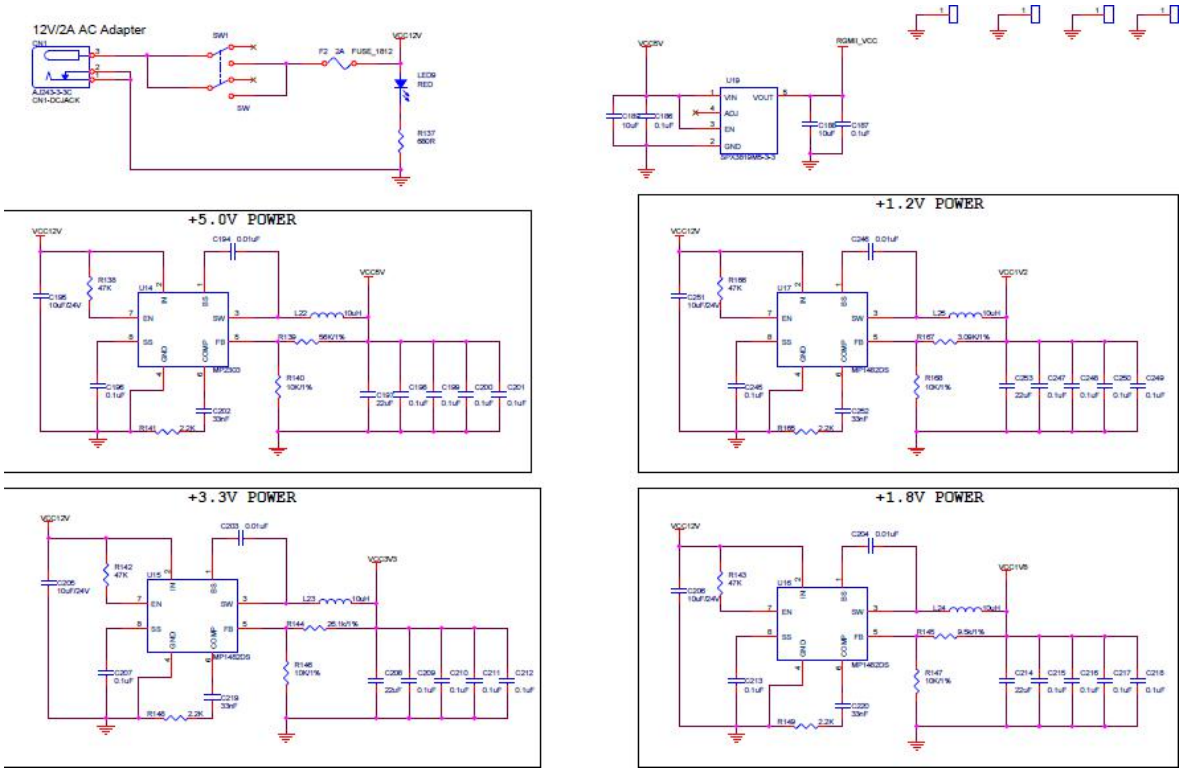


Figure 3-11-1: Power Supply Schematic on the Carrier Board

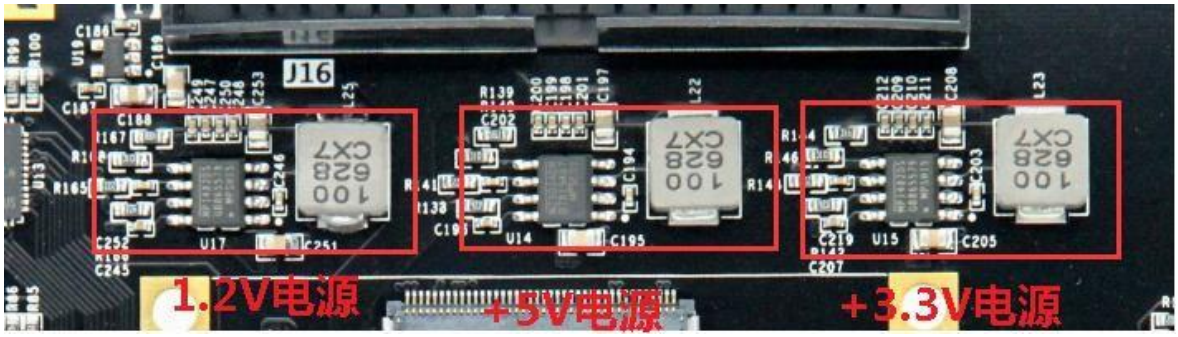


Figure 3-11-2: Power Supply on the Carrier Board (1.2V/5V/3.3V)

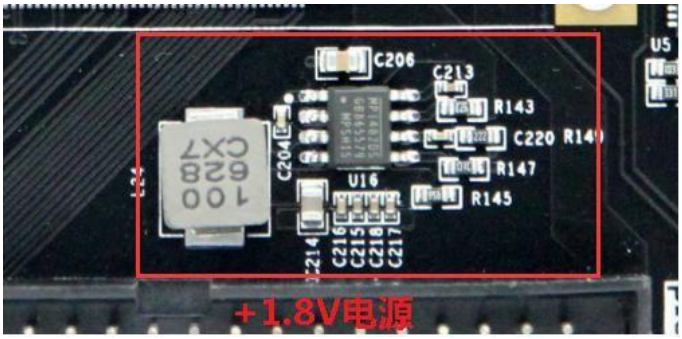


Figure 3-11-3: Power Supply on the Carrier board (1.8V)

3.12 Carrier Board Structure diagram

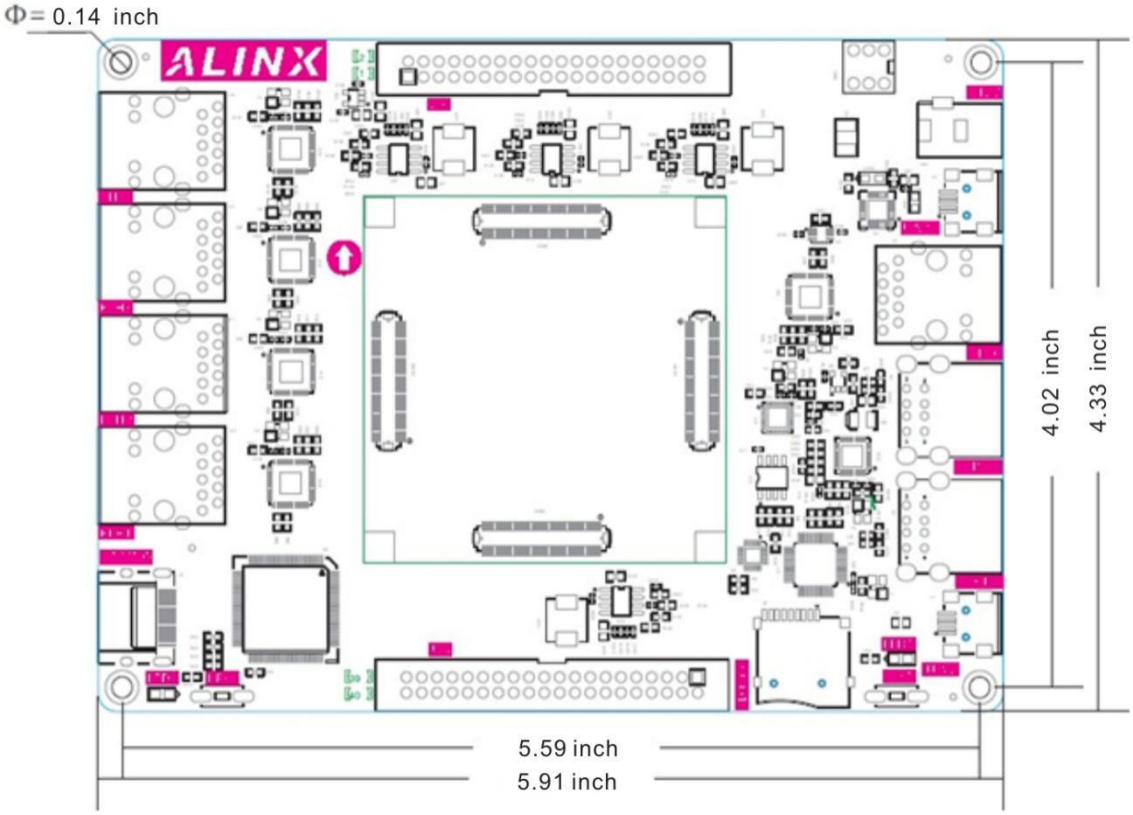


Figure 3-12-1: Carrier Board Structure Diagram