ZYNQ UltraScale+ FPGA Development Board AXU9EGB

User Manual

ALINX

Version Record

Version	Date	Release By	Description
Rev 1.1	2021-07-21	Rachel Zhou	First Release

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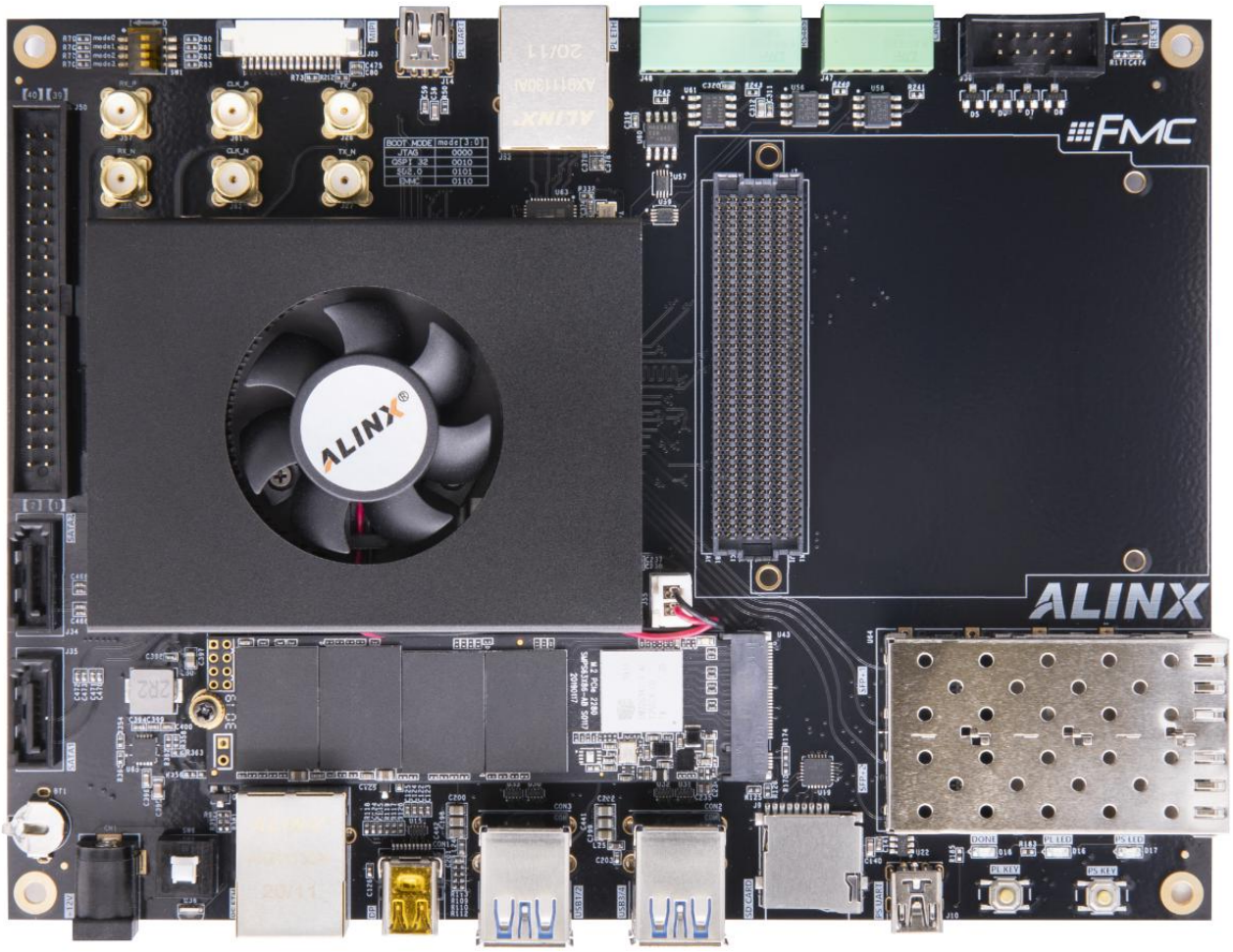
This MPSoCs FPGA development platform adopts the core board + carrier board mode, which is convenient for users to use the core board for secondary development. The core board uses XILINX Zynq UltraScale+ EG chip ZU9EV solution, uses Processing System(PS)+Programmable Logic(PL) technology to integrate dual-core ARM ARM Cortex-A53 and FPGA programmable logic on a single chip. In addition, the PS side of the core board has 4 pieces of 1GB high-speed DDR4 SDRAM chips, 1 piece of 8GB eMMC memory chip and 1 piece of 256Mb QSPI FLASH chip; the PL side of the core board has 2 pieces of 1GB DDR4 SDRAM chip

In the design of carrier board, we have extended a wealth of interfaces for users, such as 1 FMC LPC interface, 1 SATA M.2 interface, 1 DP interface, 1 PCIe x 2.0, 4 USB 3.0 Interface, 2 Gigabit Ethernet interfaces, 1 HDMI Output, 1 HDMI Input, 2 Uart, 1 SD card slot, 2-Channel CAN bus interfaces, 2-Channel RS485 bus interfaces, 1 MIPI Camera Interface. It meets users' requirements for high-speed data exchange, data storage, Video transmission processing, deep learning, artificial intelligence and industrial control. It is a "professional" ZYNQ development platform. For high-speed data transmission and exchange, pre-verification and post-application of data processing is possible. This product is very suitable for students, engineers and other groups engaged in MPSoCs development.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Part 1: FPGA Development Board Introduction

The entire structure of the AXU9EGB PGA development board is inherited from our consistent core board + carrier board model. A high-speed inter-board connector is used between the core board and the carrier board.

The core board is mainly composed of the smallest system of ZU9EG + 6 DDR4 + eMMC + 2 QSPI FLASH, the main FPGA chip is Xilinx's Zynq UltraScale+ MPSoCs family chip, the model number is XCZU9EG-2FFVB1156I. ZU9EG chip can be divided into processor system part Processor System (PS) and programmable logic part Programmable Logic (PL). On the PS side and PL side of the ZU9EV chip, there are 4 DDR4 and 2 DDR4 respectively, each with a capacity of up to 1GB, which enables the ARM system and FPGA system to independently process and store data. The 8GB eMMC FLASH memory chip and two 256Mb QSPI FLASH which are on the PS side, used to statically store the operating system, file system and user data of MPSoCs.

The AXU9EGB carrier board expands its rich peripheral interface, including 1 M.2 interface, 1 DP output interface, 4 USB 3.0 Interface, 2 Gigabit Ethernet interfaces, 2 SFP Interfaces, 2 SATA Interfaces, 2 UART, 1 SD card slot, 1 FMC Interface, 2-Channel CAN bus interfaces, 2-Channel RS485 bus interfaces, 1 MIPI Camera Interface, 40-pin expansion ports and some keys and LEDs.

The following figure shows the structure of the entire development system:

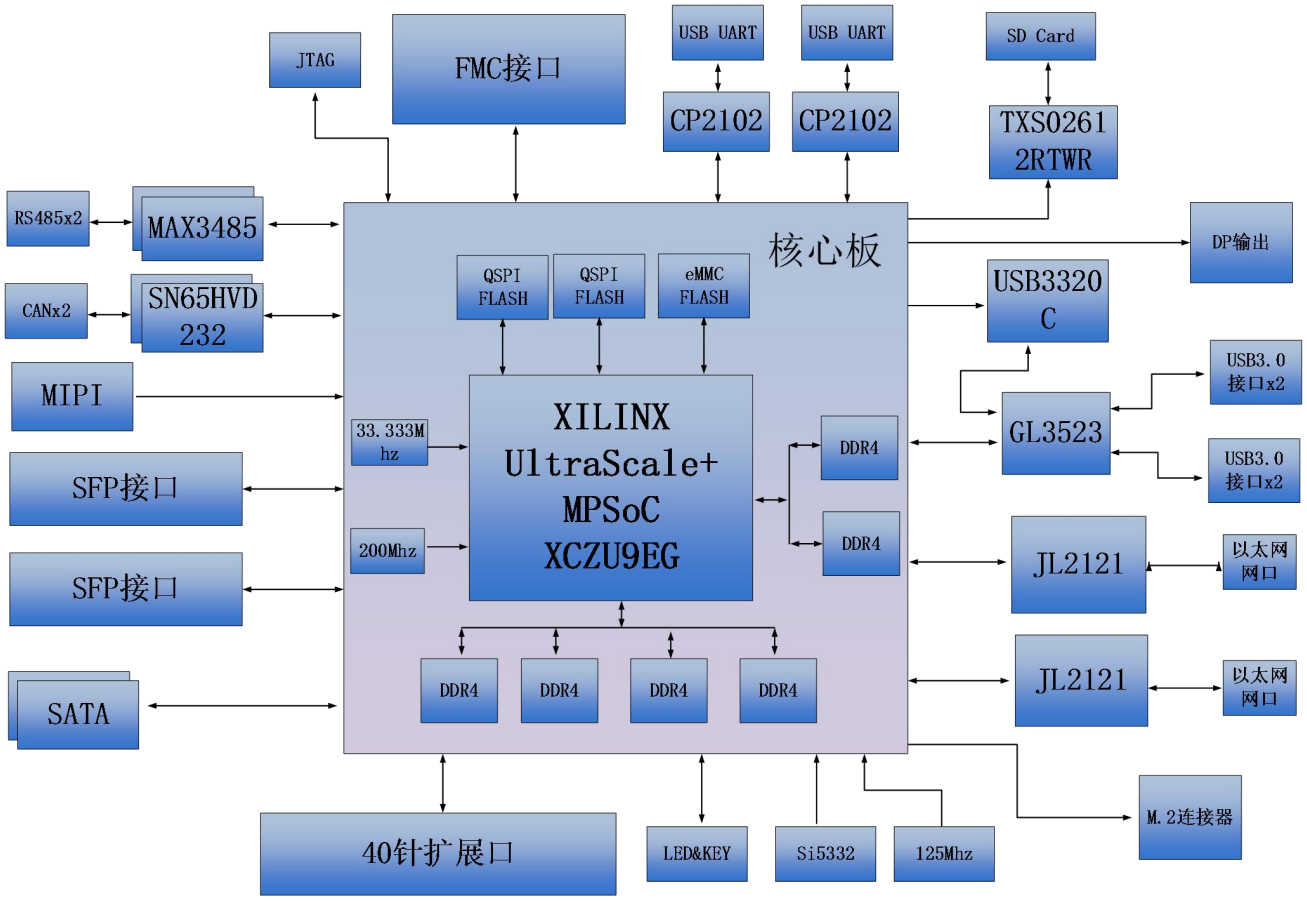


Figure 1-1-1: The Schematic Diagram of the AXU9EGB

Through this diagram, you can see the interfaces and functions that the AXU9EGB FPGA Development Board contains:

- ZU9EG core board

  It consists of ZU9EV +4GB DDR4（PS）+2GB DDR4（PL）+8GB eMMC FLASH + 512Mb QSPI FLASH, and there are 2 crystal oscillators to provide the clock, a single-ended 33.3333MHz crystal oscillator for the PS system, and a differential 200MHz crystal oscillator for the PL logic DDR reference clock.

- M.2 Interface

  1 PCIEx1 standard M.2 interface, used to connect M.2 SSD solid state drives, with a communication speed of up to 6Gbps.

- DP Output Interface

1 standard Display Port output display interface, used for video image display. Supports up to 4K@30Hz or 1080P@60Hz output

- USB 3.0 Interface

  4-channel USB3.0 HOST interface, USB interface type is TYPE A. Used to connect external USB peripherals, such as connecting a mouse, keyboard, U disk, etc.

- Gigabit Ethernet Interface

  2-Channel 10/100M/1000M Ethernet RJ45 interface for Ethernet data exchange with computers or other network devices. The network interface chip uses JLSemi JL2121-N040IRNX industrial grade GPHY chip.

- USB Uart Interface

  2-Channel Uart to USB interfaces for communication with the computer, for user debugging. The serial port chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface.

- 2-Channel SFP Fiber Interface

  The two high-speed transceivers of the GTH transceiver are connected to the transmitting and receiving of two optical modules, realizing two high-speed optical fiber communication interfaces. The transmitting and sending speed of each optical fiber data communication is as high as 12.5Gb/s.

- SD Card Slot Interface

  1 Micro SD card holder, used to store operating system image and file system.

- FMC Expansion Interface

  1 standard FMC LPC expansion port, which can be connected to various FMC modules of XILINX or ALINX (HDMI input and output modules, binocular camera modules, high-speed AD modules, etc.).

- CAN Communication Interface

  Two-way CAN bus interface, using TI's SN65HVD232 chip, the interface uses 4Pin green terminal blocks.

- 485 Communication Interface

  Two-way 485 communication interface, using MAX3485 chip of MAXIM company. The interface uses 6Pin green terminal blocks.

- MIPI Interface

  2 Lane MIPI camera input interfaces, used to connect MIPI camera module (AN5641).

- 40-pin Expansion Header

  The 40-pin 2.54mm pitch expansion port use for external ALINX modules (binocular camera, TFT LCD screen, high-speed AD module, etc.). The expansion port includes 1 channel of 5V power supply, 2 channels of 3.3V power supply, 3 channels of ground, and 34 channels of IO port.

- JTAG debug port

  A 10-pin 0.1 spacing standard JTAG ports for FPGA program download and debugging. Users can debug and download the ZU4EV system through the XILINX downloader.

- Temperature and humidity sensor chip LM75

  On-board temperature and humidity sensor chip LM75, used to detect the temperature and humidity of the surrounding environment around the FPGA development board

- EEPROM

  One EEPROM 24LC04 with I2C interface

- Real Time Clock (RTC)

  1 built-in RTC real-time clock

- LED Lights

  5 LEDs, include 1 LED on the core board, 4 LEDs on the carrier board.

There are 1 power indicator and on the core board. There are 1 power indicator,1 DONE Configuration indicator and 2 user indicators on the carrier board.

- KEYs

  3 KEYs, include 1 Rest KEY and 2 User KEYs.

Part 2: ACU9EG Core Board

Part 2.1: ACU9EG Core Board Introduction

ACU9EG (core board model, the same below) FPGA core board, ZYNQ chip is based on XCZU9EG-2FFVB1156I of XILINX company Zynq UltraScale+ MPSoCs EG Family.

This core board uses 6 Micron DDR4 chips MT40A512M16GE, of which 4 DDR4 chips are mounted on the PS side to form a 64-bit data bus bandwidth and 4GB capacity. 2 DDR4 chip is mounted on the PL end, which is a 32-bit data bus width and a capacity of 2GB. The highest operating speed of DDR4 SDRAM on the PS side can reach 1200MHz (data rate 2400Mbps), and the highest operating speed of DDR4 SDRAM on the PL side can reach 1200MHz (data rate 2400Mbps). In addition, two 256MBit QSPI FLASH and an 8GB eMMC FLASH chip are also integrated on the core board to start storage configuration and system files.

In order to connect with the carrier board, the four board-to-board connectors of this core board expand the PS side USB2.0 interface, Gigabit Ethernet interface, SD card interface and other remaining MIO ports; also expand 4 pairs of PS MGT high-speed transceiver interface; and 16 GTH transceivers and almost all IO ports on the PL side (HP I/O: 96, HD I/O: 84). The wiring between the XCZU9EG chip and the interface has been processed with equal length and differential, and the core board size is only 3.15*2.36 (inch), which is very suitable for secondary development.

Figure 2-1-1: ACU9EG Core Board (Front View)

Part 2.2: ZYNQ Chip

The FPGA core board ACU9EG uses Xilinx's Zynq UltraScale+ MPSoCs EG family chip, module XCZU9EG-2FFVB1156I. The PS system of the ZU9EG chip integrates 4 ARM Cortex™-A53 processors with a speed of up to 1.3Ghz and supports Level 2 Cache; it also contains 2 Cortex-R5 processors with a speed of up to 533Mhz

The ZU9EG chip supports 32-bit or 64-bit DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 memory chips, with rich high-speed interfaces on the PS side such as PCIE Gen2, USB3.0, SATA 3.1, DisplayPort; it also supports USB2.0, Gigabit Ethernet, SD/SDIO, I2C, CAN, UART, GPIO and other interfaces. The PL end contains a wealth of programmable logic units, DSP and internal RAM. .

Figure 2-2-1 detailed the Overall Block Diagram of the ZU9EG Chip.

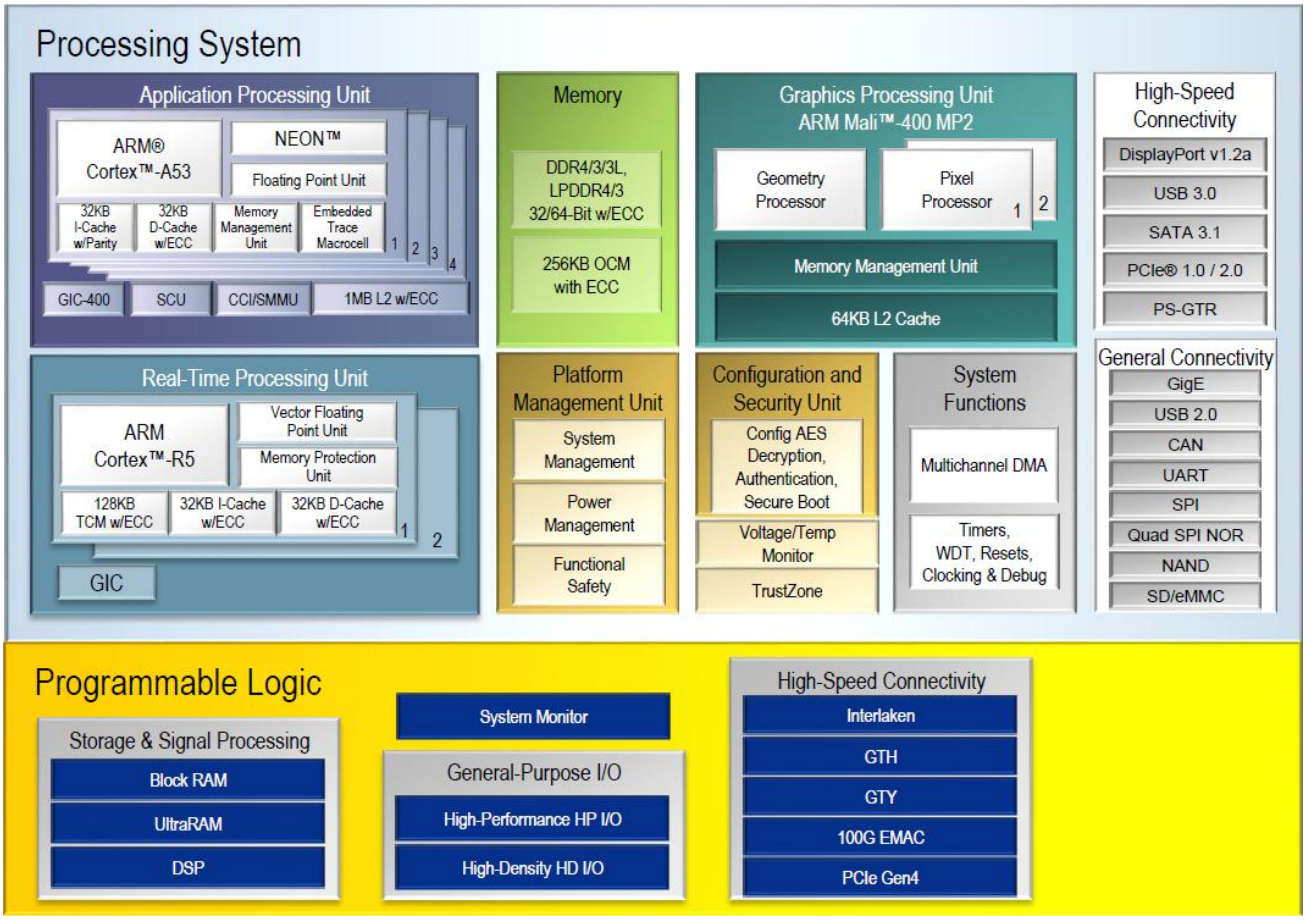


Figure 2-2-1: Overall Block Diagram of the ZYNQ ZU9EG Chip

The main parameters of the PS system part are as follows:

- ARM quad-core Cortex™-A53 processor, speed up to 1.3GHz, each CPU 32KB level 1 instruction and data cache, 1MB level 2 cache, shared by 2 CPUs
- ARM dual-core Cortex-R5 processor, speed up to 533MHz, each CPU 32KB level 1 instruction and data cache, and 128K tightly coupled memory.
- External storage interface, support 32/64bit DDR4/3/3L, LPDDR4/3 interface
- Static storage interface, support NAND, 2xQuad-SPI FLASH.
- High-speed connection interface, support PCIe Gen2 x 4, 2 x USB3.0, Sata 3.1, Display Port, 4 x Tri-mode, Gigabit Ethernet

- Common connection interfaces: 2 x USB2.0, 2 x SD/SDIO, 2 x UART, 2 x CAN 2.0B, 2 x I2C, 2 x SPI, 4 x 32b GPIO
- Power management: Support the four-part division of power supply Full/Low/PL/Battery
- Encryption algorithm: support RSA, AES and SHA.
- System monitoring: 10-bit 1Mbps AD sampling for temperature and voltage detection.

The main parameters of the PL logic part are as follows:

- Logic Cells: 600K
- CLB Flip-flops: 548K
- Look-up-tables (LUTs): 274K
- Block RAM: 32.1Mb
- Clock Management Units (CMTs): 4
- DSP Slices: 2520
- GTH 16.3Gb/s Transceiver: 24

XCZU9EG-2FFVB1156I chip speed grade is -2, industrial grade, package is FFVB1156.

Part 2.3: DDR4 DRAM

The ACU9EG core board is equipped with 6 Micron (Micron) 1GB DDR4 chips, model MT40A512M16LY-062E, of which 4 DDR4 chips are mounted on the PS side to form a 64-bit data bus bandwidth and 4GB capacity. Two DDR4 chip is mounted on the PL end, which is a 32-bit data bus width and a capacity of 2GB. The maximum operating speed of the DDR4 SDRAM on the PS side can reach 1200MHz (data rate 2400Mbps), and the 4 DDR4 storage systems are directly connected to the memory interface of the PS BANK504. The

highest operating speed of the DDR4 SDRAM on the PL side can reach 1200MHz (data rate 2400Mbps), and two piece of DDR4 is connected to the BANK64,65 interface of the FPGA. The specific configuration of DDR4 SDRAM is shown in Table 2-3-1 below:

Bit Number	Chip Model	Capacity	Factory
U4,U5,U6,U7	MT40A512M16LY-062E	512M x 16bit	Micron

Table 2-3-1: DDR4 SDRAM Configuration

The hardware design of DDR4 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR4.

The hardware connection of DDR4 SDRAM on the PS Side is shown in Figure 2-3-1:

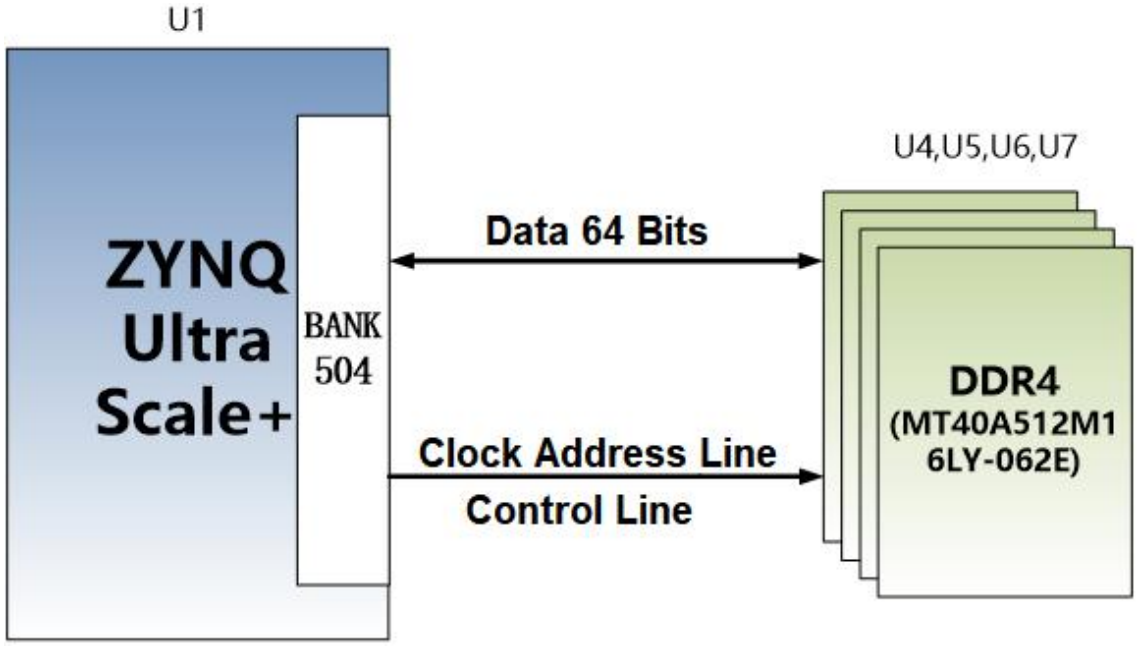


Figure 2-3-1: DDR3 DRAM schematic diagram

The hardware connection of DDR4 SDRAM on the Pl Side is shown in Figure 2-3-2:

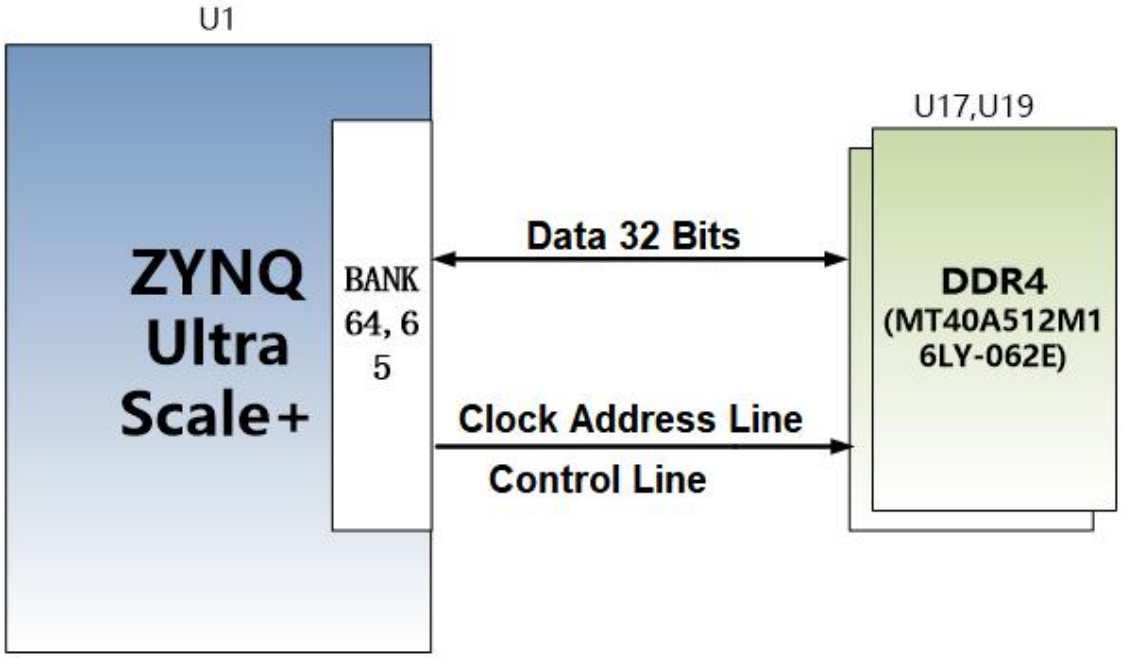


Figure 2-3-2: DDR4 DRAM schematic diagram

PS Side DDR4 DRAM pin assignment:

Signal Name	Pin Name	Pin Number
PS_DDR4_DQS0_N	PS_DDR_DQS_N0_504	AN19
PS_DDR4_DQS0_P	PS_DDR_DQS_P0_504	AN18
PS_DDR4_DQS1_N	PS_DDR_DQS_N1_504	AN22
PS_DDR4_DQS1_P	PS_DDR_DQS_P1_504	AN21
PS_DDR4_DQS2_N	PS_DDR_DQS_N2_504	AJ19
PS_DDR4_DQS2_P	PS_DDR_DQS_P2_504	AH19
PS_DDR4_DQS3_N	PS_DDR_DQS_N3_504	AH23
PS_DDR4_DQS3_P	PS_DDR_DQS_P3_504	AH22
PS_DDR4_DQS4_N	PS_DDR_DQS_N4_504	AH29
PS_DDR4_DQS4_P	PS_DDR_DQS_P4_504	AH28
PS_DDR4_DQS5_N	PS_DDR_DQS_N5_504	AE29
PS_DDR4_DQS5_P	PS_DDR_DQS_P5_504	AE28
PS_DDR4_DQS6_N	PS_DDR_DQS_N6_504	AK32
PS_DDR4_DQS6_P	PS_DDR_DQS_P6_504	AJ32
PS_DDR4_DQS7_N	PS_DDR_DQS_N7_504	AE33
PS_DDR4_DQS7_P	PS_DDR_DQS_P7_504	AE32
PS_DDR4_DQ0	PS_DDR_DQ0_504	AP20
PS_DDR4_DQ1	PS_DDR_DQ1_504	AP18

PS_DDR4_DQ2	PS_DDR_DQ2_504	AP19
PS_DDR4_DQ3	PS_DDR_DQ3_504	AP17
PS_DDR4_DQ4	PS_DDR_DQ4_504	AM20
PS_DDR4_DQ5	PS_DDR_DQ5_504	AM19
PS_DDR4_DQ6	PS_DDR_DQ6_504	AM18
PS_DDR4_DQ7	PS_DDR_DQ7_504	AL18
PS_DDR4_DQ8	PS_DDR_DQ8_504	AP22
PS_DDR4_DQ9	PS_DDR_DQ9_504	AP21
PS_DDR4_DQ10	PS_DDR_DQ10_504	AP24
PS_DDR4_DQ11	PS_DDR_DQ11_504	AN23
PS_DDR4_DQ12	PS_DDR_DQ12_504	AL21
PS_DDR4_DQ13	PS_DDR_DQ13_504	AL22
PS_DDR4_DQ14	PS_DDR_DQ14_504	AM23
PS_DDR4_DQ15	PS_DDR_DQ15_504	AL23
PS_DDR4_DQ16	PS_DDR_DQ16_504	AL20
PS_DDR4_DQ17	PS_DDR_DQ17_504	AK20
PS_DDR4_DQ18	PS_DDR_DQ18_504	AJ20
PS_DDR4_DQ19	PS_DDR_DQ19_504	AK18
PS_DDR4_DQ20	PS_DDR_DQ20_504	AG20
PS_DDR4_DQ21	PS_DDR_DQ21_504	AH18
PS_DDR4_DQ22	PS_DDR_DQ22_504	AG19
PS_DDR4_DQ23	PS_DDR_DQ23_504	AG18
PS_DDR4_DQ24	PS_DDR_DQ24_504	AG21
PS_DDR4_DQ25	PS_DDR_DQ25_504	AH21
PS_DDR4_DQ26	PS_DDR_DQ26_504	AG24
PS_DDR4_DQ27	PS_DDR_DQ27_504	AG23
PS_DDR4_DQ28	PS_DDR_DQ28_504	AK22
PS_DDR4_DQ29	PS_DDR_DQ29_504	AJ21
PS_DDR4_DQ30	PS_DDR_DQ30_504	AJ22
PS_DDR4_DQ31	PS_DDR_DQ31_504	AK23
PS_DDR4_DQ32	PS_DDR_DQ32_504	AG31
PS_DDR4_DQ33	PS_DDR_DQ33_504	AG30
PS_DDR4_DQ34	PS_DDR_DQ34_504	AG29
PS_DDR4_DQ35	PS_DDR_DQ35_504	AG28
PS_DDR4_DQ36	PS_DDR_DQ36_504	AJ30
PS_DDR4_DQ37	PS_DDR_DQ37_504	AK29

PS_DDR4_DQ38	PS_DDR_DQ38_504	AK30
PS_DDR4_DQ39	PS_DDR_DQ39_504	AJ29
PS_DDR4_DQ40	PS_DDR_DQ40_504	AE27
PS_DDR4_DQ41	PS_DDR_DQ41_504	AF28
PS_DDR4_DQ42	PS_DDR_DQ42_504	AF30
PS_DDR4_DQ43	PS_DDR_DQ43_504	AF31
PS_DDR4_DQ44	PS_DDR_DQ44_504	AD28
PS_DDR4_DQ45	PS_DDR_DQ45_504	AD27
PS_DDR4_DQ46	PS_DDR_DQ46_504	AD29
PS_DDR4_DQ47	PS_DDR_DQ47_504	AD30
PS_DDR4_DQ48	PS_DDR_DQ48_504	AH33
PS_DDR4_DQ49	PS_DDR_DQ49_504	AJ34
PS_DDR4_DQ50	PS_DDR_DQ50_504	AH34
PS_DDR4_DQ51	PS_DDR_DQ51_504	AH32
PS_DDR4_DQ52	PS_DDR_DQ52_504	AK34
PS_DDR4_DQ53	PS_DDR_DQ53_504	AK33
PS_DDR4_DQ54	PS_DDR_DQ54_504	AL32
PS_DDR4_DQ55	PS_DDR_DQ55_504	AL31
PS_DDR4_DQ56	PS_DDR_DQ56_504	AG33
PS_DDR4_DQ57	PS_DDR_DQ57_504	AG34
PS_DDR4_DQ58	PS_DDR_DQ58_504	AF32
PS_DDR4_DQ59	PS_DDR_DQ59_504	AF33
PS_DDR4_DQ60	PS_DDR_DQ60_504	AD31
PS_DDR4_DQ61	PS_DDR_DQ61_504	AD32
PS_DDR4_DQ62	PS_DDR_DQ62_504	AD34
PS_DDR4_DQ63	PS_DDR_DQ63_504	AD33
PS_DDR4_DM0	PS_DDR_DM0_504	AG20
PS_DDR4_DM1	PS_DDR_DM0_504	AN17
PS_DDR4_DM2	PS_DDR_DM1_504	AM21
PS_DDR4_DM3	PS_DDR_DM2_504	AK19
PS_DDR4_DM4	PS_DDR_DM3_504	AH24
PS_DDR4_DM5	PS_DDR_DM4_504	AH31
PS_DDR4_DM6	PS_DDR_DM5_504	AE30
PS_DDR4_DM7	PS_DDR_DM6_504	AJ31
PS_DDR4_A0	PS_DDR_A0_504	AP29
PS_DDR4_A1	PS_DDR_A1_504	AP30

PS_DDR4_A2	PS_DDR_A2_504	AP26
PS_DDR4_A3	PS_DDR_A3_504	AP27
PS_DDR4_A4	PS_DDR_A4_504	AP25
PS_DDR4_A5	PS_DDR_A5_504	AN24
PS_DDR4_A6	PS_DDR_A6_504	AM29
PS_DDR4_A7	PS_DDR_A7_504	AM28
PS_DDR4_A8	PS_DDR_A8_504	AM26
PS_DDR4_A9	PS_DDR_A9_504	AM25
PS_DDR4_A10	PS_DDR_A10_504	AL28
PS_DDR4_A11	PS_DDR_A11_504	AK27
PS_DDR4_A12	PS_DDR_A12_504	AJ25
PS_DDR4_A13	PS_DDR_A13_504	AL25
PS_DDR4_WE_B	PS_DDR_A14_504	AK25
PS_DDR4_CAS_B	PS_DDR_A15_504	AK24
PS_DDR4_RAS_B	PS_DDR_A16_504	AM24
PS_DDR4_ACT_B	PS_DDR_ACT_N_504	AG25
PS_DDR4_ALERT_B	PS_DDR_ALERT_N_504	AF22
PS_DDR4_BA0	PS_DDR_BA0_504	AH26
PS_DDR4_BA1	PS_DDR_BA1_504	AG26
PS_DDR4_BG0	PS_DDR_BG0_504	AK28
PS_DDR4_CS0_B	PS_DDR_CS_N0_504	AN28
PS_DDR4_ODT0	PS_DDR_ODT0_504	AM30
PS_DDR4_PARITY	PS_DDR_PARITY_504	AF20
PS_DDR4_RESET_B	PS_DDR_RST_N_504	AF21
PS_DDR4_CLK0_P	PS_DDR_CK0_504	AN26
PS_DDR4_CLK0_N	PS_DDR_CK_N0_504	AN27
PS_DDR4_CKE0	PS_DDR_CKE0_504	AN29

PL Side DDR4 DRAM pin assignment:

Signal Name	Pin Name	Pin Number
PL_DDR4_DQS0_N	IO_L22N_T3U_N7_DBC_AD0N_65	AF1
PL_DDR4_DQS0_P	IO_L22P_T3U_N6_DBC_AD0P_65	AJ1
PL_DDR4_DQS1_N	IO_L16N_T2U_N7_QBC_AD3N_65	AH1
PL_DDR4_DQS1_P	IO_L16P_T2U_N6_QBC_AD3P_65	AJ5
PL_DDR4_DQS2_N	IO_L10N_T1U_N7_QBC_AD4N_65	AJ6

PL_DDR4_DQS2_P	IO_L10P_T1U_N6_QBC_AD4P_65	AF8
PL_DDR4_DQS3_N	IO_L4N_T0U_N7_DBC_AD7N_65	AE8
PL_DDR4_DQS3_P	IO_L4P_T0U_N6_DBC_AD7P_65	AG11
PL_DDR4_DQ0	IO_L24P_T3U_N10 _I2C_SDA_65	AE2
PL_DDR4_DQ1	IO_L20P_T3L_N2_AD1P_65	AG3
PL_DDR4_DQ2	IO_L23N_T3U_N9_65	AD1
PL_DDR4_DQ3	IO_L21P_T3L_N4_AD8P_65	AF2
PL_DDR4_DQ4	IO_L23P_T3U_N8_I2C_SCLK_65	AD2
PL_DDR4_DQ5	IO_L20N_T3L_N3_AD1N_65	AH3
PL_DDR4_DQ6	IO_L24N_T3U_N11_PERSTN0_65	AE1
PL_DDR4_DQ7	IO_L21N_T3L_N5_AD8N_65	AF1
PL_DDR4_DQ8	IO_L17P_T2U_N8_AD10P_65	AE3
PL_DDR4_DQ9	IO_L15P_T2L_N4_AD11P_65	AH4
PL_DDR4_DQ10	IO_L18P_T2U_N10_AD2P_65	AD4
PL_DDR4_DQ11	IO_L14N_T2L_N3_GC_65	AG4
PL_DDR4_DQ12	IO_L18N_T2U_N11_AD2N_65	AE4
PL_DDR4_DQ13	IO_L14P_T2L_N2_GC_65	AG5
PL_DDR4_DQ14	IO_L17N_T2U_N9_AD10N_65	AF3
PL_DDR4_DQ15	IO_L15N_T2L_N5_AD11N_65	AJ4
PL_DDR4_DQ16	IO_L9N_T1L_N5_AD12N_65	AD6
PL_DDR4_DQ17	IO_L8P_T1L_N2_AD5P_65	AG8
PL_DDR4_DQ18	IO_L11P_T1U_N8_GC_65	AF6
PL_DDR4_DQ19	IO_L12N_T1U_N11_GC_65	AF7
PL_DDR4_DQ20	IO_L9P_T1L_N4_AD12P_65	AD7
PL_DDR4_DQ21	IO_L8N_T1L_N3_AD5N_65	AH8
PL_DDR4_DQ22	IO_L12P_T1U_N10_GC_65	AE7
PL_DDR4_DQ23	IO_L11N_T1U_N9_GC_65	AG6
PL_DDR4_DQ24	IO_L3P_T0L_N4_AD15P_65	AE12
PL_DDR4_DQ25	IO_L5N_T0U_N9_AD14N_65	AG9
PL_DDR4_DQ26	IO_L2N_T0L_N3_65	AH11
PL_DDR4_DQ27	IO_L6N_T0U_N11_AD6N_65	AE9
PL_DDR4_DQ28	IO_L2P_T0L_N2_65	AH12
PL_DDR4_DQ29	IO_L5P_T0U_N8_AD14P_65	AG10
PL_DDR4_DQ30	IO_L3N_T0L_N5_AD15N_65	AF12
PL_DDR4_DQ31	IO_L6P_T0U_N10_AD6P_65	AD10
PL_DDR4_DM0	IO_L19P_T3L_N0_DBC_AD9P_65	AH2

PL_DDR4_DM1	IO_L13P_T2L_N0_GC_QBC_65	AE5
PL_DDR4_DM2	IO_L7P_T1L_N0_QBC_AD13P_65	AH7
PL_DDR4_DM3	IO_L1P_T0L_N0_DBC_65	AE10
PL_DDR4_A0	IO_L5P_T0U_N8_AD14P_64	AN9
PL_DDR4_A1	IO_L16P_T2U_N6_QBC_AD3P_64	AN6
PL_DDR4_A2	IO_L10P_T1U_N6_QBC_AD4P_64	AN7
PL_DDR4_A3	IO_L15P_T2L_N4_AD11P_64	AP5
PL_DDR4_A4	IO_L11P_T1U_N8_GC_64	AK8
PL_DDR4_A5	IO_L10N_T1U_N7_QBC_AD4N_64	AP7
PL_DDR4_A6	IO_L3N_T0L_N5_AD15N_64	AM10
PL_DDR4_A7	IO_L7P_T1L_N0_QBC_AD13P_64	AN8
PL_DDR4_A8	IO_L11N_T1U_N9_GC_64	AK7
PL_DDR4_A9	IO_L4N_T0U_N7_DBC_AD7N_64	AP10
PL_DDR4_A10	IO_L14P_T2L_N2_GC_64	AM6
PL_DDR4_A11	IO_L8N_T1L_N3_AD5N_64	AM8
PL_DDR4_A12	IO_L15N_T2L_N5_AD11N_64	AP4
PL_DDR4_A13	IO_L7N_T1L_N1_QBC_AD13N_64	AP8
PL_DDR4_BA0	IO_L6P_T0U_N10_AD6P_64	AJ10
PL_DDR4_BA1	IO_L5N_T0U_N9_AD14N_64	AP9
PL_DDR4_RAS_B	IO_L4P_T0U_N6_DBC_AD7P_64	AP11
PL_DDR4_CAS_B	IO_L16N_T2U_N7_QBC_AD3N_64	AP6
PL_DDR4_WE_B	IO_L9P_T1L_N4_AD12P_64	AJ9
PL_DDR4_ACT_B	IO_L8P_T1L_N2_AD5P_64	AM9
PL_DDR4_CS_B	IO_L17N_T2U_N9_AD10N_64	AN4
PL_DDR4_CKE	IO_L6N_T0U_N11_AD6N_64	AK10
PL_DDR4_OTD	IO_L9N_T1L_N5_AD12N_64	AK9
PL_DDR4_BG0	IO_L3P_T0L_N4_AD15P_64	AL10
PL_DDR4_CLK_N	IO_L13N_T2L_N1_GC_QBC_64	AL5
PL_DDR4_CLK_P	IO_L13P_T2L_N0_GC_QBC_64	AL6
PL_DDR4_RST	IO_L14N_T2L_N3_GC_64	AM5

Part 2.4: QSPI Flash

The FPGA core board ACU9EG is equipped with two 256MBit Quad-SPI FLASH chip to form an 8-bit bandwidth data bus, the flash model is MT25QU256ABA1EW9-0SIT, which uses the 1.8V CMOS voltage standard.

Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 2-4-1.

Position	Model	Capacity	Factory
U2, U3	MT25QU256ABA1EW9-0SIT	256Mbit	Winbond

Table 2-4-1: QSPI FLASH Specification

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 2-4-1 shows the QSPI Flash in the schematic.

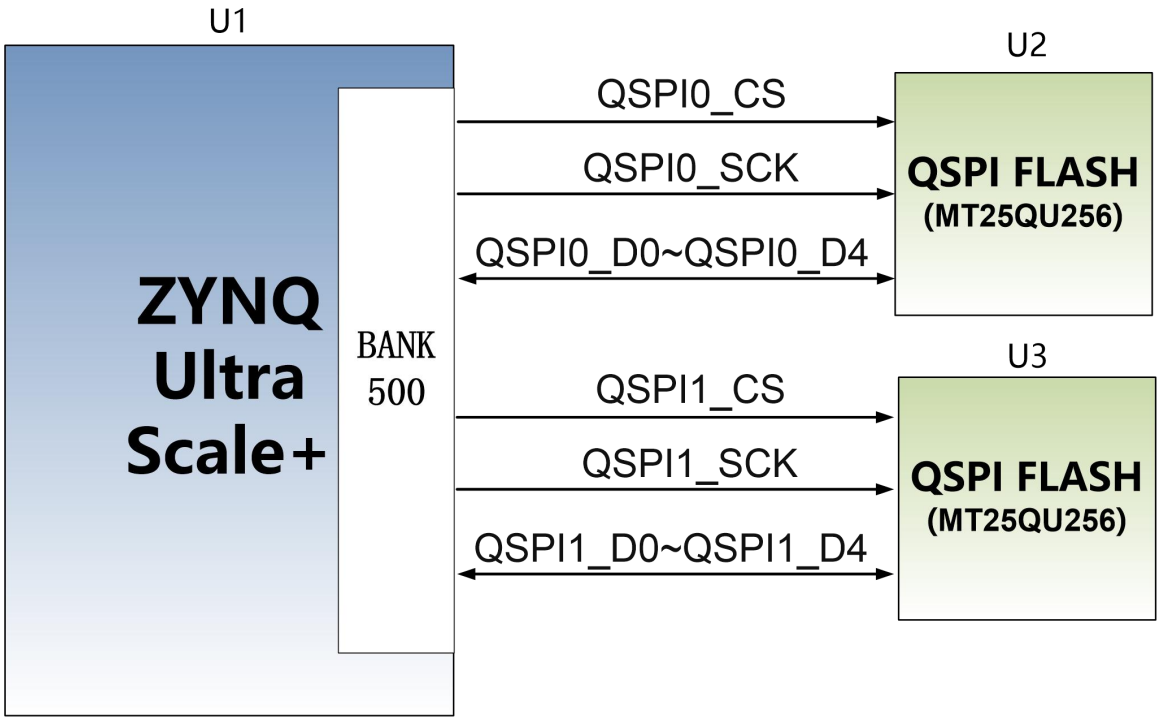


Figure 2-4-1: QSPI Flash in the schematic

Configure chip pin assignments:

Signal Name	Pin Name	Pin Number

MIO5_QSPI0_SS_B	PS_MIO5_500	AM15
MIO0_QSPI0_SCLK	PS_MIO0_500	AF16
MIO1_QSPI0_IO1	PS_MIO1_500	AJ16
MIO1_QSPI0_IO2	PS_MIO2_500	AD16
MIO1_QSPI0_IO3	PS_MIO3_500	AG16
MIO1_QSPI0_IO0	PS_MIO4_500	AH16
MIO7_QSPI1_SS_B	PS_MIO7_500	AD17
MIO12_QSPI1_SCLK	PS_MIO12_500	AJ17
MIO8_QSPI1_IO0	PS_MIO8_500	AE17
MIO8_QSPI1_IO1	PS_MIO9_500	AP15
MIO8_QSPI1_IO2	PS_MIO10_500	AH17
MIO8_QSPI1_IO3	PS_MIO11_500	AF17

Part 2.5: eMMC Flash

The ACU9EG core board is equipped with a large-capacity 8GB eMMC FLASH chip, the model is MTFC8GAKAJCN-4M, it supports the HS-MMC interface of the JEDEC e-MMC V5.0 standard, and the level supports 1.8V or 3.3V. The data width of eMMC FLASH and ZYNQ connection is 8bit. Due to the large-capacity and non-volatile characteristics of eMMC FLASH, it can be used as a large-capacity storage device in the ZYNQ system, such as storing ARM applications, system files and other user data files The specific models and related parameters of eMMC FLASH are shown in Table 2-5-1.

Position	Model	Capacity	Factory
U19	MTFC8GAKAJCN-4M	8G Byte	Micron

Table 2-5-1: eMMC FLASH Specification

The eMMC FLASH is connected to the GPIO port of the BANK500 of the PS part of the ZYNQ UltraScale+. In the system design, it is necessary to configure the GPIO port function of the PS side as an EMMC interface. Figure 2-5-1 shows the part of eMMC Flash in the schematic diagram.

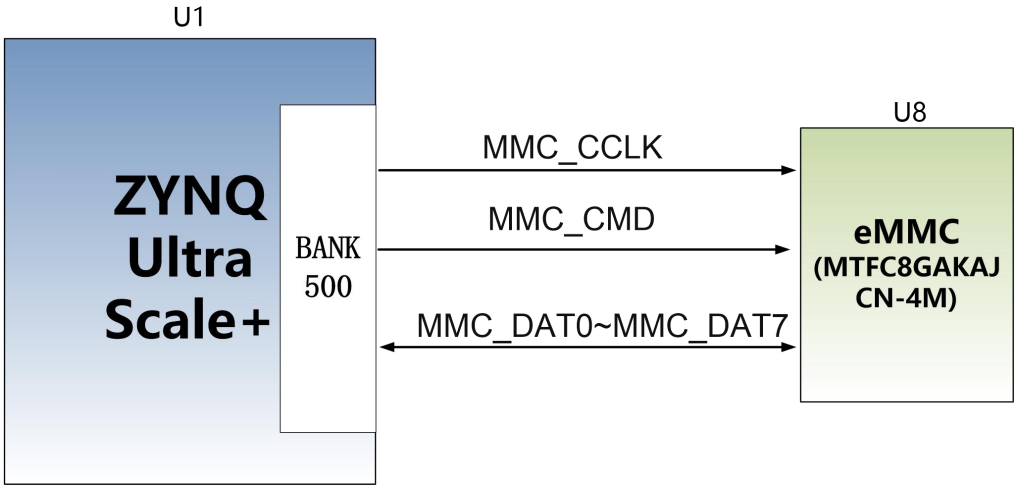


Figure 2-5-1: eMMC Flash in the schematic

Configuration Chip pin assignment:

Signal Name	Pin Name	Pin Number
MMC_CCLK	PS_MIO22_500	AD20
MMC_CMD	PS_MIO21_500	AF18
MMC_DAT0	PS_MIO13_500	AK17
MMC_DAT1	PS_MIO14_500	AL16
MMC_DAT2	PS_MIO15_500	AN16
MMC_DAT3	PS_MIO16_500	AM16
MMC_DAT4	PS_MIO17_500	AP16
MMC_DAT5	PS_MIO18_500	AE18
MMC_DAT6	PS_MIO19_500	AL17
MMC_DAT7	PS_MIO20_500	AD18
MMC_CCLK	PS_MIO22_500	AD20

Part 2.6: Clock configuration

The core board provides reference clock and RTC real-time clock for PS system and PL logic respectively, so that PS system and PL logic can work independently. The schematic diagram of the clock circuit design is shown in Figure 2-6-1:

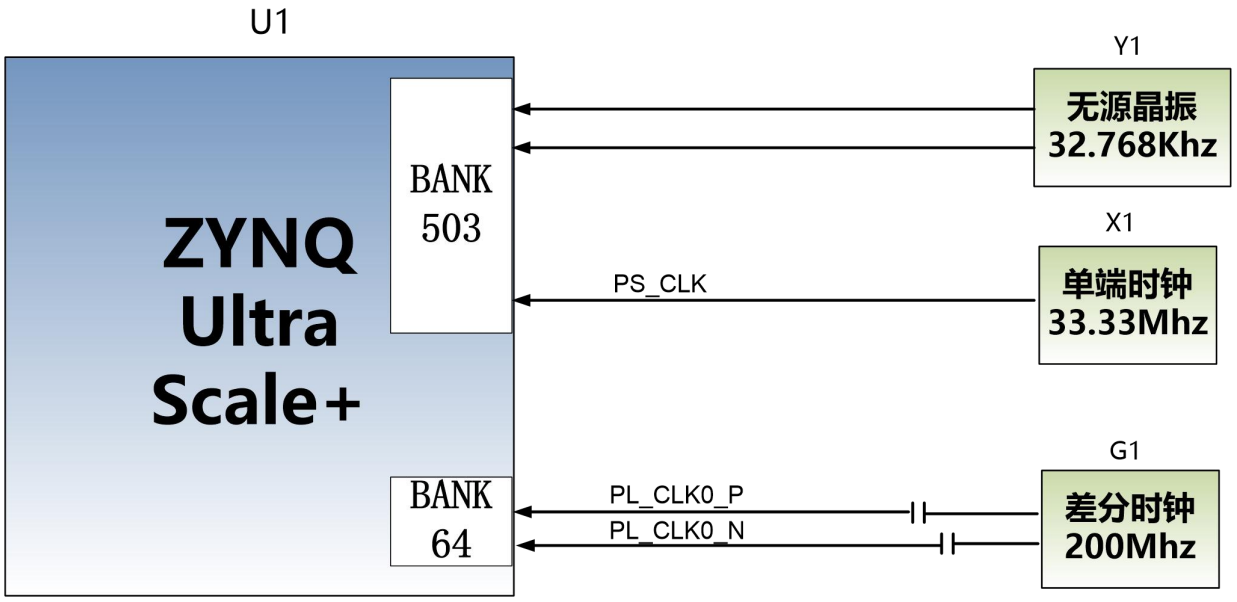


Figure 2-6-1: Core Board Clock Source

PS System RTC Real Time Clock

The passive crystal Y1 on the core board provides a 32.768KHz real-time clock source for the PS system. The crystal is connected to the PS_PADI_503 and PS_PADO_503 pins of BANK503 of the ZYNQ chip. The schematic diagram is shown in Figure 2-6-2:

Figure 2-6-2: Passive Crystal Oscillator for RTC

Clock pin assignment:

Signal Name	Pin
PS_PADI_503	**V21**
PS_PADO_503	**V22**

PS System Clock Source

The X1 crystal on the core board provides a 33.333MHz clock input for the PS part. The clock input is connected to the PS_REF_CLK_503 pin of BANK503 of the ZYNQ chip. The schematic diagram is shown in Figure 2-6-3:

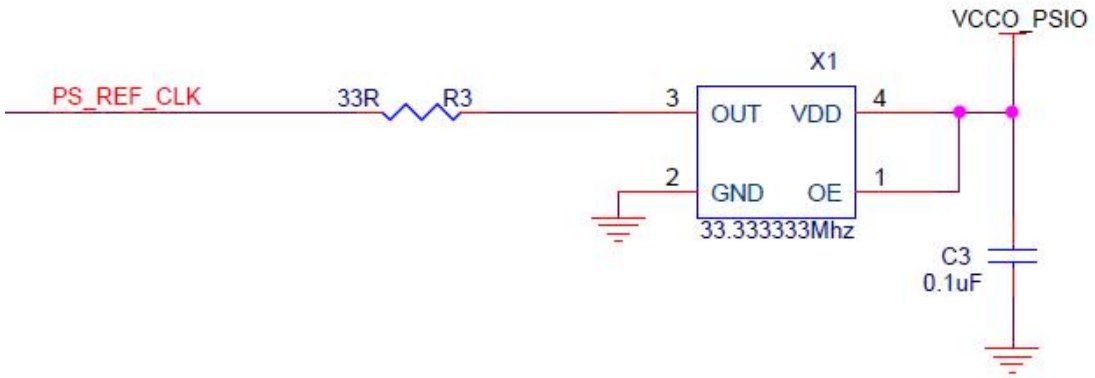


Figure 2-6-3: Active Crystal in PS part

Clock pin assignment:

Signal Name	Pin
PS_REF_CLK	U24

PL System Clock Source

The core board provides a differential 200MHz PL system clock source for the reference clock of the DDR4 controller. The crystal oscillator output is connected to the global clock (MRCC) of PL BANK64. This global clock can be used to drive the DDR4 controller and user logic circuits in the FPGA. The schematic diagram of this clock source is shown in Figure 2-6-4

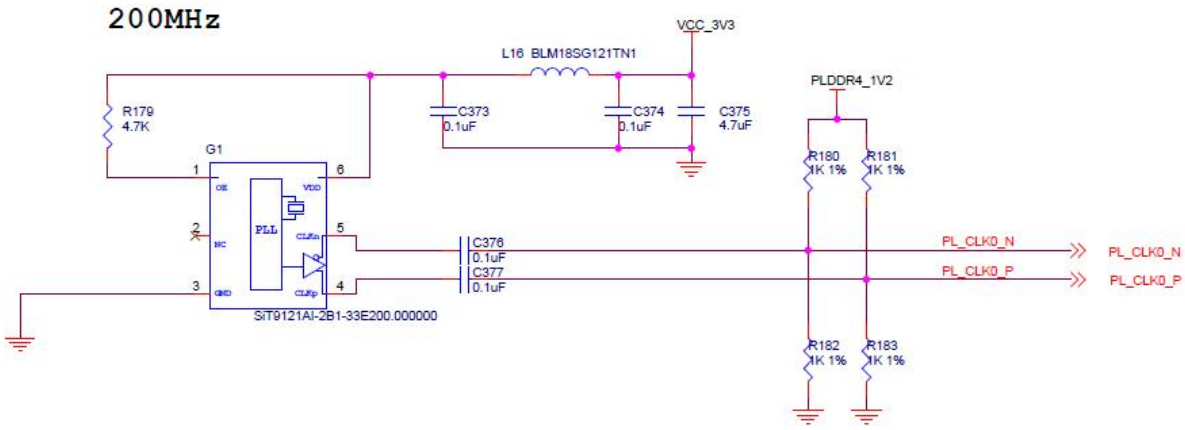


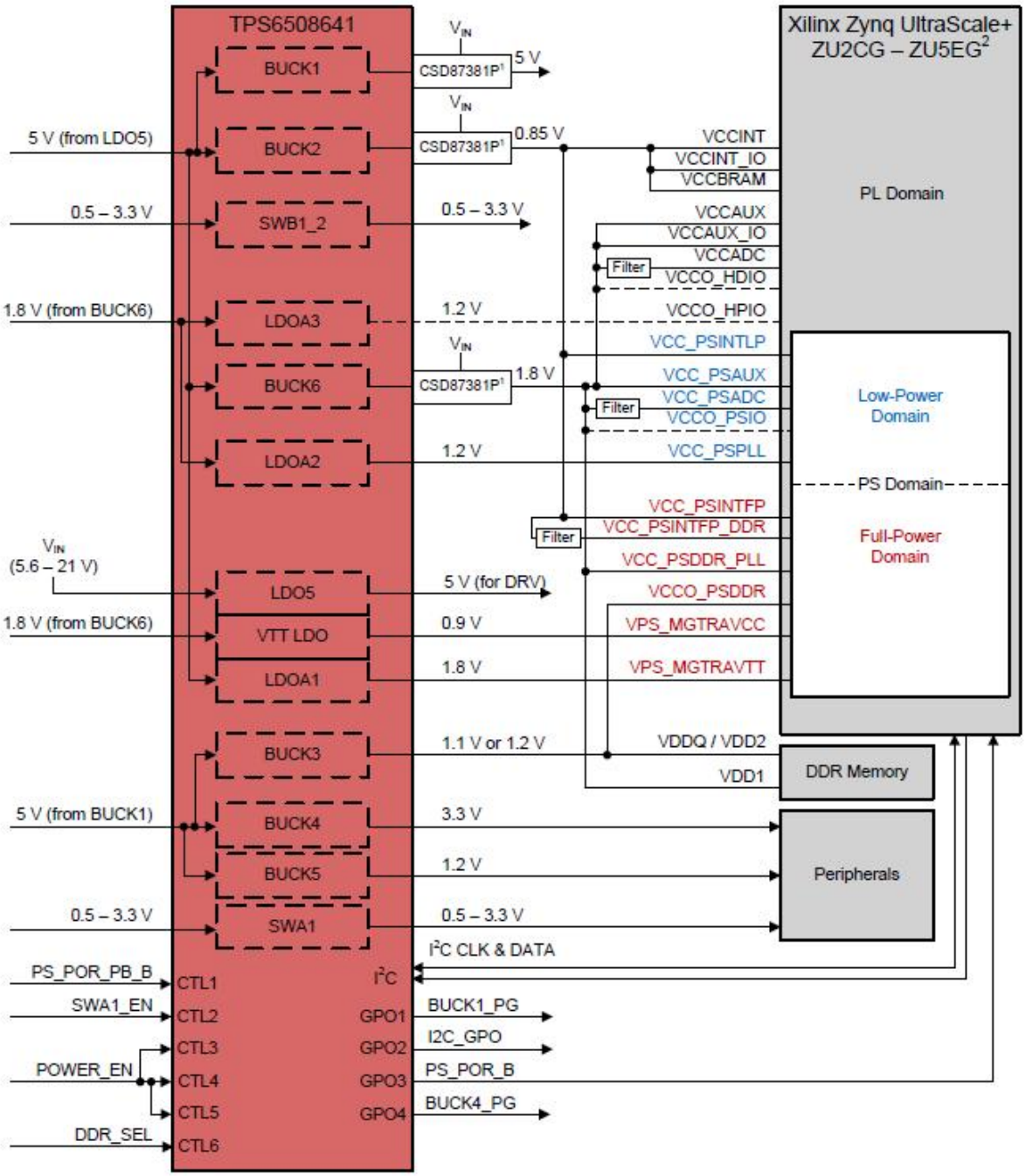
Figure 2-6-4: PL system clock source

Clock pin assignment:

Signal Name	Pin
PL_CLK0_P	AL8
PL_CLK0_N	AL7

Part 2.7: Power Supply

The power supply voltage of the ACU9EG core board is DC12V, which is supplied by connecting the carrier board. The core board uses 2 MYMGM1R824 power chips in parallel to achieve a 50A current to provide the core power of the XCZU9EG with 0.85V. In addition, a PMIC chip TPS6508640 is used to generate all other power supplies required by the XCZU9EG chip. For the TPS6508640 power supply design, please refer to the power supply chip manual. The design block diagram is as follows :


TPS6508641
BUCK1
BUCK2
SWB1_2
LDOA3
BUCK6
LDOA2
LDO5
VTT LDO
LDOA1
BUCK3
BUCK4
BUCK5
SWA1
CTL1
CTL2
CTL3
CTL4
CTL5
CTL6
I²C
GPO1
GPO2
GPO3
GPO4
CSD87381P¹
5 V
0.85 V
0.5 – 3.3 V
1.2 V
1.8 V
5 V (for DRV)
0.9 V
1.1 V or 1.2 V
3.3 V
5 V (from LDO5)
1.8 V (from BUCK6)
5 V (from BUCK1)
VIN (5.6 – 21 V)
PS_POR_PB_B
SWA1_EN
POWER_EN
DDR_SEL
I²C CLK & DATA
BUCK1_PG
I2C_GPO
PS_POR_B
BUCK4_PG
Filter
Xilinx Zynq UltraScale+ ZU2CG – ZU5EG²
PL Domain
VCCINT
VCCINT_IO
VCCBRAM
VCCAUX
VCCAUX_IO
VCCADC
VCCO_HDIO
VCCO_HPIO
VCC_PSINTLP
VCC_PSAUX
VCC_PSADC
VCCO_PSIO
VCC_PSPLL
VCC_PSINTFP
VCC_PSINTFP_DDR
VCC_PSDDR_PLL
VCCO_PSDDR
VPS_MGTRAVCC
VPS_MGTRAVTT
Low-Power Domain
PS Domain
Full-Power Domain
VDDQ / VDD2
VDD1
DDR Memory
Peripherals

Part 2.8: ACU9EG Core Board Size Dimension

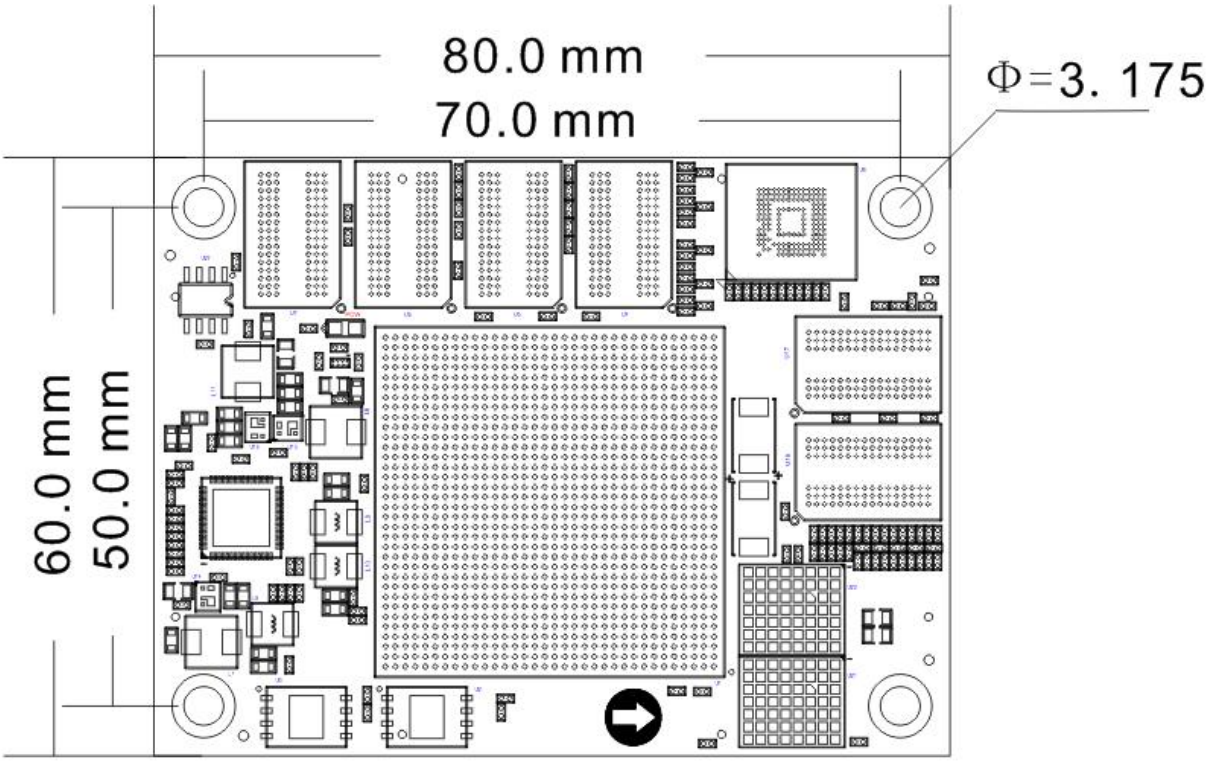


Figure 2-8-1: ACU9EG Core Board Size Dimension

Part 2.9: Board to Board Connectors pin assignment

The core board has a total of four high-speed expansion ports. It uses four 120-pin inter-board connectors (J29/J30/J31/J32) to connect to the carrier board. The connectors used is Panasonic AXK5A2137YG, and the corresponding connector model in the carrier board is Panasonic AXK6A2337YG.

J29 connector

J29 connects the IO of BANK66, BANK67 and the GTX signal of BANK228; the level standard of BANK66, 67 is determined by the VCCO_66 and VCCO_67 power supply of the carrier board, the carrier board provides +1.8V by default.

Pin assignment of board to board connector J29

J29 Pin	Signal Name	Pin Number	J29 Pin	Signal Name	Pin Number
1	-	-	2	-	-
3	B66_L3_P	AA11	4	B67_L1_P	W12
5	B66_L3_N	AA10	6	B67_L1_N	W11
7	B66_L2_P	AB11	8	B66_L7_P	AC7
9	B66_L2_N	AB10	10	B66_L7_N	AC6
11	GND	-	12	GND	-
13	B66_L5_N	AA12	14	B66_L8_P	AB8
15	B66_L5_P	Y12	16	B66_L8_N	AC8
17	B67_L2_N	R13	18	B66_L1_N	AC11
19	B67_L2_P	T13	20	B66_L1_P	AC12
21	GND	-	22	GND	-
23	B66_L19_P	AC2	24	B66_L11_N	Y7
25	B66_L19_N	AC1	26	B66_L11_P	Y8
27	B67_L16_P	N9	28	B67_L6_P	U11
29	B67_L16_N	N8	30	B67_L6_N	T11
31	GND	-	32	GND	-
33	B67_L19_N	K16	34	B66_L14_N	AA5
35	B67_L19_P	L16	36	B66_L14_P	Y5
37	B66_L9_P	W7	38	B66_L21_P	AA2
39	B66_L9_N	W6	40	B66_L21_N	AA1
41	GND	-	42	GND	-
43	B67_L8_P	V6	44	B67_L21_N	N12
45	B67_L8_N	U6	46	B67_L21_P	P12
47	B67_L5_P	V12	48	B67_L24_N	K15
49	B67_L5_N	V11	50	B67_L24_P	L15
51	GND	-	52	GND	-
53	B66_L22_N	Y1	54	B66_L13_P	Y4
55	B66_L22_P	Y2	56	B66_L13_N	Y3
57	B66_L24_N	W1	58	B67_L4_P	T12
59	B66_L24_P	W2	60	B67_L4_N	R12
61	GND	-	62	GND	-
63	B67_L20_P	M15	64	B67_L22_P	N13
65	B67_L20_N	M14	66	B67_L22_N	M13
67	B67_L23_N	K13	68	B67_L17_P	M11

69	B67_L23_P	L13	70	B67_L17_N	L11
71	GND	-	72	GND	-
73	B67_L7_N	V7	74	B67_L13_P	P11
75	B67_L7_P	V8	76	B67_L13_N	N11
77	B67_L9_P	U9	78	B66_L23_N	V1
79	B67_L9_N	U8	80	B66_L23_P	V2
81	GND	-	82	GND	-
83	B67_L18_P	L12	84	B67_L12_P	T8
85	B67_L18_N	K12	86	B67_L12_N	R8
87	B67_L10_P	T7	88	B67_L14_P	P10
89	B67_L10_N	T6	90	B67_L14_N	P9
91	GND	-	92	GND	-
93	228_RX1_N	P1	94	228_RX0_N	T1
95	228_RX1_P	P2	96	228_RX0_P	T2
97	GND	-	98	GND	-
99	228_TX1_N	P5	100	228_TX0_N	R3
101	228_TX1_P	P6	102	228_TX0_P	R4
103	GND	-	104	GND	-
105	228_RX3_N	L3	106	228_RX2_N	M1
107	228_RX3_P	L4	108	228_RX2_P	M2
109	GND	-	110	GND	D1
111	228_TX3_N	M5	112	228_TX2_N	N3
113	228_TX3_P	M6	114	228_TX2_P	N4
115	GND	-	116	GND	-
117	228_CLK0_N	L7	118	228_CLK1_N	J7
119	228_CLK0_P	L8	120	228_CLK1_P	J8

Pin assignment of board to board connector J30

J30 is connected to the transceiver signal of BANK505 MGT, MIO of PS, VCCO_66, VCCO_67 and +12V power supply. The MIO level of PS is 1.8V standard

J29 Pin	Signal Name	Pin Number	J29 Pin	Signal Name	Pin Number
1	505_TX0_P	AB29	2	505_CLK0_P	AA27
3	505_TX0_N	AB30	4	505_CLK0_N	AA28

5	GND	-	6	GND	-
7	505_RX0_P	AB33	8	505_TX3_P	V29
9	505_RX0_N	AB34	10	505_TX3_N	V30
11	GND	-	12	GND	-
13	505_CLK1_P	W27	14	505_TX2_P	W31
15	505_CLK1_N	W28	16	505_TX2_N	W32
17	GND	-	18	GND	-
19	505_RX2_N	Y34	20	505_CLK2_P	U27
21	505_RX2_P	Y33	22	505_CLK2_N	U28
23	GND	-	24	GND	-
25	505_RX3_P	V33	26	505_RX1_N	AA32
27	505_RX3_N	V34	28	505_RX1_P	AA31
29	GND	-	30	GND	-
31	505_CLK3_P	U31	32	505_TX1_N	Y30
33	505_CLK3_N	U32	34	505_TX1_P	Y29
35	GND	-	36	GND	-
37	PS_MIO26	P21	38	USB_STP	G23
39	PS_MIO35	P22	40	USB_DIR	E23
41	GND	-	42	GND	-
43	PS_MIO28	N21	44	USB_CLK	F22
45	PS_MIO37	N22	46	USB_NXT	B23
47	PS_MIO39	N23	48	USB_DATA0	C23
49	PS_MIO27	M21	50	USB_DATA1	A23
51	GND	-	52	GND	-
53	PS_MIO40	M23	54	USB_DATA2	F23
55	PS_MIO30	L21	56	USB_DATA3	B24
57	PS_MIO34	L22	58	USB_DATA4	E24
59	PS_MIO29	K22	60	USB_DATA5	C24
61	GND	-	62	GND	-
63	PS_MIO31	J22	64	USB_DATA6	G24
65	PS_MIO32	H22	66	USB_DATA7	D24
67	PS_MIO42	M24	68	PHY1_MDC	H25
69	PS_MIO36	K23	70	PHY1_MDIO	F25
71	GND	-	72	GND	-
73	PS_MIO33	H23	74	PHY1_TXD0	A26
75	PS_MIO38	L23	76	PHY1_TXD1	A27

77	PS_MIO43	K24	78	PHY1_TXD2	B25
79	PS_MIO41	J24	80	PHY1_TXD3	B26
81	GND	-	82	GND	-
83	PS_MIO44	N24	84	PHY1_TXCK	A25
85	SD_CD	P24	86	PHY1_TXCTL	B27
87	SD_D0	J25	88	PHY1_RXD3	G25
89	SD_D3	K25	90	PHY1_RXD2	H24
91	GND	-	92	GND	-
93	SD_D1	L25	94	PHY1_RXD1	E25
95	SD_D2	M25	96	PHY1_RXD0	C27
97	SD_CLK	N25	98	PHY1_RXCTL	D25
99	SD_CMD	P25	100	PHY1_RXCK	C26
101	GND	-	102	GND	-
103	VCCO_66	-	104	VCCO_67	-
105	VCCO_66	-	106	VCCO_67	-
107	GND	-	108	GND	-
109	+12V	-	110	+12V	-
111	+12V	-	112	+12V	-
113	+12V	-	114	+12V	-
115	+12V	-	116	+12V	-
117	+12V	-	118	+12V	-
119	+12V	-	120	+12V	-

Pin assignment of board to board connector J31

J31 connects the IO of BANK40, BANK50, BANK66, and BANK67. BANK25, BANK26, IO of BANK66 and the GTX signal of BANK505; the level standard of BANK66, 67 is determined by the VCCO_66 and VCCO_67 power supply of the carrier board, the carrier board provides +1.8V by default.

J31 Pin	Signal Name	Pin Number	J31 Pin	Signal Name	Pin Number
			2	FPGA_TCK	R25
3	POWER_SW	-	4	FPGA_TMS	R24
5	PS_MODE3	R23	6	FPGA_TDO	T25
7	PS_MODE2	T23	8	FPGA_TDI	U25

9	GND	-	10	GND	-
11	PS_MODE1	R22	12	VBAT_IN	-
13	PS_MODE0	T22	14	PS_POR_B	V23
15	PS_ERROR_STATUS	R21	16	FPGA_DONE	W21
17	PS_ERROR_OUT	T21	18	GND	-
19	GND	-	20	GND	-
21	B44_L5_P	AK15	22	B50_L11_N	G16
23	B44_L5_N	AK14	24	B50_L11_P	H16
25	B50_L9_P	G15	26	B50_L12_P	J16
27	B50_L9_N	G14	28	B50_L12_N	J15
29	GND	-	30	GND	-
31	B44_L12_P	AE15	32	B50_L10_N	H14
33	B44_L12_N	AE14	34	B50_L10_P	J14
35	B44_L7_P	AH14	36	B44_L8_P	AJ15
37	B44_L7_N	AH13	38	B44_L8_N	AJ14
39	GND	-	40	GND	-
41	B44_L11_N	AG15	42	B44_L6_P	AK13
43	B44_L11_P	AF15	44	B44_L6_N	AL12
45	B44_L1_N	AP14	46	B44_L2_N	AN13
47	B44_L1_P	AN14	48	B44_L2_P	AM14
49	GND	-	50	GND	-
51	B44_L3_N	AP12	-	-	-
53	B44_L3_P	AN12	-	-	-
55	B44_L4_N	AM13	-	-	-
57	B44_L4_P	AL13	-	-	-
59	GND	-	60	GND	-
61	B44_L10_P	AG14	-	-	-
63	B44_L10_N	AG13	-	-	-
65	B50_L8_N	G13	66	B44_L9_N	AF13
67	B50_L8_P	H13	68	B44_L9_P	AE13
69	GND	-	70	GND	-
71	B50_L7_N	H12	72	B50_L6_P	F12
73	B50_L7_P	J12	74	B50_L6_N	F11
75	-	-	76	B50_L5_N	G11
77	-	-	78	B50_L5_P	H11
79	GND	-	80	GND	-

81	B50_L2_P	H10	82	B50_L1_P	J11
83	B50_L2_N	G10	84	B50_L1_N	J10
85	B50_L3_N	E10	86	B50_L4_P	D11
87	B50_L3_P	F10	88	B50_L4_N	D10
89	GND	-	90	GND	-
91	B66_L17_P	V4	92	B66_L15_P	W5
93	B66_L17_N	V3	94	B66_L15_N	W4
95	B66_L12_P	AA7	96	B66_L16_N	AC4
97	B66_L12_N	AA6	98	B66_L16_P	AB4
99	GND	-	100	GND	-
101	B66_L10_P	AB6	102	B66_L20_N	AC3
103	B66_L10_N	AB5	104	B66_L20_P	AB3
105	B66_L4_P	AB9	106	B67_L15_P	M10
107	B66_L4_N	AC9	108	B67_L15_N	L10
109	GND	-	110	GND	-
111	B66_L6_P	Y10	112	B67_L3_P	U10
113	B66_L6_N	Y9	114	B67_L3_N	T10
115	B66_L18_P	U5	116	B67_L11_P	R10
117	B66_L18_N	U4	118	B67_L11_N	R9
119	GND	-	120	GND	-

Pin assignment of board to board connector J32

J32 connects the IO of BANK47, 48, 49 and the transceiver signal of BANK128, 129, 130.

J32 Pin	Signal Name	Pin Number	J32 Pin	Signal Name	Pin Number
1	B48_L5_P	G18	2	B48_L10_N	B19
3	B48_L5_N	G19	4	B48_L10_P	B18
5	B48_L11_P	C18	6	B49_L9_N	A12
7	B48_L11_N	C19	8	B49_L9_P	A13
9	GND	-	10	GND	-
11	B49_L8_N	B13	12	B47_L12_N	A20
13	B49_L8_P	C13	14	B47_L12_P	B20
15	B47_L11_N	A22	16	B49_L4_N	A15
17	B47_L11_P	A21	18	B49_L4_P	B15
19	GND	-	20	GND	-

21	-	-	22	-	-
23	-	-	24	-	-
25	-	-	26	B49_L10_N	B12
27	-	-	28	B49_L10_P	C12
29	-	-	30	-	-
31	GND	-	32	GND	-
33	130_RX3_N	B34	34	130_TX2_N	B30
35	130_RX3_P	B33	36	130_TX2_P	B29
37	GND	-	38	GND	-
39	130_TX3_N	A32	40	130_RX2_N	C32
41	130_TX3_P	A31	42	130_RX2_P	C31
43	GND	-	44	GND	-
45	130_RX0_N	E32	46	130_RX1_N	D34
47	130_RX0_P	E31	48	130_RX1_P	D33
49	GND	-	50	GND	-
51	130_TX0_N	F30	52	130_TX1_N	D30
53	130_TX0_P	F29	54	130_TX1_P	D29
55	GND	-	56	GND	-
57	130_CLK0_N	G28	58	130_CLK1_N	E28
59	130_CLK0_P	G27	60	130_CLK1_P	E27
61	GND	-	62	GND	-
63	129_TX3_N	G32	64	129_RX3_N	F34
65	129_TX3_P	G31	66	129_RX3_P	F33
67	GND	-	68	GND	-
69	129_RX1_N	K34	70	129_TX2_N	H30
71	129_RX1_P	K33	72	129_TX2_P	H29
73	GND	-	74	GND	-
75	129_TX1_N	J32	76	129_RX2_N	H34
77	129_TX1_P	J31	78	129_RX2_P	H33
79	GND	-	80	GND	-
81	129_RX0_N	L32	82	129_TX0_N	K30
83	129_RX0_P	L31	84	129_TX0_P	K29
85	GND	-	86	GND	-
87	129_CLK0_N	L28	88	129_CLK1_N	J28
89	129_CLK0_P	L27	90	129_CLK1_P	J27
91	GND	-	92	GND	-

93	128_TX3_N	M30	94	128_RX3_N	M34
95	128_TX3_P	M29	96	128_RX3_P	M33
97	GND	-	98	GND	-
99	128_TX2_N	P30	100	128_RX1_P	P33
101	128_TX2_P	P29	102	128_RX1_N	P34
103	GND	-	104	GND	-
105	128_TX0_N	T30	106	128_RX0_P	T33
107	128_TX0_P	T29	108	128_RX0_N	T34
109	GND	-	110	GND	-
111	128_TX1_N	R32	112	128_RX2_P	N31
113	128_TX1_P	R31	114	128_RX2_N	N32
115	GND	-	116	GND	-
117	128_CLK0_N	R28	118	128_CLK1_P	N27
119	128_CLK0_P	R27	120	128_CLK1_N	N28

Part 3: Carrier Board

Part 3.1: Carrier Board Introduction

Through the previous function introduction, you can understand the function of the carrier board part

- 1-Channel M.2 interface
- 1-Channel DP output interface
- 4 USB 3.0 Interfaces
- 2-Channel 10/100M/1000M Ethernet RJ-45 interface
- 2-Channel USB Uart Interfaces
- 1-Channel Micro SD card slot
- 1-Channel MIPI camera interface
- 1-Channel FMC interface
- 2-Channel CAN communication interfaces
- 2-Channel 485 communication interfaces
- JTAG debugging interface
- 40-Pin Expansion Header
- 1-Channel temperature sensor
- 1-Channel EEPROM
- 1-Channel RTC real-time clock
- 2 LED lights
- 2 Keys

Part 3.2: M.2 Interface

The AXU9EGB FPGA development board is equipped with a PCIE x1 standard M.2 interface for connecting M.2 SSD solid state drives, with a communication speed of up to 6Gbps. The M.2 interface uses the M key slot, which only supports PCI-E, not SATA. When users choose SSD solid state drives, they need to choose PCIE type SSD solid state drives.

The PCIE signal is directly connected to the BANK505 PS MGT transceiver of ZU9EG, and the TX signal and RX signal of one channel are connected to the LANE1 of MGT in a differential signal mode. The PCIE clock is provided by the Si5332 chip, the frequency is 100Mhz, and the schematic diagram of the M.2 circuit design is shown in Figure 3-2-1:

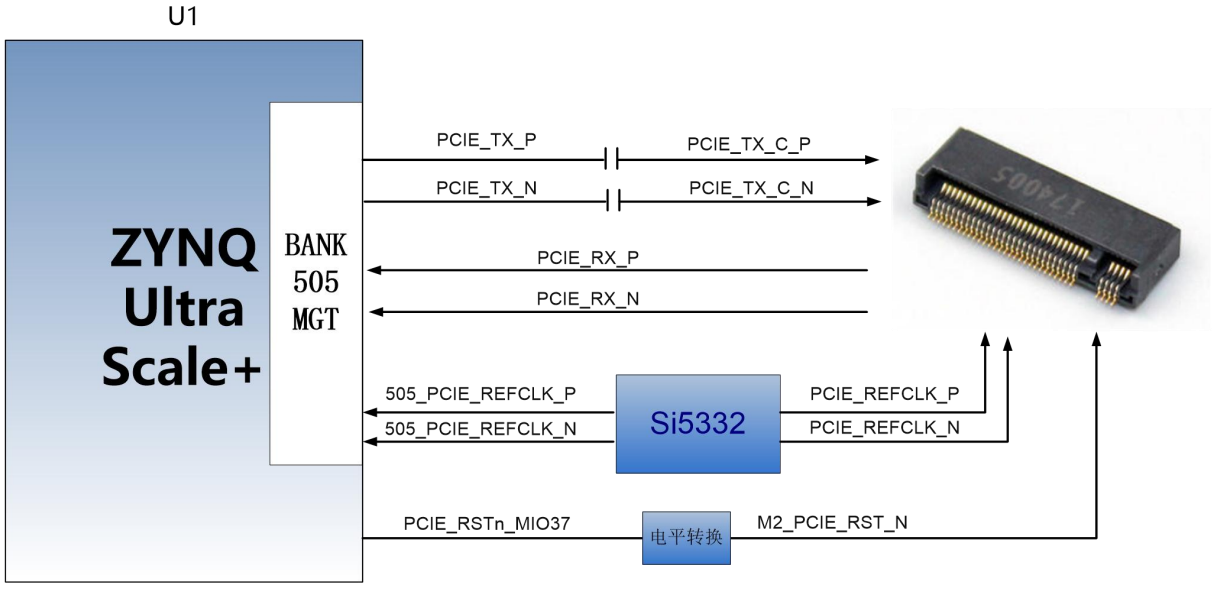


Figure 3-2-1: M.2 Interface Schematic

The pin assignment of M.2 interface ZYNQ is as follows:

Signal Name	Pin Name	Pin Number	Description
PCIE_TX_P	505_TX0_P	AB29	PCIE Data Transmit Positive
PCIE _TX_N	505_TX0_N	AB30	PCIE Data Transmit Negative
PCIE _RX_P	505_RX0_P	AB33	PCIE Data Receive Positive
PCIE _RX_N	505_RX0_N	AB34	PCIE Data Receive Negative
505_PCIE_REFCLK_P	505_CLK0_P	AA27	PCIE Reference Clock Positive
505_PCIE_REFCLK_N	505_CLK0_N	AA28	PCIE Reference Clock Negative
PCIE_RSTn_MIO37	PS_MIO37	N22	PCIE Reset Signal

Part 3.3: DP Interface

The AXU9EGB FPGA development board has a standard DisplayPort output display interface for video image display. The interface supports VESA

DisplayPort V1.2a output standard, up to 4K x 2K@30Fps output, supports Y-only, YCbCr444, YCbCr422, YCbCr420 and RGB video formats, each color supports 6, 8, 10, or 12 bits.

The DisplayPort data transmission channel is directly driven and output by the BANK505 PS MGT of ZU9EG, and the LANE2 and LANE3 TX signals of MGT are connected to the DP connector in a differential signal mode. The DisplayPort auxiliary channel is connected to the MIO pin of the PS. The schematic diagram of the DP output interface design is shown in Figure 3-3-1:

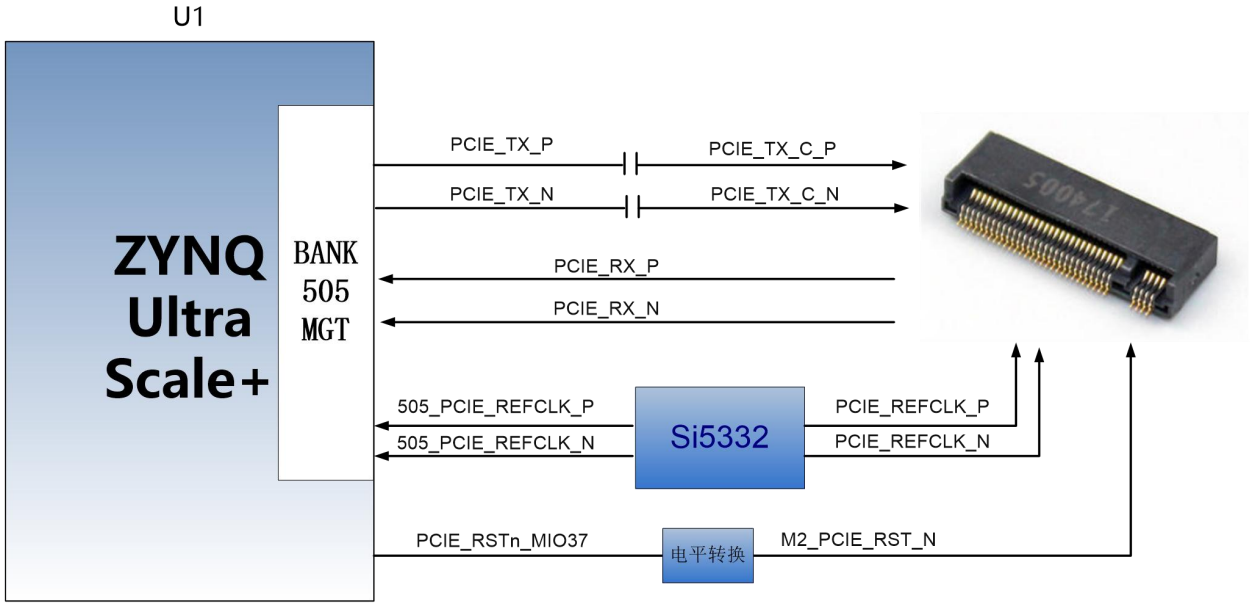


Figure 3-3-1: DP interface design Schematic

The DisplayPort interface ZYNQ pin assignment is as follows:

Signal Name	ZYNQ Pin Number	ZYNQ Pin Number	Description
GT0_DP_TX_P	505_TX3_P	V29	Low bits of DP Data Transmit Positive
GT0_DP_TX_N	505_TX3_N	V30	Low bits of DP Data Transmit Negative
GT1_DP_TX_P	505_TX2_P	W31	High bits of DP Data Transmit Positive
GT1_DP_TX_N	505_TX2_N	W32	High bits of DP Data Transmit Negative
505_DP_CLKP	505_CLK2_P	U27	DP Reference Clock Positive

505_DP_CLKN	505_CLK2_N	U28	DP Reference Clock Negative
DP_AUX_OUT	PS_MIO27	M21	DP Auxiliary Data Output
DP_AUX_IN	PS_MIO30	L21	DP Auxiliary Data Input
DP_OE	PS_MIO29	K22	DP Auxiliary Data Output Enable
DP_HPD	PS_MIO28	N21	DP Insertion Signal Detection

Part 3.4: USB3.0 Interface

There are 4 USB3.0 ports on the AXU9EGB carrier board, supporting the HOST working mode, and the data transmission speed is up to 5.0Gb/s. USB3.0 is connected through the PIPE3 interface, and USB2.0 is connected to the external USB3320C chip through the ULPI interface to realize high-speed USB3.0 and USB2.0 data communication.

The USB interface is a flat USB interface (USB Type A), which is convenient for users to connect different USB Slave peripherals (such as USB mouse, keyboard or U disk) at the same time. The schematic diagram of USB3.0 connection is shown as 3-4-1:

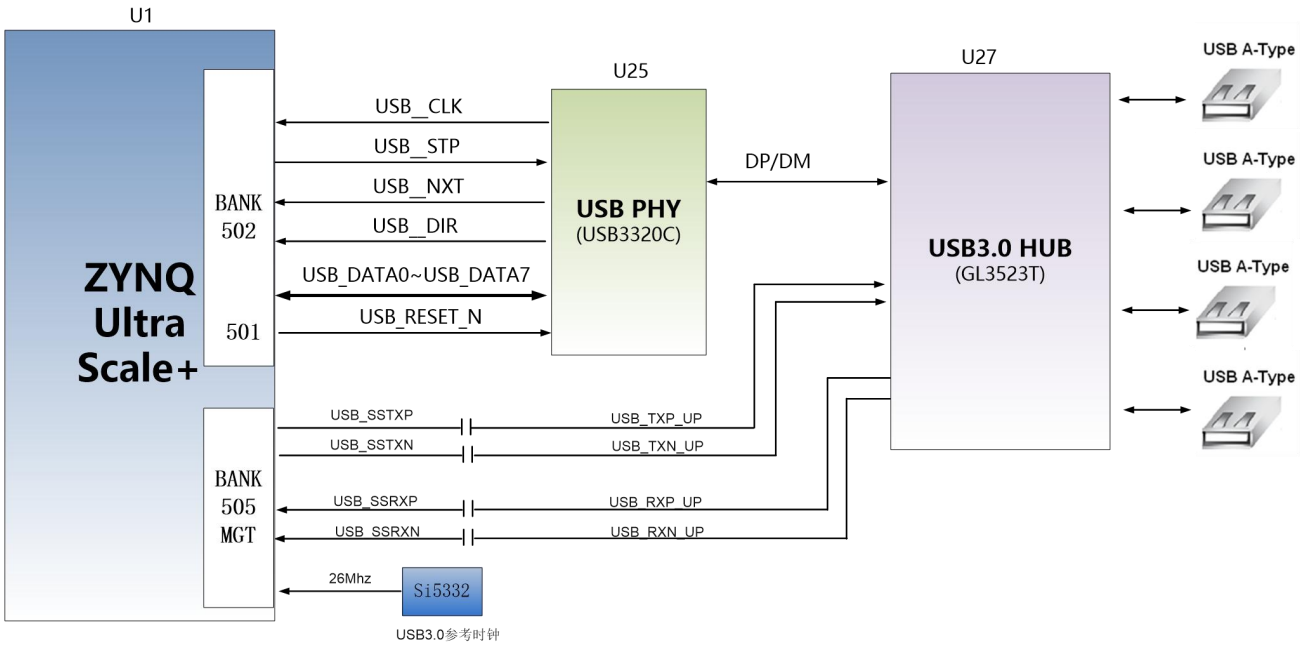


Figure 3-4-1: USB3.0 Interface Schematic

USB Interface Pin Assignment:

Signal Name	Pin Name	Pin Number	Description
USB_SSTXP	505_TX1_P	Y29	USB3.0 Data Transmit Positive
USB_SSTXN	505_TX1_N	Y30	USB3.0 Data Transmit Negative
USB_SSRXP	505_RX1_P	AA31	USB3.0 Data Receive Positive
USB_SSRXN	505_RX1_N	AA32	USB3.0 Data Receive Negative
USB_DATA0	PS_MIO56	C23	USB2.0 Data Bit0
USB_DATA1	PS_MIO57	A23	USB2.0 Data Bit1
USB_DATA2	PS_MIO54	F23	USB2.0 Data Bit2
USB_DATA3	PS_MIO59	B24	USB2.0 Data Bit3
USB_DATA4	PS_MIO60	E24	USB2.0 Data Bit4
USB_DATA5	PS_MIO61	C24	USB2.0 Data Bit5
USB_DATA6	PS_MIO62	G24	USB2.0 Data Bit6
USB_DATA7	PS_MIO63	D24	USB2.0 Data Bit7
USB_STP	PS_MIO58	G23	USB2.0 Stop Signal
USB_DIR	PS_MIO53	E23	USB2.0 Data Direction Signal
USB_CLK	PS_MIO52	F22	USB2.0 Clock Signal
USB_NXT	PS_MIO55	B23	USB2.0 Next Data Signal
USB_RESET_N	PS_MIO32	H22	USB2.0 Reset Signal

Part 3.5: Gigabit Ethernet Interface

There are 2 Gigabit Ethernet ports on the AXU9EGB carrier board, one is connected to the PS end, and the other is connected to the PL end. The GPHY chip uses JLSemi JL2121-N040IRNX Ethernet PHY chip to provide users with network communication services. The Ethernet PHY chip on the PS side is connected to the MIO interface of the BANK502 of the PS side of ZYNQ. The Ethernet PHY chip on the PL side is connected to the IO of the BANK66. The JL2121-N040I chip supports 10/100/1000 Mbps network transmission rate, and communicates with the MAC layer of the ZU9EG system through the RGMII interface. JL2121-N040I supports MDI/MDX adaptation, various speed adaptation, Master/Slave adaptation, and MDIO bus for PHY register management.

When the JL2121-N040IRNX is powered on, it will detect the level status of some specific IOs to determine its own operating mode. Table 3-5-1 describes the default settings after the GPHY chip is powered on.

Configuration Pin	Instructions	Configuration value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	MDIO/MDC Mode PHYaddress	PHY Address 001
RXD1_TXDLY	TX clock 2ns delay	delay
RXD0_RXDLY	RX clock 2ns delay	delay
Configuration Pin	Instructions	Configuration value

Table 3-5-1: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of ZYNQ and PHY chip JL2121-N040I is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising edge and falling samples of the clock.

When the network is connected to 100M Ethernet, the data transmission of ZYNQ and PHY chip JL2121-N040I is communicated through RMII bus, and the transmission clock is 25Mhz. Data is sampled on the rising edge and falling samples of the clock.

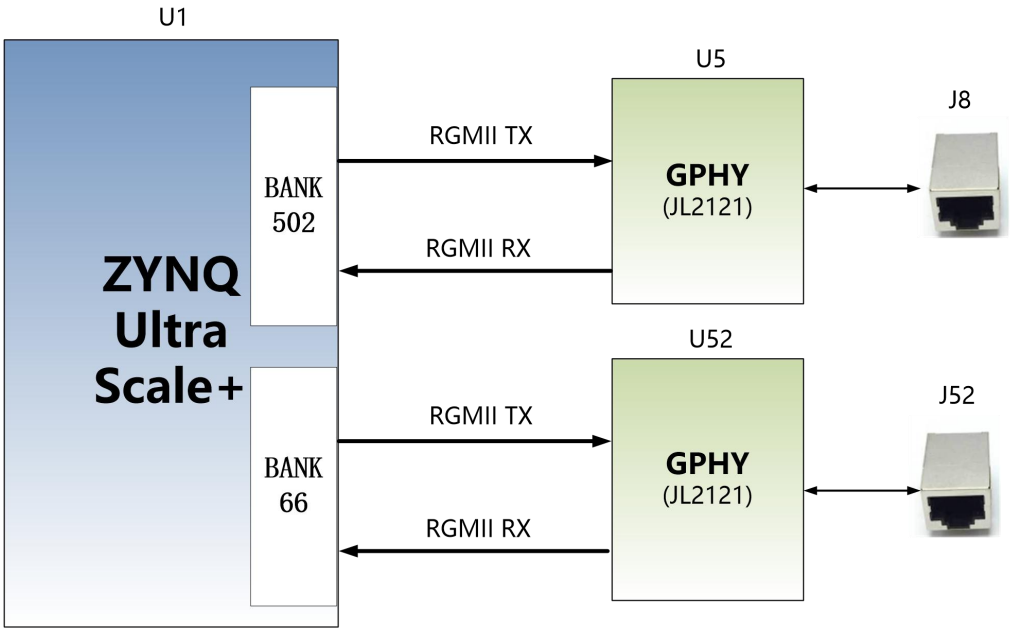


Figure 3-5-1: ZYNQ PS system and GPHY connection diagram

PS Gigabit Ethernet pin assignment is as follows

Signal Name	Pin Name	Pin Number	Description
PHY1_TXCK	PS_MIO64	A25	Ethernet 1 RGMII Transmit Clock
PHY1_TXD0	PS_MIO65	A26	Ethernet 1 Transmit data bit0
PHY1_TXD1	PS_MIO66	A27	Ethernet 1 Transmit data bit1
PHY1_TXD2	PS_MIO67	B25	Ethernet 1 Transmit data bit2
PHY1_TXD3	PS_MIO68	B26	Ethernet 1 Transmit data bit3
PHY1_TXCTL	PS_MIO69	B27	Ethernet 1 Transmit Enable Signal
PHY1_RXCK	PS_MIO70	C26	Ethernet 1 RGMII Receive Clock
PHY1_RXD0	PS_MIO71	C27	Ethernet 1 Receive Data Bit0
PHY1_RXD1	PS_MIO72	E25	Ethernet 1 Receive Data Bit1
PHY1_RXD2	PS_MIO73	H24	Ethernet 1 Receive Data Bit2
PHY1_RXD3	PS_MIO74	G25	Ethernet 1 Receive Data Bit3
PHY1_RXCTL	PS_MIO75	D25	Ethernet 1 Receive Enable Signal
PHY1_MDC	PS_MIO76	H25	Ethernet 1 MDIO Clock Management
PHY1_MDIO	PS_MIO77	F25	Ethernet 1 MDIO Management Data

PL Gigabit Ethernet pin assignment is as follows

Signal Name	Pin Name	Pin Number	Description
PHY2_TXCK	B66_L17_N	V3	Ethernet 2 RGMII Transmit Clock
PHY2_TXD0	B66_L4_N	AC9	Ethernet 2 Transmit data bit0
PHY2_TXD2	B66_L10_N	AB5	Ethernet 2 Transmit data bit1
PHY2_TXD1	B66_L4_P	AB9	Ethernet 2 Transmit data bit2
PHY2_TXD3	B66_L10_P	AB6	Ethernet 2 Transmit data bit3
PHY2_TXCTL	B66_L17_P	V4	Ethernet 2 Transmit Enable Signal
PHY2_RXCK	B66_L12_P	AA7	Ethernet 2 RGMII Transmit Clock
PHY2_RXD0	B66_L18_N	U4	Ethernet 2 Receive Data Bit0
PHY2_RXD1	B66_L18_P	U5	Ethernet 2 Receive Data Bit1
PHY2_RXD2	B66_L6_N	Y9	Ethernet 2 Receive Data Bit2
PHY2_RXD3	B66_L6_P	Y10	Ethernet 2 Receive Data Bit3
PHY2_RXCTL	B66_L12_N	AA6	Ethernet 2 Receive Enable Signal
PHY2_MDC	B67_L15_P	M10	Ethernet 2 MDIO Clock Management
PHY2_MDIO	B67_L15_N	L10	Ethernet 2 MDIO Management Data
PHY2_RESET	B67_L11_N	R9	Ethernet 2 Reset Signal

Part 3.6: USB to Serial Port

The AXU9EGB carrier board is equipped with two Uart to USB ports, one is connected to the PS end, and one is connected to the PL end.

The conversion chip uses Silicon Labs CP2102GM's USB-UAR chip, and the USB interface is a MINI USB interface. You can use a USB cable to connect it to the PC's USB port for serial data communication. The schematic diagram of the USB Uart circuit design is shown in the figure below:

The schematic diagram of the USB Uart circuit design is shown in Figure 3-6-1:

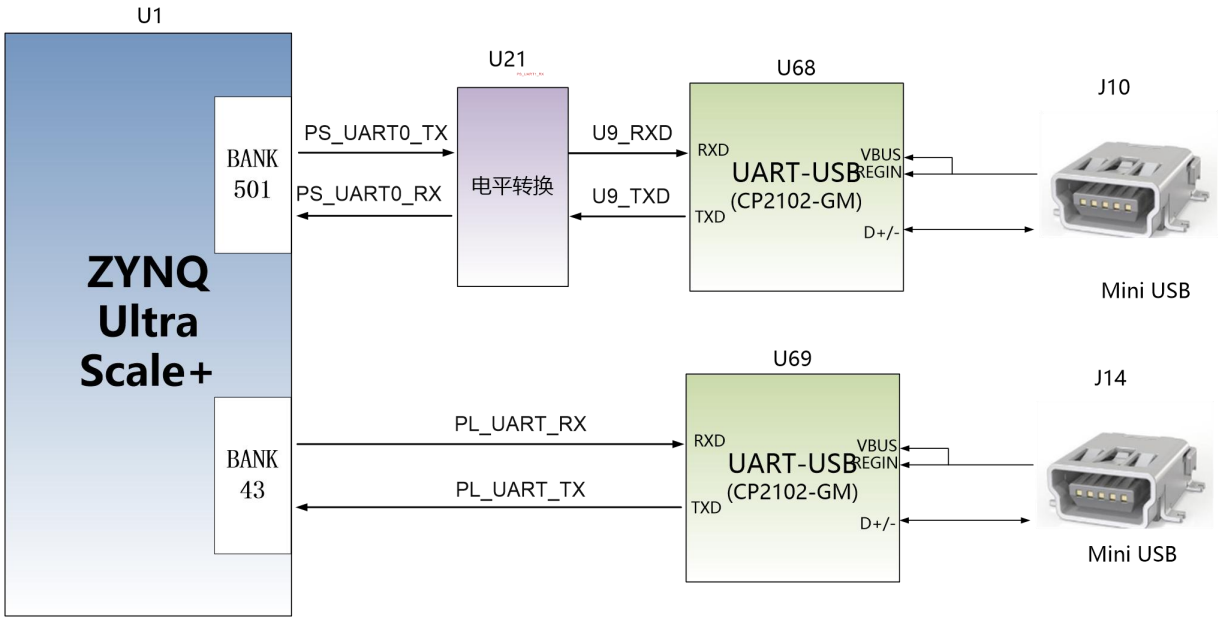


Figure 3-6-1: USB to serial port schematic

USB to serial port ZYNQ pin assignment:

Signal name	Pin Name	Pin Number	Description
PS_UART_TX	PS_MIO43	K24	PS Uart Data Output
PS_UART_RX	PS_MIO42	M24	PS Uart Data Input
PL_UART_TX	B50_L4_P	D10	PL Uart Data Output
PL_UART_RX	B50_L4_N	D10	PL Uart Data Input

Part 3.7: SD Card Slot Interface

The AXU9EGB FPGA Development Board contains a Micro SD card interface to provide user access to the SD card memory, the BOOT program for the ZU9EG chip, the Linux operating system kernel, the file system and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of ZU9EG. Since the VCCMIO of the BANK is set to 1.8V, but the data level of the SD card is 3.3V, connected through the TXS02612 level shifter. The schematic of the ZU9EG PS and SD card connector is shown in Figure 3-7-1:

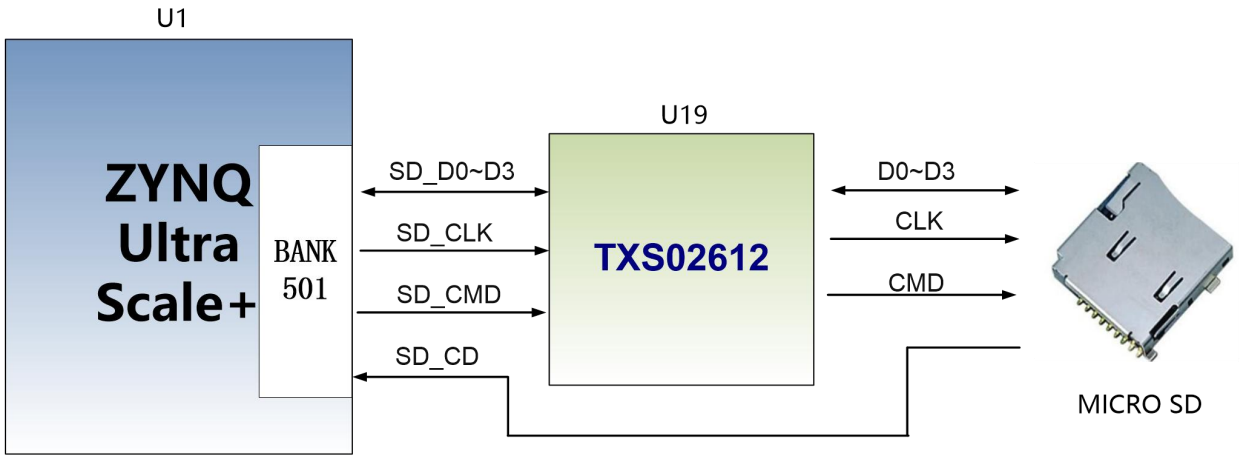


Figure 3-7-1: SD Card Connection Diagram

SD card slot pin assignment:

Signal Name	Pin Name	Pin Number	Description
SD_CMD	SD_CMD	P25	SD Clock Signal
SD_CD	SD_CD	P24	SD Command Signal
SD_D0	SD_D0	J25	SD Data0
SD_D1	SD_D1	L25	SD Data1
SD_D2	SD_D2	M25	SD Data2
SD_D3	SD_D3	K25	SD Data3
SD_CMD	SD_CMD	P25	SD card insertion signal

Part 3.8: SFP Interface

The AXU9EGB FPGA carrier board has two optical interfaces. Users can purchase SFP optical modules (1.25G, 2.5G, 10G optical modules on the market) and insert them into these two optical interfaces for optical data communication. The two fiber interfaces are connected to the two RX/TX of the GNK transceiver of ZYNQ BANK228, and the data rate of each TX transmission and RX reception is up to 12.5Gb/s. The reference clock of the GTH transceiver is provided by the 125M differential clock of the core board.

The SFP Schematic detailed is shown in Figure 3-8-1:

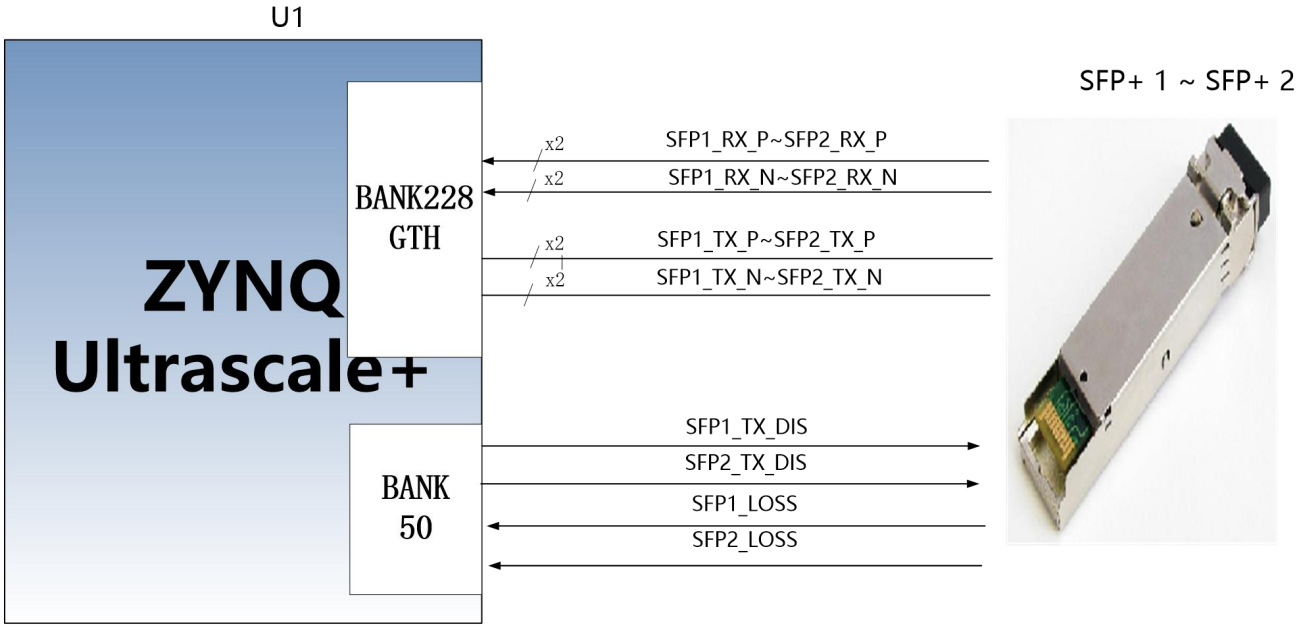


Figure 3-8-1: SFP Schematic

SFP ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
SFP1_TX_N	228_TX2_N	N3	Optical Module 1 Data Transmit Negative
SFP1_TX_P	228_TX2_P	N4	Optical Module 1 Data Transmit Positive
SFP1_RX_N	228_RX2_N	M1	Optical Module 1 Data Receive Negative
SFP1_RX_P	228_RX2_P	M2	Optical Module 1 Data Receive Positive
SFP2_TX_N	228_TX0_N	R3	Optical Module 2 Data Transmit Negative
SFP2_TX_P	228_TX0_P	R4	Optical Module 2 Data Transmit Positive
SFP2_RX_N	228_RX0_N	T1	Optical Module 2 Data Receive Negative
SFP2_RX_P	228_RX0_P	T2	Optical Module 2 Data Receive Positive
SFP1_TX_DIS	B50_L8_N	G13	Optical Module 1 Light Emission Prohibited, High Level (Positive) Enable
SFP2_TX_DIS	B50_L7_N	H12	Optical Module 2 Light Emission Prohibited, High Level (Positive) Enable
SFP1_LOSS	B50_L8_P	H13	Optical Module 1 Receive LOSS Detect Signal
SFP2_LOSS	B50_L7_P	J12	Optical Module 2 Receive LOSS Detect Signal

Part 3.9: CAN Communication Interface

There are 2 CAN communication interfaces on the AXU9EGB carrier board, which are connected to the MIO interface of the BANK501 on the PS system side. The CAN transceiver chip selected TI's SN65HVD232C chip for user CAN communication services. The connection of the CAN transceiver chip on the PS side is show as Figure 3-9-1

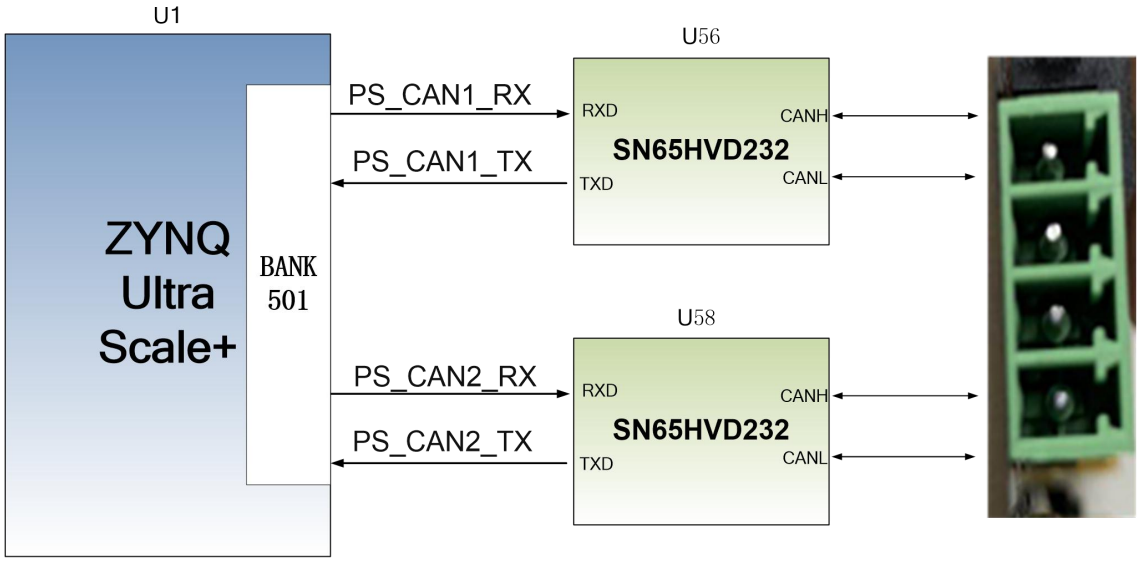


Figure 3-9-1: Connection diagram of CAN transceiver chip on PS side

The CAN communication pin assignments are as follows:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_CAN1_TX	PS_MIO39	N23	CAN1 Transmitter
PS_CAN1_RX	PS_MIO38	L23	CAN1 Receiver
PS_CAN2_TX	PS_MIO40	M23	CAN2 Transmitter
PS_CAN2_RX	PS_MIO41	J24	CAN2 Receiver

Part 3.10: 485 Communication Interface

There are two 485 communication interfaces on the AXU9EGB carrier board. The 485 communication port 1 is connected to the IO interface of

BANK43~45 on the PL system. The 485 transceiver chip selects the MAX3485 chip from MAXIM for the user's 485 communication service.

Figure 3-10-1 is the connection diagram of the 485 transceiver chip on the PL side

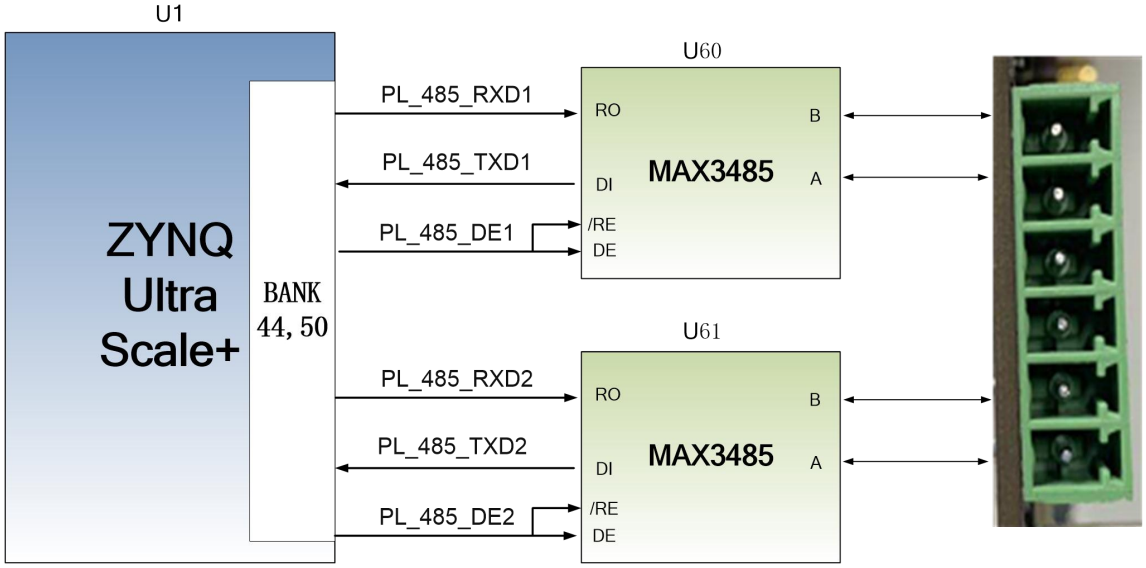


Figure 3-10-1: 485 Communication on the PL Side

The 485 communication pins are assigned as follows:

Signal Name	Pin Name	Pin Number	Description
PL_485_TXD1	B44_L10_N	AG13	The 1st Channel 485 Transceiver
PL_485_RXD1	B44_L4_P	AL13	The 1st Channel 485 Receiver
PL_485_DE1	B44_L10_P	AG14	The 1st Channel 485 Transmit Enable
PL_485_TXD2	B50_L1_P	J11	The 2nd Channel 485 Transceiver
PL_485_RXD2	B50_L5_N	G11	The 2nd Channel 485 Receiver
PL_485_DE2	B50_L5_P	H11	The 2nd Channel 485 Transmit Enable

Part 3.11: MIPI Camera Interface

The AXU9EGB carrier board includes a MIPI camera interface, which can be used to connect with the ALINX Brand MIPI OV5640 camera module AN5641. MIPI interface 15PIN FPC connector, 2 LANE data and 1 pair of clock, connected to the differential IO pin of BANK67, other control signals are

connected to the IO of BANK43, level standard It is 3.3V.

The circuit schematic of the MIPI interface part is shown in Figure 3-14-1 below:

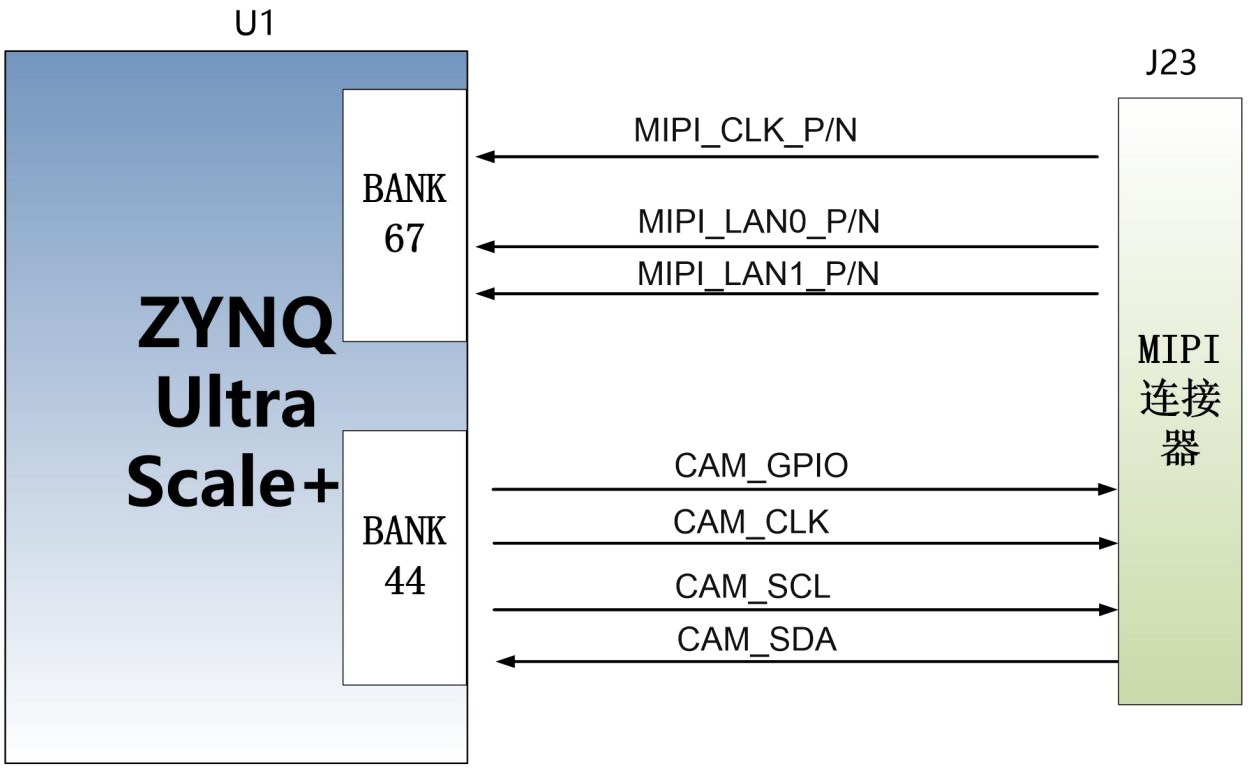


Figure 3-14-1: MIPI camera interface design schematic

MIPI interface pin assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
MIPI_CLK_P	B67_L1_P	W12	MIPI Input Clock Positive
MIPI_CLK_N	B67_L1_N	W11	MIPI Input Clock Negative
MIPI_LAN0_P	B67_L2_P	T13	MIPI Input Date LANE0 Positive
MIPI_LAN0_N	B67_L2_N	R13	MIPI Input Date LANE0 Negative
MIPI_LAN1_P	B67_L3_P	U10	MIPI Input Date LANE1 Positive
MIPI_LAN1_N	B67_L3_N	T10	MIPI Input Date LANE1 Negative
CAM_GPIO	B44_L6_P	AK13	GPIO Control of Camera
CAM_CLK	B44_L6_N	AL12	Clock Input of Camera

CAM_SCL	B44_L2_N	AN13	I2C Clock of Camera
CAM_SDA	B44_L2_P	AM14	I2C Data of Camera

Part 3.12: FMC Interface

The AXU9EGB FPGA Carrier board has a standard FMC HPC expansion port that can be connected to various FMC modules of XILINX or ALINX (HDMI input and output modules, binocular camera modules, high-speed AD modules, etc.). The FMC expansion port contains 36 pairs of differential IO signals and 8 pairs of GTX Transceivers.

The 36 pairs of differential signals of the FMC expansion port are connected to the IO of the BANK66 and BANK67 of the ZYNQ Ultrascale+ chip. The level standard is 1.8V, and the differential signal supports LVDS data communication, 8 pairs of GTX transceiver signals are connected to BANK129 and BANK130. The schematic diagram of ZYNQ Ultrascale+ and FMC connectors is shown in Figure 3-12-1.

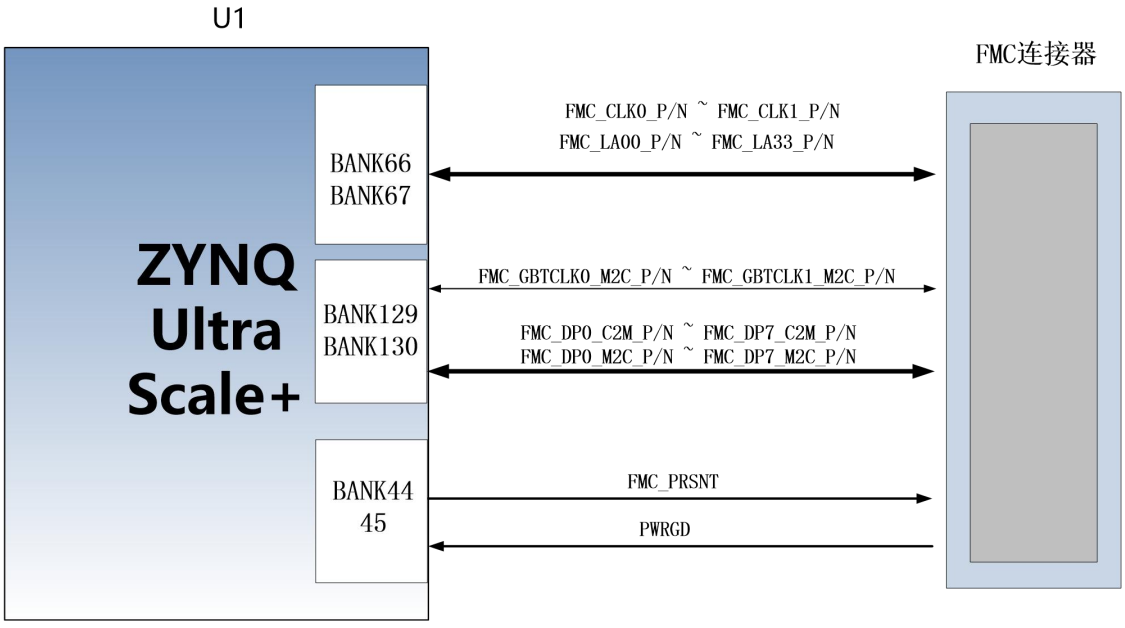


Figure 3-12-1: FMC Schematic

FMC connector pin assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin	Description

		Number	
FMC_GBTCLK0_M2C_P	130_CLK0_P	G27	FMC Transceiver Reference Clock 0 Positive
FMC_GBTCLK0_M2C_N	130_CLK0_N	G28	FMC Transceiver Reference Clock 0 Negative
FMC_GBTCLK1_M2C_P	129_CLK0_P	L27	FMC Transceiver Reference Clock 1 Positive
FMC_GBTCLK1_M2C_N	129_CLK0_N	L28	FMC Transceiver Reference Clock 1 Negative
FMC_DP0_C2M_P	130_TX0_P	F29	FMC Transceiver Data Transmission 0 Positive
FMC_DP0_C2M_N	130_TX0_N	F30	FMC Transceiver Data Transmission 0 Negative
FMC_DP1_C2M_P	130_TX1_P	D29	FMC Transceiver Data Transmission 1 Positive
FMC_DP1_C2M_N	130_TX1_N	D30	FMC Transceiver Data Transmission 1 Negative
FMC_DP2_C2M_P	130_TX2_P	B29	FMC Transceiver Data Transmission 2 Positive
FMC_DP2_C2M_N	130_TX2_N	B30	FMC Transceiver Data Transmission 2 Negative
FMC_DP3_C2M_P	130_TX3_P	A31	FMC Transceiver Data Transmission 3 Positive
FMC_DP3_C2M_N	130_TX3_N	A32	FMC Transceiver Data Transmission 3 Negative
FMC_DP4_C2M_P	129_TX0_P	K29	FMC Transceiver Data Transmission 4 Positive
FMC_DP4_C2M_N	129_TX0_N	K30	FMC Transceiver Data Transmission 4 Negative
FMC_DP5_C2M_P	129_TX1_P	J31	FMC Transceiver Data Transmission 5 Positive
FMC_DP5_C2M_N	129_TX1_N	J32	FMC Transceiver Data Transmission 5 Negative
FMC_DP6_C2M_P	129_TX2_P	H29	FMC Transceiver Data Transmission 6 Positive
FMC_DP6_C2M_N	129_TX2_N	H30	FMC Transceiver Data Transmission 6 Negative

FMC_DP7_C2M_P	129_TX3_P	G31	FMC Transceiver Data Transmission 7 Positive
FMC_DP7_C2M_N	129_TX3_N	G32	FMC Transceiver Data Transmission 7 Negative
FMC_DP0_M2C_P	130_RX0_P	E31	FMC Transceiver Data Receive 0 Positive
FMC_DP0_M2C_N	130_RX0_N	E32	FMC Transceiver Data Receive 0 Negative
FMC_DP1_M2C_P	130_RX1_P	D33	FMC Transceiver Data Receive 1 Positive
FMC_DP1_M2C_N	130_RX1_N	D34	FMC Transceiver Data Receive 1 Negative
FMC_DP2_M2C_N	130_RX2_N	C32	FMC Transceiver Data Receive 2 Positive
FMC_DP2_M2C_P	130_RX2_P	C31	FMC Transceiver Data Receive 2 Negative
FMC_DP3_M2C_P	130_RX3_P	B33	FMC Transceiver Data Receive 3 Positive
FMC_DP3_M2C_N	130_RX3_N	B34	FMC Transceiver Data Receive 3 Negative
FMC_DP4_M2C_P	129_RX0_P	L31	FMC Transceiver Data Receive 4 Positive
FMC_DP4_M2C_N	129_RX0_N	L32	FMC Transceiver Data Receive 4 Negative
FMC_DP5_M2C_P	129_RX1_P	K33	FMC Transceiver Data Receive 5 Positive
FMC_DP5_M2C_N	129_RX1_N	K34	FMC Transceiver Data Receive 5 Negative
FMC_DP6_M2C_P	129_RX2_P	H33	FMC Transceiver Data Receive 6 Positive
FMC_DP6_M2C_N	129_RX2_N	H34	FMC Transceiver Data Receive 6 Negative
FMC_DP7_M2C_P	129_RX3_P	F33	FMC Transceiver Data Receive 7 Positive
FMC_DP7_M2C_N	129_RX3_N	F34	FMC Transceiver Data Receive 7 Negative
FMC_CLK0_P	B67_L14_P	P10	FMC Reference 1st Clock P

FMC_CLK0_N	B67_L14_N	P9	FMC Reference 1st Clock N
FMC_CLK1_P	B66_L13_P	Y4	FMC Reference 2nd Clock P
FMC_CLK1_N	B66_L13_N	Y3	FMC Reference 2nd Clock N
FMC_LA00_CC_P	B67_L12_P	T8	FMC Reference 0th Data (Clock) P
FMC_LA00_CC_N	B67_L12_N	R8	FMC Reference 0th Data (Clock) N
FMC_LA01_CC_P	B67_L13_P	P11	FMC Reference 1st Data (Clock) P
FMC_LA01_CC_N	B67_L13_N	N11	FMC Reference 1st Data (Clock) N
FMC_LA02_P	B67_L10_P	T7	FMC Reference 2nd Data P
FMC_LA02_N	B67_L10_N	T6	FMC Reference 2nd Data N
FMC_LA03_P	B67_L18_P	L12	FMC Reference 3rd Data P
FMC_LA03_N	B67_L18_N	K12	FMC Reference 3rd Data N
FMC_LA04_P	B67_L23_P	L13	FMC Reference 4th Data P
FMC_LA04_N	B67_L23_N	K13	FMC Reference 4th Data N
FMC_LA05_P	B67_L22_P	N13	FMC Reference 5th Data P
FMC_LA05_N	B67_L22_N	M13	FMC Reference 5th Data N
FMC_LA06_P	B67_L17_P	M11	FMC Reference 6th Data P
FMC_LA06_N	B67_L17_N	L11	FMC Reference 6th Data N
FMC_LA07_P	B67_L8_P	V6	FMC Reference 7th Data P
FMC_LA07_N	B67_L8_N	U6	FMC Reference 7th Data N
FMC_LA08_P	B67_L20_P	M15	FMC Reference 8th Data P
FMC_LA08_N	B67_L20_N	M14	FMC Reference 8th Data N
FMC_LA09_P	B67_L7_P	V8	FMC Reference 9th Data P
FMC_LA09_N	B67_L7_N	V7	FMC Reference 9th Data N
FMC_LA10_P	B67_L4_P	T12	FMC Reference 10th Data P
FMC_LA10_N	B67_L4_N	R12	FMC Reference 10th Data N
FMC_LA11_P	B67_L9_P	U9	FMC Reference 11th Data P
FMC_LA11_N	B67_L9_N	U8	FMC Reference 11th Data N
FMC_LA12_P	B67_L24_P	L15	FMC Reference 12th Data P
FMC_LA12_N	B67_L24_N	K15	FMC Reference 12th Data N
FMC_LA13_P	B67_L19_P	L16	FMC Reference 13th Data P
FMC_LA13_N	B67_L19_N	K16	FMC Reference 13th Data N
FMC_LA14_P	B67_L21_P	P12	FMC Reference 14th Data P
FMC_LA14_N	B67_L21_N	N12	FMC Reference 14th Data N
FMC_LA15_P	B67_L5_P	V12	FMC Reference 15th Data P
FMC_LA15_N	B67_L5_N	V11	FMC Reference 15th Data N
FMC_LA16_P	B67_L16_P	N9	FMC Reference 16th Data P

FMC_LA16_N	B67_L16_N	N8	FMC Reference 16th Data N
FMC_LA17_CC_P	B66_L14_P	Y5	FMC Reference 17th Data (Clock) P
FMC_LA17_CC_N	B66_L14_N	AA5	FMC Reference 17th Data (Clock) N
FMC_LA18_CC_P	B66_L11_P	Y8	FMC Reference 18th Data (Clock) P
FMC_LA18_CC_N	B66_L11_N	Y7	FMC Reference 18th Data (Clock) N
FMC_LA19_P	B66_L21_P	AA2	FMC Reference 19th Data P
FMC_LA19_N	B66_L21_N	AA1	FMC Reference 19th Data N
FMC_LA20_P	B66_L23_P	V2	FMC Reference 20th Data P
FMC_LA20_N	B66_L23_N	V1	FMC Reference 20th Data N
FMC_LA21_P	B66_L22_P	Y2	FMC Reference 21st Data P
FMC_LA21_N	B66_L22_N	Y1	FMC Reference 21st Data N
FMC_LA22_P	B66_L9_P	W7	FMC Reference 22nd Data P
FMC_LA22_N	B66_L9_N	W6	FMC Reference 22nd Data N
FMC_LA23_P	B66_L24_P	W2	FMC Reference 23rd Data P
FMC_LA23_N	B66_L24_N	W1	FMC Reference 23rd Data N
FMC_LA24_P	B66_L8_P	AB8	FMC Reference 24th Data P
FMC_LA24_N	B66_L8_N	AC8	FMC Reference 24th Data N
FMC_LA25_P	B66_L5_P	Y12	FMC Reference 25th Data P
FMC_LA25_N	B66_L5_N	AA12	FMC Reference 25th Data N
FMC_LA26_P	B66_L19_P	AC2	FMC Reference 26th Data P
FMC_LA26_N	B66_L19_N	AC1	FMC Reference 26th Data N
FMC_LA27_P	B66_L1_P	AC12	FMC Reference 27th Data P
FMC_LA27_N	B66_L1_N	AC11	FMC Reference 27th Data N
FMC_LA28_P	B66_L2_P	AB11	FMC Reference 28th Data P
FMC_LA28_N	B66_L2_N	AB10	FMC Reference 28th Data N
FMC_LA29_P	B66_L7_P	AC7	FMC Reference 29th Data P
FMC_LA29_N	B66_L7_N	AC6	FMC Reference 29th Data N
FMC_LA30_P	B66_L16_P	AB4	FMC Reference 30th Data P
FMC_LA30_N	B66_L16_N	AC4	FMC Reference 30th Data N
FMC_LA31_P	B66_L3_P	AA11	FMC Reference 31st Data P
FMC_LA31_N	B66_L3_N	AA10	FMC Reference 31st Data N
FMC_LA32_P	B66_L20_P	AB3	FMC Reference 32nd Data P
FMC_LA32_N	B66_L20_N	AC3	FMC Reference 32nd Data N
FMC_LA33_P	B66_L15_P	W5	FMC Reference 33rd Data P
FMC_LA33_N	B66_L15_N	W4	FMC Reference 33rd Data N
FMC_PRSNT	B50_L3_P	F10	FMC Module Exist Signal

PWRGD	B50_L3_N	E10	FMC Power Good Signal
FMC_HDMI_SDA	B50_L2_P	H10	FMC I2C Communication Data
FMC_HDMI_SCL	B50_L2_N	G10	FMC I2C Communication Clock

Part 3.13: 40-Pin Expansion Headers

The carrier board is reserved with one 0.1inch spacing standard 40-pin expansion ports J50, which is used to connect the ALINX modules or the external circuit designed by the user. The expansion port has 40 signals, of which 1-channel 5V power supply, 2-channel 3.3 V power supply, 3-channle ground and 34 IOs. The IO of the expansion port is connected to the IO of the PL end of the ZYNQ chip, and the level standard is 3.3V.

J50 Expansion Header Pin Assignment

J50 Pin	Signal Name	Pin Number	J50 Pin	Signal Name	Pin Number
1	GND	-	2	+5V	-
3	IO_1N	G19	4	IO_1P	G18
5	IO_2N	B19	6	IO_2P	B18
7	IO_3N	C19	8	IO_3P	C18
9	IO_4N	A12	10	IO_4P	A13
11	IO_5N	B13	12	IO_5P	C13
13	IO_6N	A20	14	IO_6P	B20
15	IO_7N	A15	16	IO_7P	B15
17	IO_8N	A22	18	IO_8P	A21
19	IO_9N	B12	20	IO_9P	C12
21	IO_10N	AG15	22	IO_10P	AF15
23	IO_11N	AE14	24	IO_11P	AE15
25	IO_12N	G14	26	IO_12P	G15
27	IO_13N	AK14	28	IO_13P	AK15
29	IO_14N	AH13	30	IO_14P	AH14
31	IO_15N	AP14	32	IO_15P	AN14
33	IO_16N	G16	34	IO_16P	H16
35	IO_17N	J15	36	IO_17P	J16
37	GND	-	38	GND	-

39	+3.3V	-	40	+3.3V	-

Part 3.14: JTAG Debug Port

The JTAG interface is reserved on the AXU9EGB expansion board for downloading ZYNQ UltraScale+ programs or firmware programs to FLASH. In order to not damage the ZYNQ UltraScale+ chip by plugging and unplugging under power, we aded a protection diode to the JTAG signal to ensure that the signal voltage is within the range accepted by the FPGA and avoid damage to the ZYNQ UltraScale+ chip.

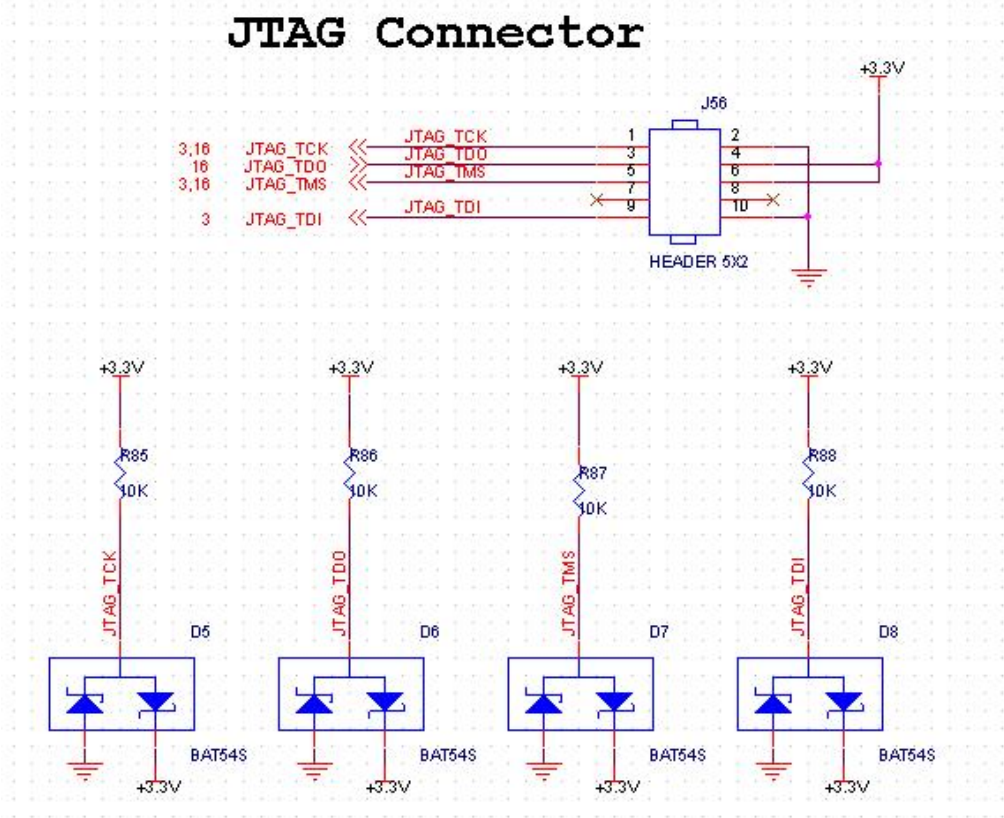


Figure 3-14-1: JTAG Interface Schematic

Part 3.15: Real-time Clock

The ZU9EG chip has the function of an RTC real-time clock, with timing functions such as year, month, day, hour, minute, and second, and week. External need to connect a 32.768KHz passive clock to provide an accurate clock source to the internal clock circuit, so that the RTC can accurately provide

clock information. At the same time, in order for the real-time clock to operate normally after the product is powered off, it is generally necessary to equip the coin battery (**model LR1130, voltage is 5V**) to supply power to the clock chip. The BT1 on the development board is a battery Socket. After we put the coin battery, even the system is off, the coin battery can also power the RTC system and provide continuous time information.

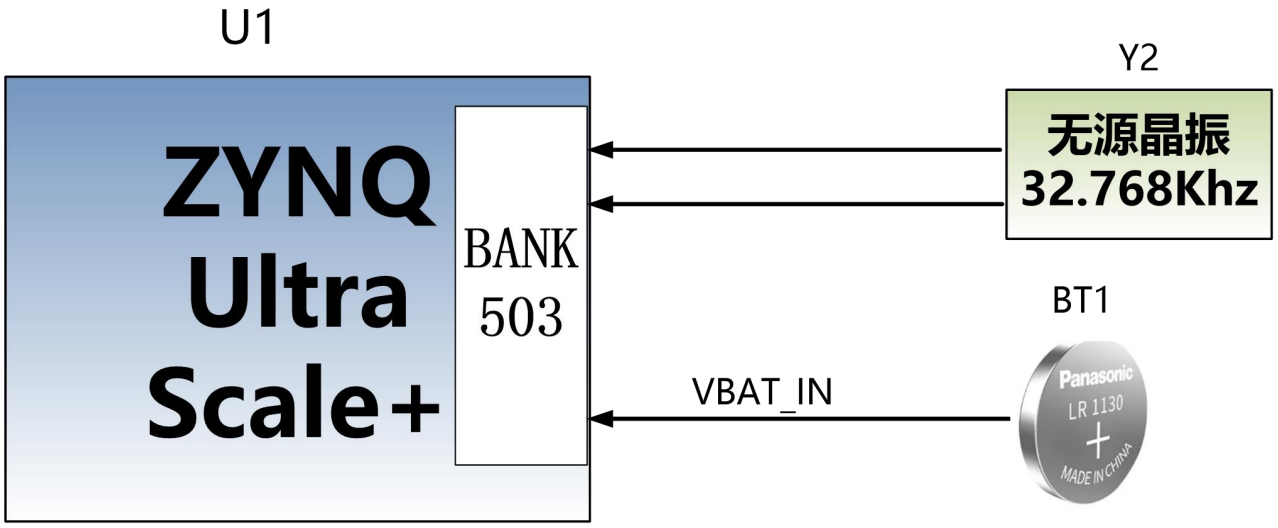


Figure 3-15-1: RTC Schematic

Part 3.16: EEPROM and Temperature Sensor

The AXU9EGB Fpga development board has an EEPROM onboard. The model of the EEPROM is 24LC04, and the capacity is: 4Kbit (2 * 256 * 8bit), which is connected to the PS terminal through the I2C bus.

A high-precision, low-power, digital temperature sensor chip is installed on the AXU9EGB FPGA development board, and the model is LM75 from ON Semiconductor. The temperature accuracy of the LM75 chip is 0.5 degrees.

The EEPROM and temperature sensor are mounted on the Bank500 MIO of ZYNQ UltraScale+ through the I2C bus. Figure 3-16-1 is the schematic diagram of EEPROM and temperature sensor

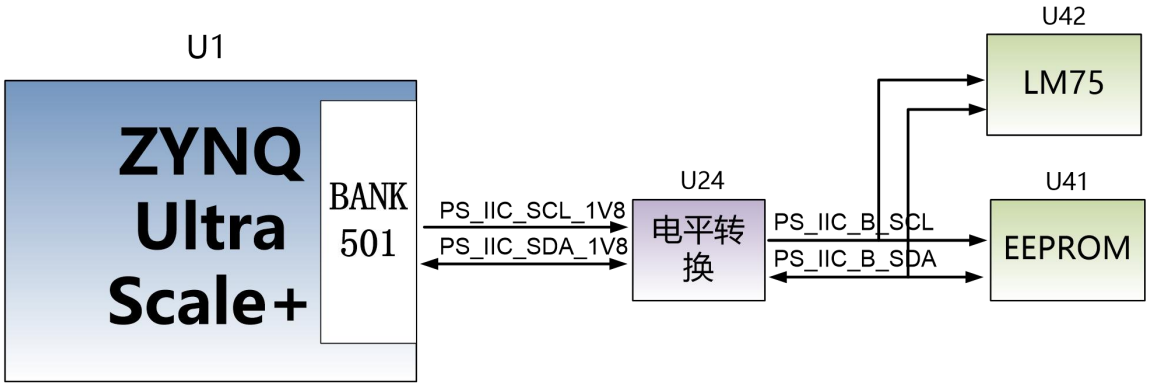


Figure 3-16-1: EEPROM and Sensor connection diagram

EEPROM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_IIC_SCL_1V8	PS_MIO34	L22	I2C Clock Signal
PS_IIC_SDA_1V8	PS_MIO35	P22	I2C Data Signal

Part 3.17: User LEDs

There are 4 LEDs on the AXU9EGB Carrier board. including 1 two-color indicator light, 1 DONE indicator, 1 PS control indicator, and 1 PL control indicator. The user can control the on and off through the program. The schematic diagram of the user's LED light hardware connection is shown in Figure 3-17-1:

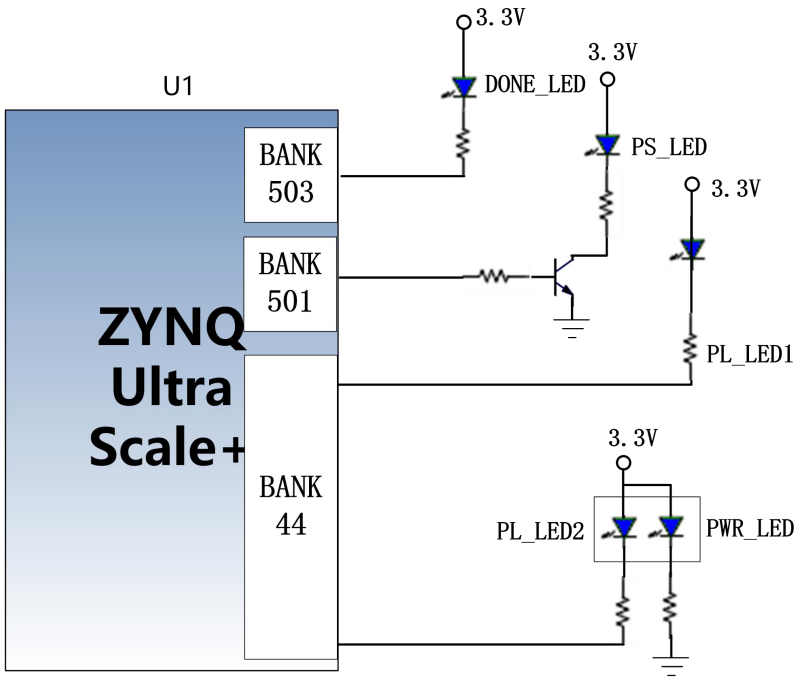


Figure 3-17-1: The User LEDs Hardware Connection Diagram

Pin assignment of user LED lights

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_LED	PS_MIO44	N24	PS User LED Light
PL_LED1	B44_L4_N	AM13	PL User LED1 Light
PL_LED2	B44_L3_N	AP12	PL User LED2 Light

Part 3.18: Keys

There are 1 reset KEY RESET and 2 user buttons on the AXU9EGB carrier board. The reset signal is connected to the reset chip input of the core board ACU4EV, and the user can use this reset KEY to reset the ZYNQ system. One user KEY is connected to the MIO of the PS, and one is connected to the IO of the PL. The reset KEY and the user KEYs are both low-level active. The connection diagram of the user key is shown in Figure 3-18-1:

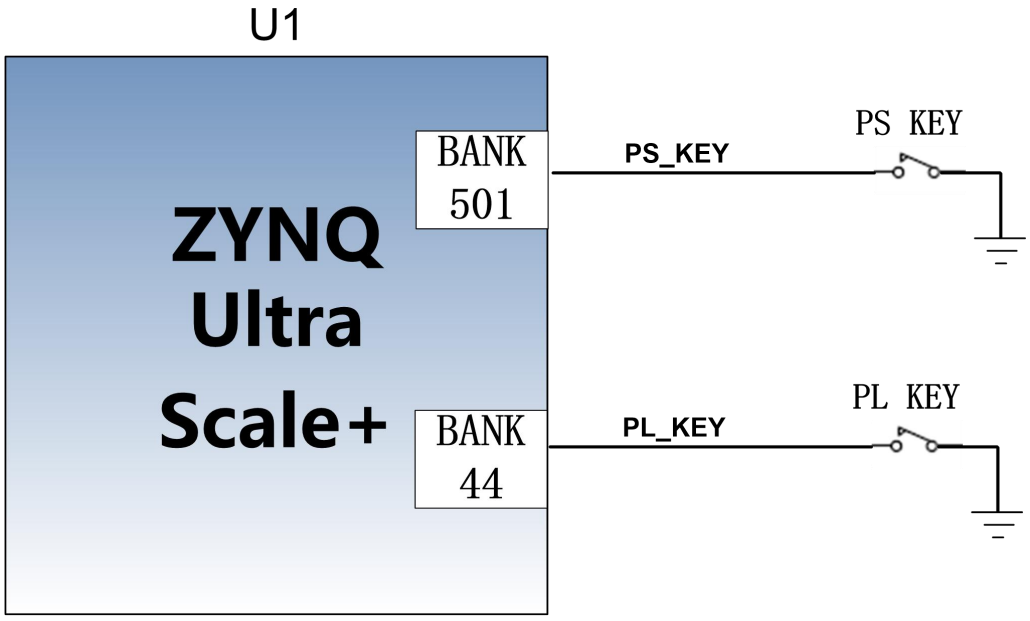


Figure 3-18-1: Rest keys connection diagram

ZYNQ pin assignment of keys

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_KEY1	PS_MIO26	H23	PS KEY Input
PL_KEY1	B44_L1_N	AN12	PL KEY Input

Part 3.19: DIP Switch Configuration

There is a 4-digit DIP switch SW1 on the FPGA development board to configure the startup mode of the ZYNQ system. The AXU9EGB system development platform supports 4 startup modes. The 4 startup modes are JTAG debug mode, QSPI FLASH, EMMC and SD2.0 card startup mode. After ZU15EV chip is powered on, it will detect the level of (PS_MODE0~3) to determine the startup mode. The user can select different startup modes through the DIP switch SW1 on the expansion board. The SW1 startup mode configuration is shown in the following table 3-19-1.

SW1	Dial Position（1，2，3，4）	MODE[3:0]	Start mode
	ON，ON，ON，ON	0000	PS JTAG

	ON，ON，OFF ,ON	0010	QSPI FLASH
	ON，OFF，ON，OFF	0101	SD Card
	ON，OFF， OFF， ON	0110	EMMC

Part 3.20: Power Supply

The power input voltage of the AXU9EGB development board is DC12V. In the carrier board, the DC12V is converted into +5V, +3.3V, +1.8V, and +1.2V, through one-way DC/DC power chip TPS54620 and three-way DC/DC power chip MP1482. The schematic diagram of the power supply design on the board is shown in Figure 3-20-1:

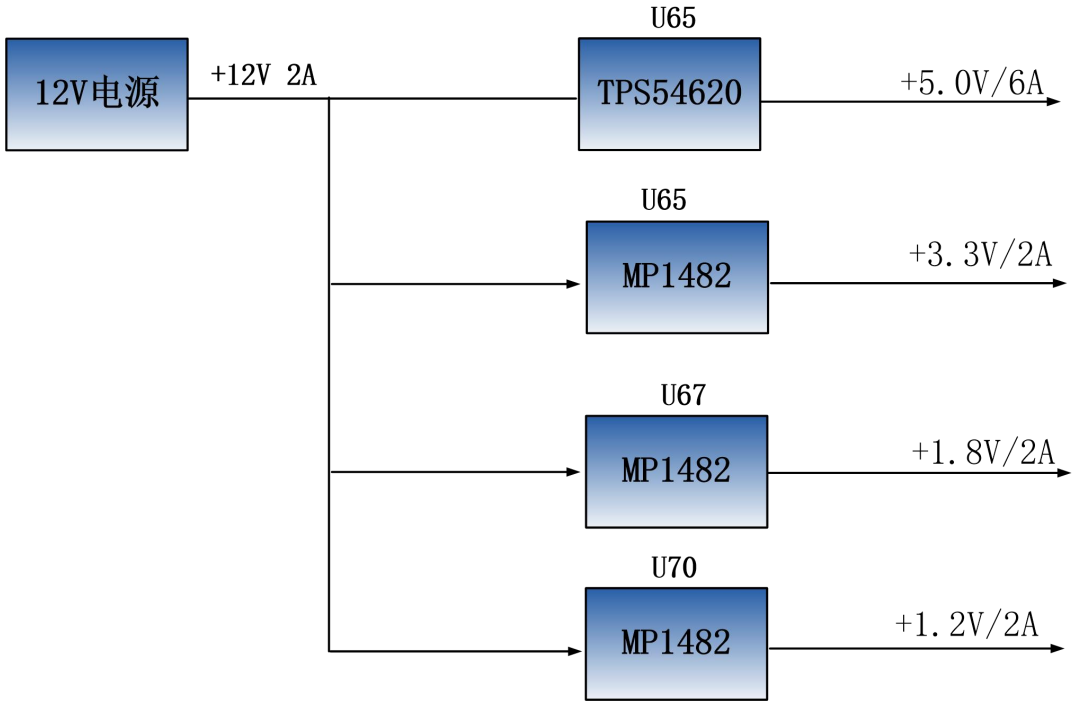


Figure 3-20-1: Carrier Board Power Schematic

The functions of each power distribution are shown in the following table:

Power	Function
+5.0V	USB power supply
+1.8V	Ethernet, USB2.0, BANK66,67 of Core Board

+3.3V	Ethernet, USB2.0, SD, DP, CAN, RS485
+1.2V	Ethernet

Part 3.21: ALINX Customized Fan

Because ZU9EG generates a lot of heat when it works normally, we add a heat sink and fan to the chip on the board to prevent the chip from overheating. The control of the fan is controlled by the ZYNQ chip. The control pin is connected to the IO of the BANK50 (PIN J10). If the IO level output is high, the MOSFET is turned on and the fan is working. If the IO level output is low, the fan stops. The fan design on the board is shown in Figure 3-21-1.

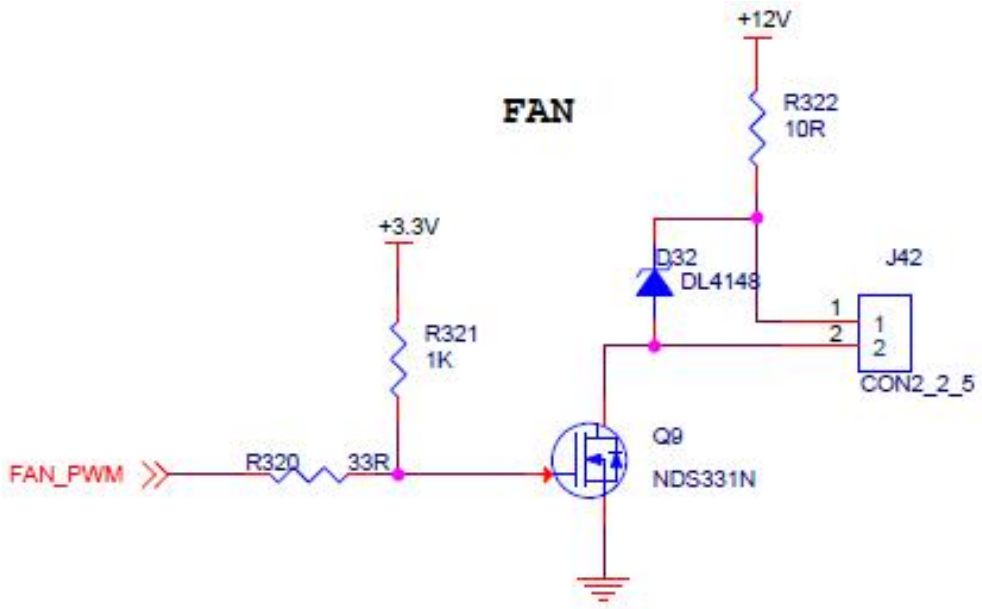


Figure 3-21-1：Fan Design Schematic

The fan has been screwed to the FPGA development board before leaving the factory. The power of the fan is connected to the socket of J55. The red is positive and the black is negative.

Part 3.22: Carrier Board Size Dimension

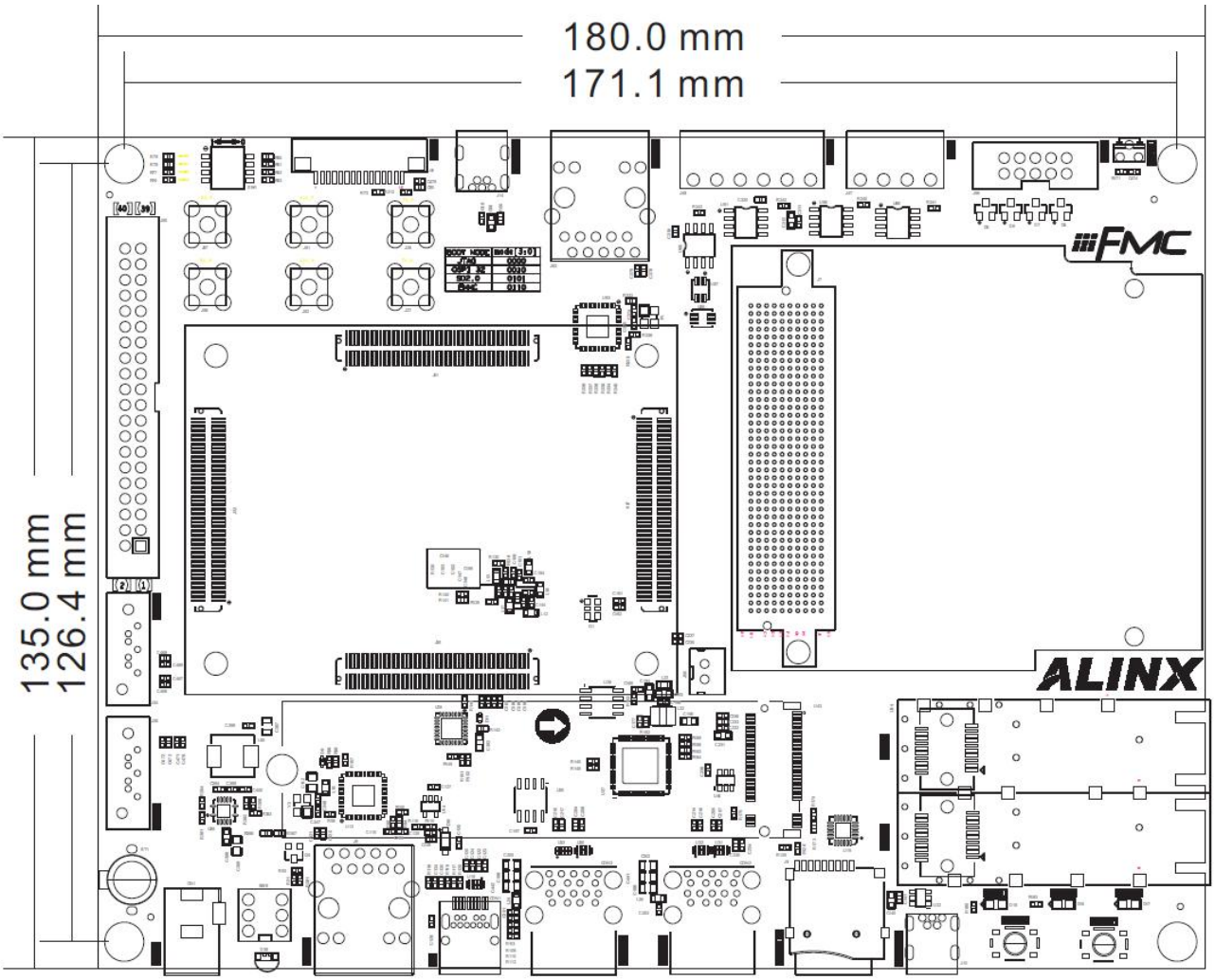


Figure 3-22-1: Top View