FMC 4-Channel High Speed AD Module FL9627 User Manual

ALINX

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Part1: FL9627 4-channel High Speed AD Module

General Description

ALINX FMC High Speed AD Module FL9627 is a 4-channel 125MSPS, 12-bit analog to digital signal conversion module. The FMC AD conversion module uses two AD9627 chips from Analog Devices. Each AD9627 chip supports two AD input conversions, so the two AD9627 chips support a total of four AD input conversions. The analog signal input has a voltage range of -5V to +5V and the interface is an SMA socket.

The module has a standard LPC FMC interface for connecting to the FPGA development board. The FMC connector model is: ASP_134604_01

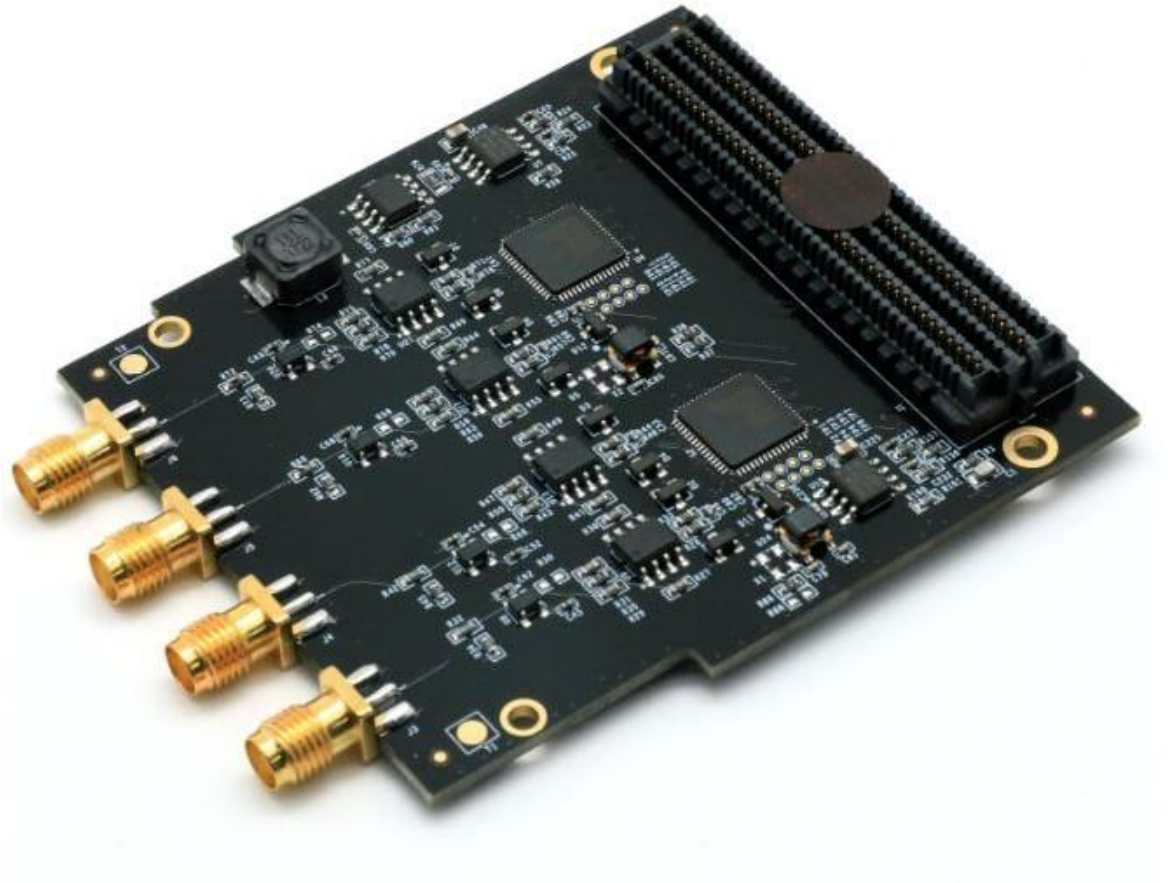

Figure 1-1: FL9627 module product photo

Part 1.1: FL9627 Module Detail Parameter

FL9627 FMC 4-channel high speed AD Module detail parameter listed as below:

- AD Conversion chip: 2 pieces AD9627
- AD Conversion channel: 4 channels
- AD update rate: 125MSPS
- AD bits: 12 digits
- Digital interface level standard: LVDS level of +1.8V
- AD analog signal input range: -5V~+5V;
- Analog signal input interface: SMA interface
- Configuration interface: SPI interface
- Working temperature: -40 ˚C ~ 85 ˚C

Part 1.2: FL9627 Module Size Dimension

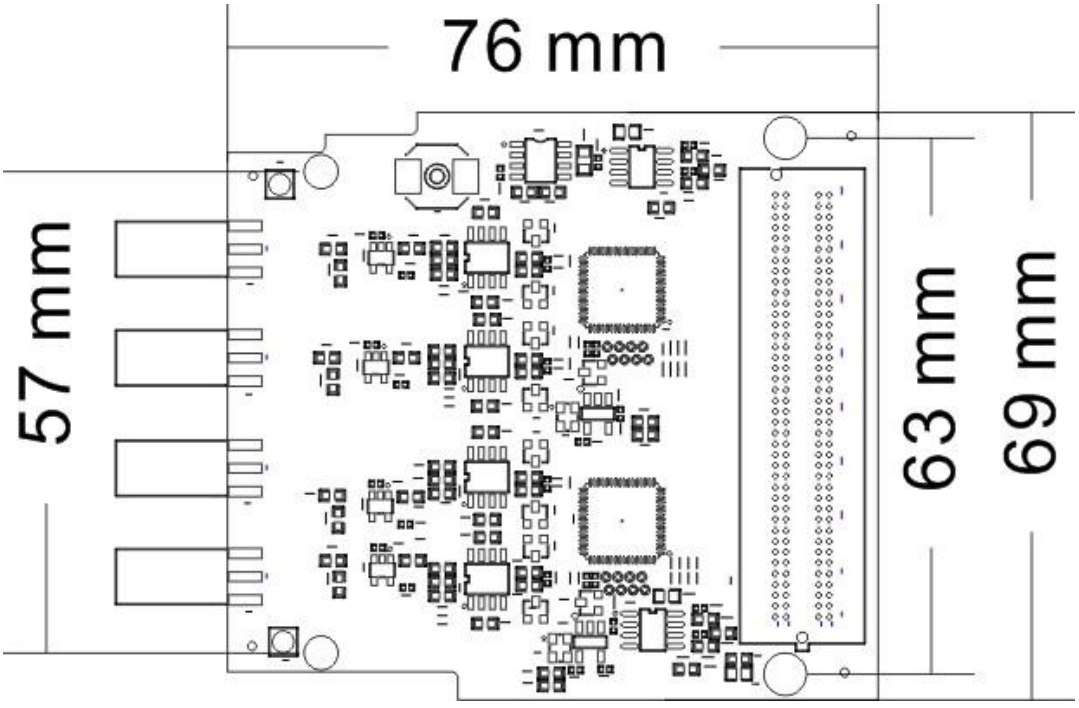

Figure 1-2: FL9627 FMC 4-channel High Speed AD Module Size Dimension

Part 2: FL9627 Module Function Description

Part 2.1: FL9627 Module Block Diagram

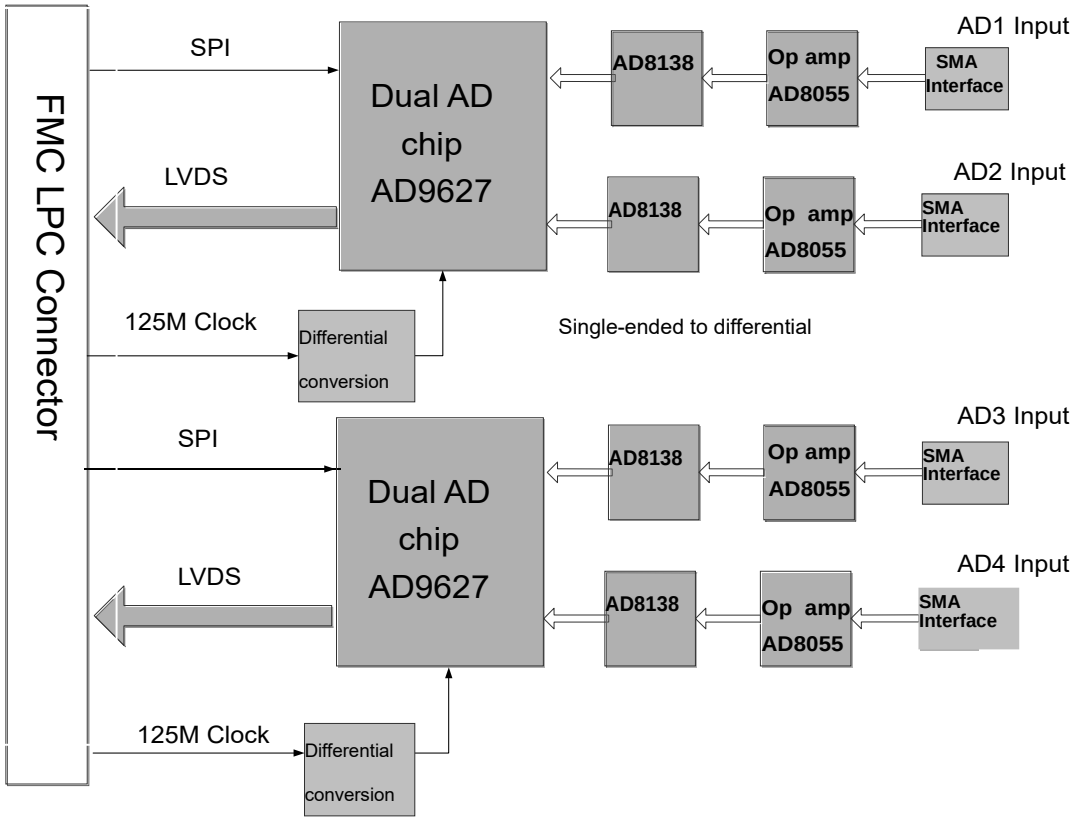

Figure 2-1: FL9627 Module Block Diagram

For the circuit design of the AD9627, please refer to the chip manual of the AD9267.

Part 2.2: Operational amplifier Circuit on the FL9627 Module

The FPGA development board uses a 300Mhz bandwidth AD8055 chip and a voltage divider resistor to reduce the voltage of the -5V~+5V input to -1V~+1V. If the user wants to input a wider range of voltage inputs, simply modify the resistance of the front-end divider resistor.

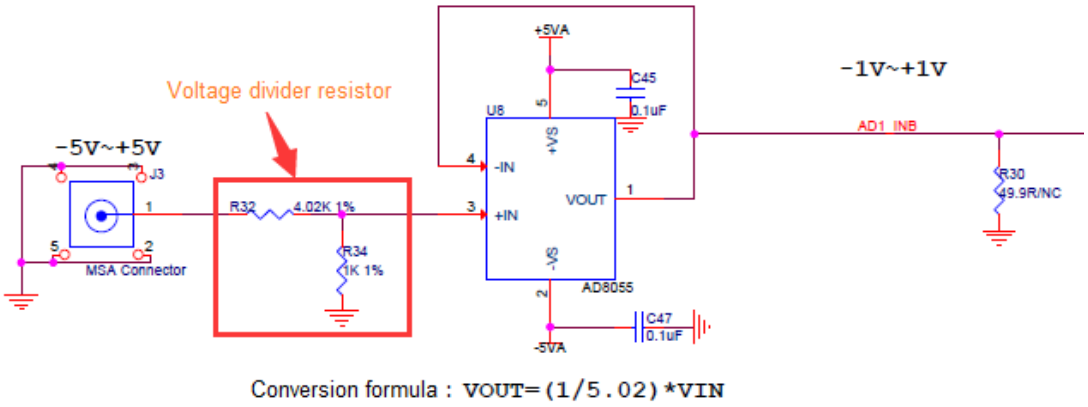

Figure 2-2：Input voltage conversation

The following table is a comparison of the analog input signal and the voltage of the AD8055 op amp output:

AD analog input value	AD8055 op amp output
-5V	-1V
0V	0V
+5V	+1V

Part 2.3: Single-ended to differential and AD conversion

The input voltage of -1V~+1V is converted into a differential signal (VIN+ −VIN−) by the AD8138 chip. The common mode level of the differential signal is determined by the CML pin of AD.

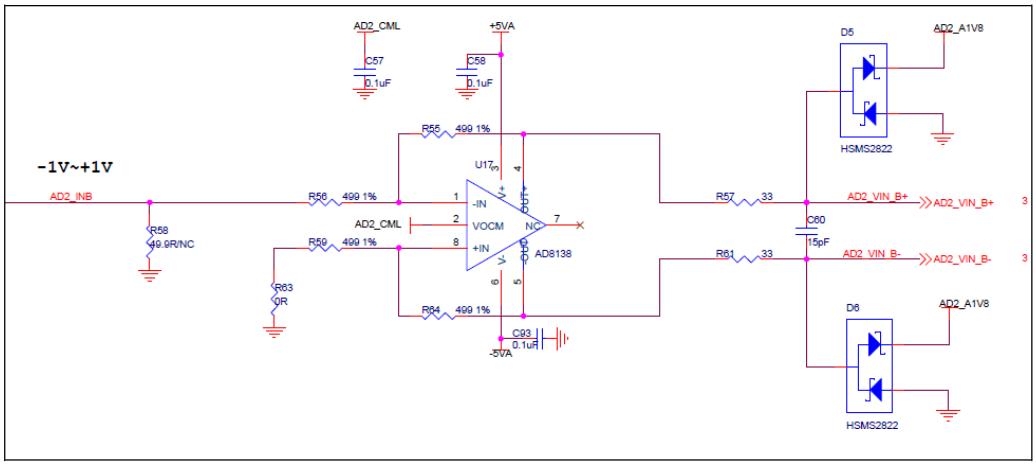

Figure 2-3：Compressed input voltage conversation to differential signal

The following table shows the voltage comparison table after the analog input signal to the differential output of the AD8138:

AD analog input value	AD8055 op amp output	AD8138 Differential Output (VIN+−VIN−)
-5V	-1V	+1V
0V	0V	0V
+5V	+1V	-1V

If AD is configured as Offset Binary Output Mode, the value of AD conversion is as shown below:

Table 16. Output Data Format

Input (V)	Condition (V)	Offset Binary Output Mode
VIN+ – VIN–	< –VREF – 0.5 LSB	0000 0000 0000
VIN+ – VIN–	= –VREF	0000 0000 0000
VIN+ – VIN–	= 0	1000 0000 0000
VIN+ – VIN–	= +VREF – 1.0 LSB	1111 1111 1111
VIN+ – VIN–	> +VREF – 0.5 LSB	1111 1111 1111

In the module circuit design, the VREF value of the AD9627 is 1V, so the final analog signal input and AD conversion data are as follows:

AD analog input value	AD8055 op amp output	AD8138 Differential Output (VIN+−VIN−)	AD9627 digital output
-5V	-1V	+1V	11111111111
0V	0V	0V	100000000000
+5V	+1V	-1V	000000000000

From the table we can see that the AD9627 converts the largest digital value when the -5V input, and the digital value converted by the AD9627 is the smallest when the +5V input.

Part 2.4: FL9627 digital output timing

The digital output of the AD9627 dual AD are configured as a +1.8V LVDS output mode. The two channels (A and B) share a pair of differential clock

signals and 12 pairs of differential data signals. The order of data output is alternate output, one AD is output on the rising edge of the clock, and the other AD data is output on the falling edge of the clock.

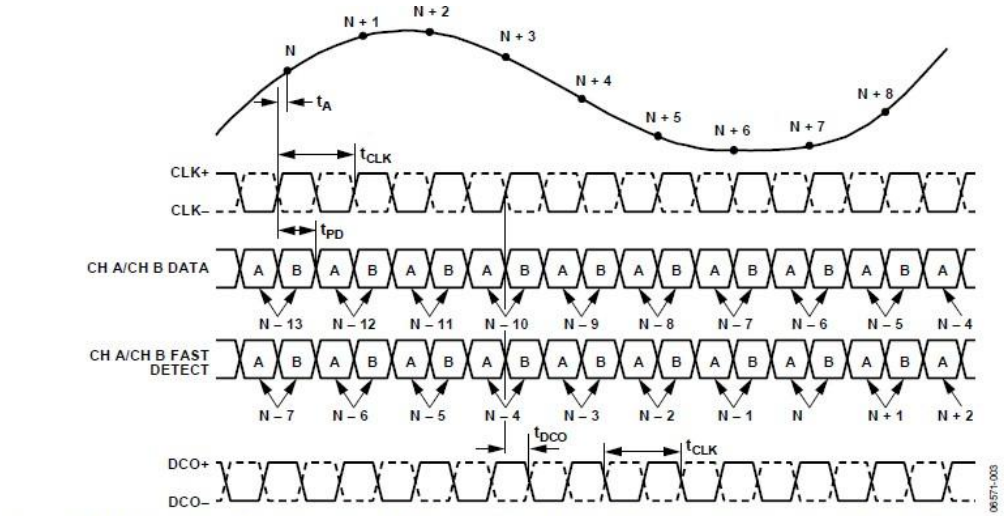

Figure 3. LVDS Mode Data and Fast Detect Output Timing (Fast Detect Mode Select Bits = 001 Through Fast Detect Mode Select Bits = 100)

Figure 2-4：FL9627 digital output timing

Part 2.5: FL9627 LVDS standard

From the chip manual of the AD9627, we can see that the level standard of the +1.8V LVDS output by the AD9627 is as follows:

Parameter	Temperature	Min	Typ	Max	Unit
LVDS Mode—DRVDD = 1.8 V					
Differential Output Voltage (V_{OD}), ANSI Mode	Full	250	350	450	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.15	1.25	1.35	V
Differential Output Voltage (V_{OD}), Reduced Swing Mode	Full	150	200	280	mV
Output Offset Voltage (V_{OS}), Reduced Swing Mode	Full	1.15	1.25	1.35	V

The level standard of the +2.5V LVDS input of the FPGA chip is as follows:

Table 12: **LVDS_25 DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.375	2.500	2.625	V
V_{IDIFF}	Differential Input Voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.500	V

The differential signal output from the AD9627 fully meets the +2.5V LVDS input level standard of the FPGA.

Part 2.6: FL9627 Module FMC LPC pin assignment

Only the signals of the power supply and interface are listed below. The signal of GND is not listed. For details, please refer to the schematic.

Pin Number	Signal Name	Description
C35	+12V	12V Power Input
C37	+12V	12V Power Input
D32	+3.3V	3.3V Power Input
C34	GA0	Bit0 of EEPROM address
D35	GA1	Bit1 of EEPROM address
D8	CLK1_125M	125M reference clock input for the AD1 chip
G6	AD1_DCO+	Data clock output –P of AD1 channel A and channel B LVDS
G7	AD1_DCO-	Data clock output –N of AD1 channel A and channel B LVDS
H7	AD1_DO+	Data 0 Output -P for AD1 Channel A and Channel B LVDS
H8	AD1_DO-	Data 0 Output -N for AD1 Channel A and Channel B LVDS
C10	AD1_D1+	Data 1 Output -P for AD1 Channel A and Channel B LVDS
C11	AD1_D1-	Data 1 Output -N for AD1 Channel A and Channel B LVDS
D11	AD1_D2+	Data 2 Output -P for AD1 Channel A and Channel B LVDS
D12	AD1_D2-	Data 2 Output -N for AD1 Channel A and Channel B LVDS
H10	AD1_D3+	Data 3 Output -P for AD1 Channel A and Channel B LVDS
H11	AD1_D3-	Data 3 Output -N for AD1 Channel A and Channel B LVDS
C14	AD1_D4+	Data 4 Output -P for AD1 Channel A and Channel B LVDS
C15	AD1_D4-	Data 4 Output -N for AD1 Channel A and Channel B LVDS
G12	AD1_D5+	Data 5 Output -P for AD1 Channel A and Channel B LVDS
G13	AD1_D5-	Data 5 Output -N for AD1 Channel A and Channel B LVDS
H13	AD1_D6+	Data 6 Output -P for AD1 Channel A and Channel B LVDS

H14	AD1_D6-	Data 6 Output -N for AD1 Channel A and Channel B LVDS
D14	AD1_D7+	Data 7 Output -P for AD1 Channel A and Channel B LVDS
D15	AD1_D7-	Data 7 Output -N for AD1 Channel A and Channel B LVDS
G15	AD1_D8+	Data 8 Output -P for AD1 Channel A and Channel B LVDS
G16	AD1_D8-	Data 8 Output -N for AD1 Channel A and Channel B LVDS
H16	AD1_D9+	Data 9 Output -P for AD1 Channel A and Channel B LVDS
H17	AD1_D9-	Data 9 Output -N for AD1 Channel A and Channel B LVDS
D17	AD1_D10+	Data 10 Output -P for AD1 Channel A and Channel B LVDS
D18	AD1_D10-	Data 10 Output -N for AD1 Channel A and Channel B LVDS
C18	AD1_D11+	Data 11 Output -P for AD1 Channel A and Channel B LVDS
C19	AD1_D11-	Data 11 Output -N for AD1 Channel A and Channel B LVDS
G9	AD1_SPI_CS	SPI communication chip select signal for AD1 chip
G10	AD1_SPI_SDIO	SPI communication data signal of AD1 chip
D9	AD1_SPI_SCLK	SPI communication clock signal of AD1 chip
G19	AD1_SMI_SCLK	AD1 monitor signal serial output clock signal
G18	AD1_SMI_SDFS	AD1 monitor signal serial output data frame sync signal
D20	CLK2_125M	125M reference clock input for the AD2 chip
C22	AD2_DCO+	Data clock output –P of AD2 channel A and channel B LVDS
C23	AD2_DCO-	Data clock output –N of AD2 channel A and channel B LVDS
G21	AD2_DO+	Data 0 Output -P for AD2 Channel A and Channel B LVDS
G22	AD2_DO-	Data 0 Output -N for AD2 Channel A and Channel B LVDS
H22	AD2_D1+	Data 1 Output -P for AD2 Channel A and Channel B LVDS
H23	AD2_D1-	Data 1 Output -N for AD2 Channel A and Channel B LVDS

C26	AD2_D2+	Data 2 Output -P for AD2 Channel A and Channel B LVDS
C27	AD2_D2-	Data 2 Output -N for AD2 Channel A and Channel B LVDS
G24	AD2_D3+	Data 3 Output -P for AD2 Channel A and Channel B LVDS
G25	AD2_D3-	Data 3 Output -N for AD2 Channel A and Channel B LVDS
H25	AD2_D4+	Data 4 Output -P for AD2 Channel A and Channel B LVDS
H26	AD2_D4-	Data 4 Output -N for AD2 Channel A and Channel B LVDS
D26	AD2_D5+	Data 5 Output -P for AD2 Channel A and Channel B LVDS
D27	AD2_D5-	Data 5 Output -N for AD2 Channel A and Channel B LVDS
G27	AD2_D6+	Data 6 Output -P for AD2 Channel A and Channel B LVDS
G28	AD2_D6-	Data 6 Output -N for AD2 Channel A and Channel B LVDS
H28	AD2_D7+	Data 7 Output -P for AD2 Channel A and Channel B LVDS
H29	AD2_D7-	Data 7 Output -N for AD2 Channel A and Channel B LVDS
G30	AD2_D8+	Data 8 Output -P for AD2 Channel A and Channel B LVDS
G31	AD2_D8-	Data 8 Output -N for AD2 Channel A and Channel B LVDS
H31	AD2_D9+	Data 9 Output -P for AD2 Channel A and Channel B LVDS
H32	AD2_D9-	Data 9 Output -N for AD2 Channel A and Channel B LVDS
G33	AD2_D10+	Data 10 Output -P for AD2 Channel A and Channel B LVDS
G34	AD2_D10-	Data 10 Output -N for AD2 Channel A and Channel B LVDS
H34	AD2_D11+	Data 11 Output -P for AD2 Channel A and Channel B LVDS
D21	AD2_SPI_CS	SPI communication chip select signal for AD2 chip
D23	AD2_SPI_SDIO	SPI communication data signal of AD2 chip
D24	AD2_SPI_SCLK	SPI communication clock signal of AD2 chip
G37	AD2_SMI_SCLK	AD2 monitor signal serial output clock signal

G36	AD2_SMI_SDFS	AD2 monitor signal serial output data frame sync signal
H37	AD2_SMI_SDO	AD2 chip monitor signal serial output data signal
H20	AD_SYNC	Digital synchronization signal
C30	SCL	EEPROM I2C clock
C31	SDA	EEPROM I2C data
G39	VADJ	VADJ power input
H40	VADJ	VADJ power input

Part 3: DEMO program description for AD sampling

We provide the AD acquisition and display routines for the ALINX FPGA development board, in which the differential LVDS clock signals and differential LVDS data signals from the two AD9627 inputs are converted to single-ended signals by the IBUFDS module, respectively. Then converted to A channel 12-bit data and B-channel 12-bit data by the IDDR module. The 12-bit data of the A channel and the B channel are observed by the ILA online debug.

After power on, the AD9267 register needs to be configured. Here, the SPI bus is used to configure the register for each AD9267 chip, so that the AD9627 operates in LVDS mode.

The functional block diagram of the FPGA AD testing is as follows:

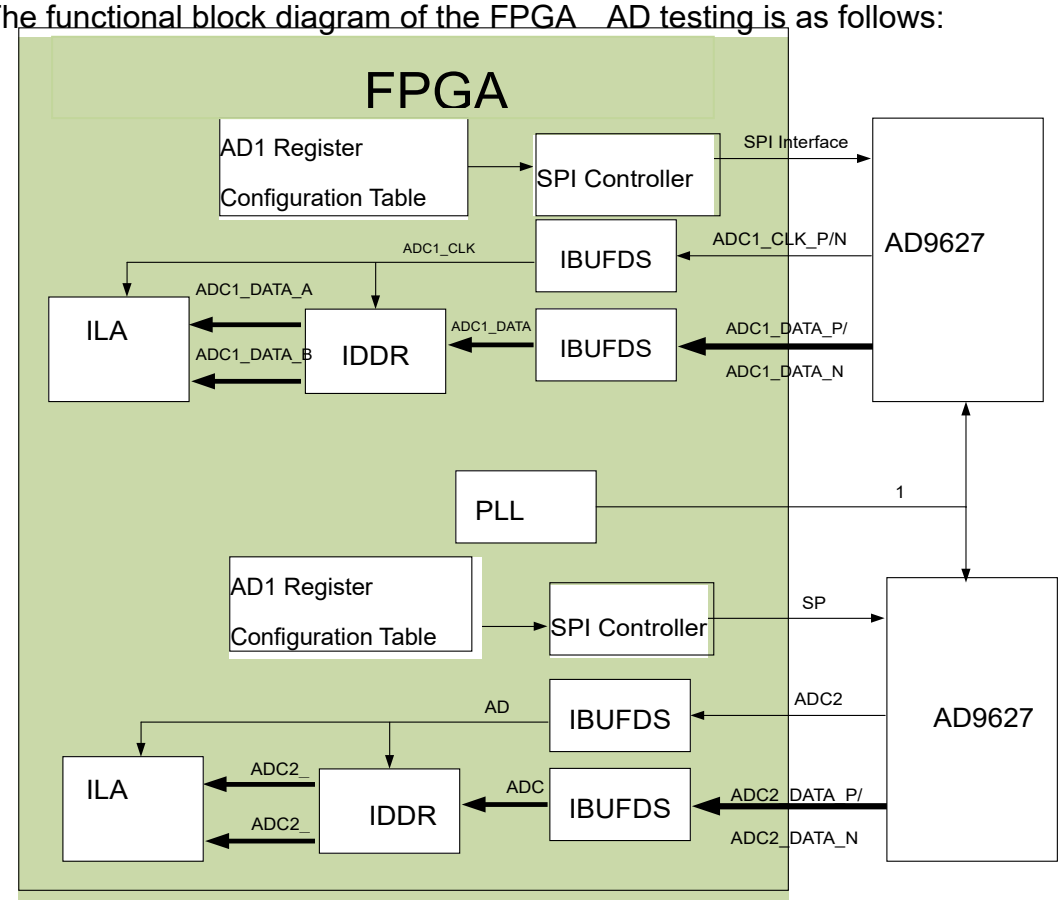

Figure 3-1: The functional block diagram of the FPGA AD Testing

The following is a brief introduction to the functions of each module used in the FPGA program:

1) lut_config.v

The AD9627 register configuration table, where only two register values are configured, one is register 0x14 and the other is register 0x FF.

Register 0x14 is configured as an LVDS output format and the output is in offset binary mode.

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0x14	Output Mode	Drive strength 0 V to 3.3 V CMOS or ANSI LVDS; 1 V to 1.8 V CMOS or reduced LVDS (global)	Output type 0 = CMOS 1 = LVDS (global)	Open	Output enable bar (local)	Open	Output invert (local)	00 = offset binary 01 = twos complement 01 = gray code 11 = offset binary (local)		0x00	Configures the outputs and the format of the data

After register 0x14, you need to write 1 to the lowest bit of the 0xFF register to take effect.

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0xFF	Transfer	Open	Open	Open	Open	Open	Open	Open	Transfer	0x00	Synchronously transfers data from the master shift register to the slave

Specific register meanings refer to the AD9627 chip manual.

2) spi_config.v

This module configures the AD9627 chip registers by calling the SPI communication module (adc_spi.v). The configured register address and value are defined in the lut_config.v file.

3) top.v

The top module implements the following functions in addition to the submodules above:

- Calling PLL IP to generate the 125Mhz reference clock required for the AD9627 chip
- Call IBUFDS to convert LVDS differential clock signals and data signals into single-ended clocks and single-ended data.
- Call IDDR to realize double-edge A and B channel data conversion

to single-edge A channel data and B channel data

4) **Xdc constraint file**

The xdc constraint file defines two AD communication pins and an ILA debug interface. The user can modify the ILA interface signal to observe the signal he wants to observe.

Part4: Hardware Connection and Testing

The hardware connection between the FL9627 module and the FPGA development board is very simple. Simply plug the FL9627 FMC interface into the FMC interface of the FPGA development board and fix it with screws. The following is the hardware connection of the ALINX AX7325 development board and FL9627:

After power on the FPGA development board, the signal generator generates a positive selection wave of -5V~+5V, the frequency is 200Khz, and then downloads the program in the Vivado environment.

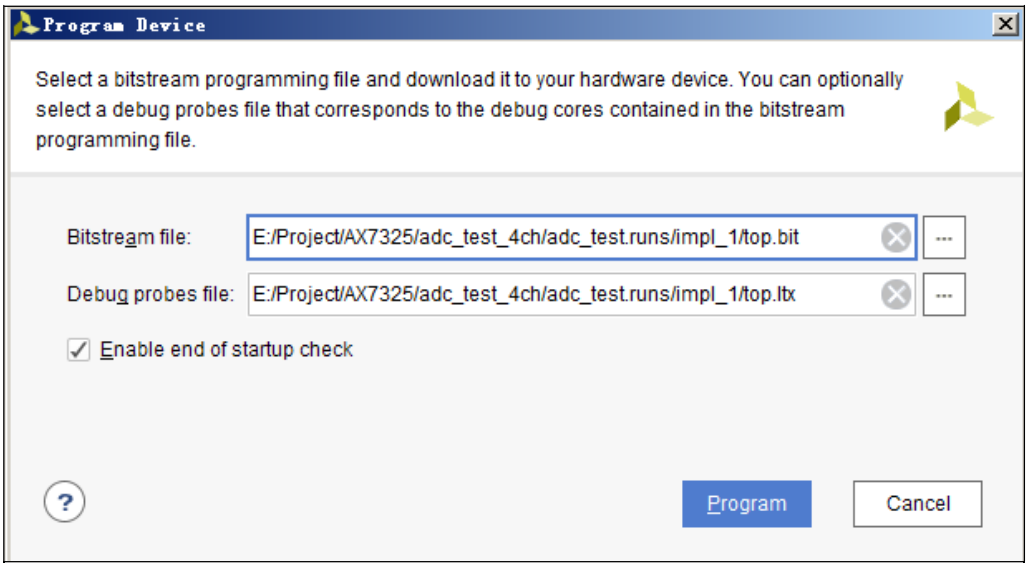

Figure 4-1: Hardware connection of ALINX AX7325 and FL9627:

The interface of hw_ila_1 will appear here, and the AD acquisition data of channel A and channel B of the first AD module will be displayed in the hw_ila_1

interface. Click the "Run trigger mode for this ILA core" button and the adc1_data_a_d0 channel will display the positive selection wave.

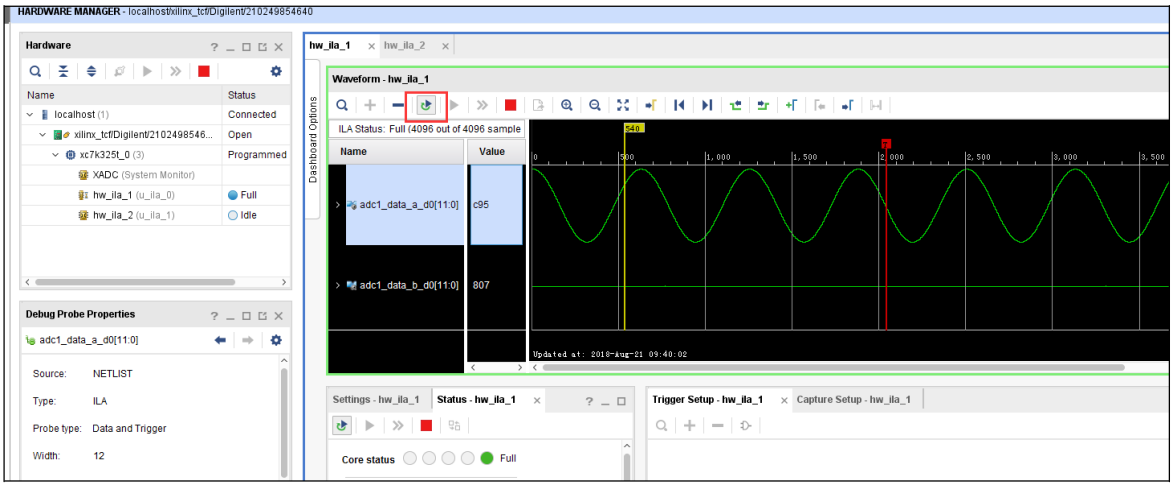

Figure 4-2: The interface of hw_ila_1

Change the signal transmitter to generate a square wave of -5V~+5V, and then click the "Run trigger mode for this ILA core" button. The adc1_data_a_d0 channel will display a square wave. We can see that when +5V is used, the data collected by AD is 04e, and the data collected by AD when -5V is fb3.

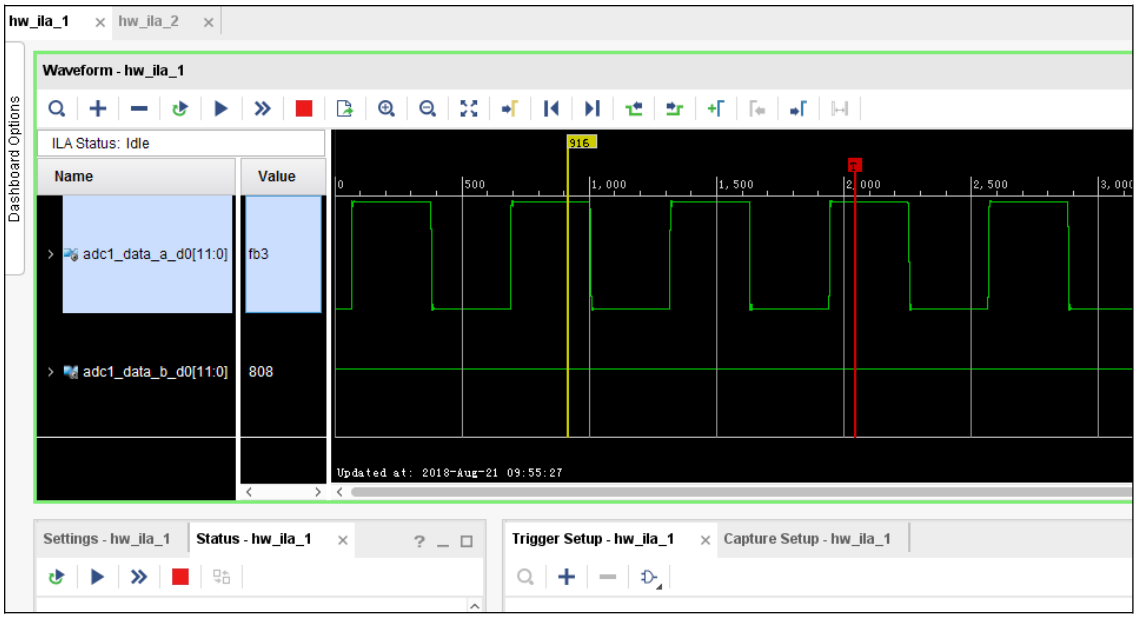

Figure 4-3: Square wave

If the user needs to measure the waveform of another AD2, the analog signals needs to be input to channel A or channel B of AD2. Then double-click hw_ila_2 to display the interface of hw_ila_2.

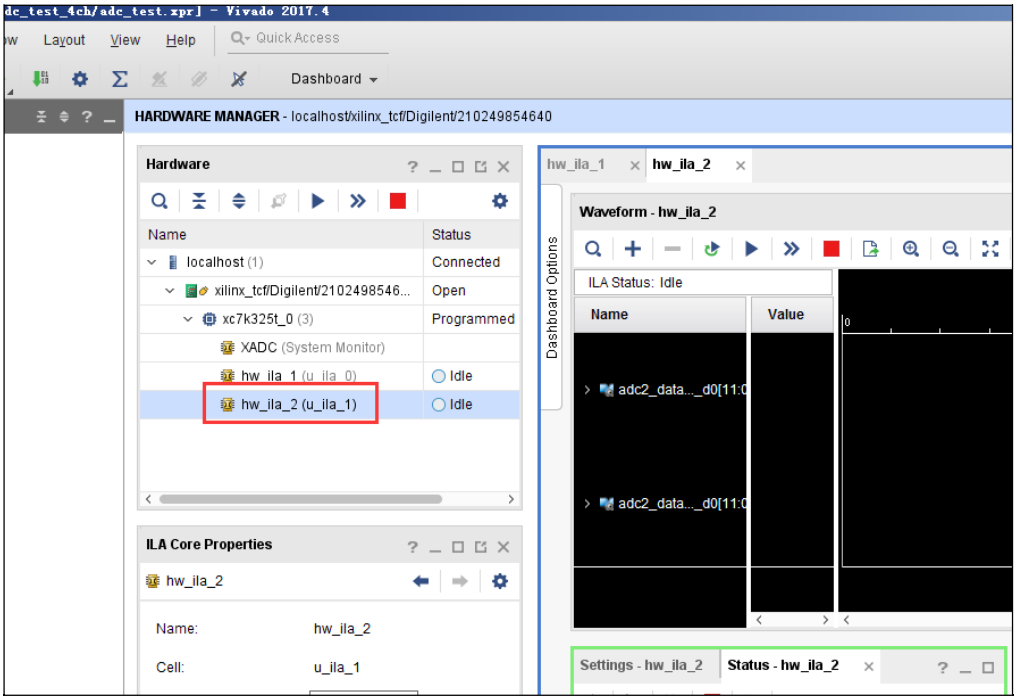

Figure 4-4: The interface of hw_ila_2