

Versal AI Edge Series Development Board User Manual

VD100

REV Version 1.0

ALINX ELECTRONIC LIMITED

WWW.EN.ALINX.COM

Version Record

| Version | Date | Release By | Description |
|---------|-----------|------------|---------------|
| Rev 1.0 | 2024/2/26 | Kathy Xia | First Release |

Table of Contents

| | |
|--|----|
| Version Record | 2 |
| Part 1: Development Board Introduction..... | 5 |
| Part 2: VE2302 SOM..... | 8 |
| Part 2.1: Introduction..... | 8 |
| Part 2.2: VE2302..... | 9 |
| Part 2.3: Clock Configuration | 10 |
| Part 2.4: DDR4 DRAM | 11 |
| Part 2.5: QSPI Flash..... | 15 |
| Part 2.6: eMMC Flash | 16 |
| Part 2.7: LEDs..... | 17 |
| Part 2.8: Power Supply..... | 17 |
| Part 2.9: Expansion Interface..... | 18 |
| Part 2.10: Structure Diagram | 24 |
| Part 3: Baseboard | 25 |
| Part 3.1: Introduction..... | 25 |
| Part 3.2: Gigabit Ethernet Interface..... | 25 |
| Part 3.3: PCIe3.0X4 Interface..... | 27 |
| Part 3.4: SFP+ Fiber Interface | 28 |
| Part 3.5: USB to Serial Port | 29 |
| Part 3.6: USB2.0 Interface | 30 |
| Part 3.7: LVDS Display Interface | 31 |
| Part 3.8: MIPI Interface..... | 32 |
| Part 3.9: SD Card | 33 |
| Part 3.10: EEPROM 24LC04 & Temperature Sensor..... | 34 |
| Part 3.11: JTAG Interface | 34 |
| Part 3.12: CANFD Communication Interface | 35 |
| Part 3.13: PMOD Expansion Port | 36 |
| Part 3.14: Keys | 36 |
| Part 3.15: LEDs..... | 37 |
| Part 3.16: Power Supply | 38 |
| Part 3.17: Structural Dimension Drawing | 39 |

The Adaptive Computing Acceleration Platform (ACAP) (Model: VD100) of the ALINX Versal AI Edge Series has been officially released. To let you quickly understand this development platform, we have written this user manual.

This Versal AI Edge development platform uses a System-on-Module (SOM/module) plus base board model to facilitate users' secondary development and utilization of the SOM. In the base board design, we use 1×12-pin PMOD interface, 2×10 Gigabit optical fiber interfaces, 2×Ethernet interfaces, 2×MIPI interfaces, 1×USB2.0 interface, 1×UART interface and 1×PCIe3.0 x4 interface. It meets users' requirements for high-speed data transmission and exchange and is a “professional-level” and “all-around-level” development platform for data communications. We believe that such a product is very suitable for students, engineers and other groups engaged in artificial intelligence, data acceleration and video image processing.



Figure 1: VD100 development board

Part 1: Development Board Introduction

Here is a brief introduction to the Versal AI VD100 platform.

The whole structure of the development board is designed by inheriting our consistent SOM plus base board model. High-speed inter-board connectors are used between the SOM and the base board.

The SOM is mainly composed of Versal AI VE2302 + 4×DDR4 + QSPI FLASH + EMMC. We choose the VE2302 chip of Versal AI Series and package it with SFVA784. The VE2302 and DDR4 have a data bit width of 64 bits, DDR4 capacity up to 4GB, and data rate up to 3200bps. Meet the need for high buffers during data processing. In addition, there are 8G EMMC and 512Mbit QSPI FLASH on the SOM for system startup and data storage.

There are abundant peripheral interfaces on the baseboard. Figure 2 shows the structure of the entire VD100 platform:

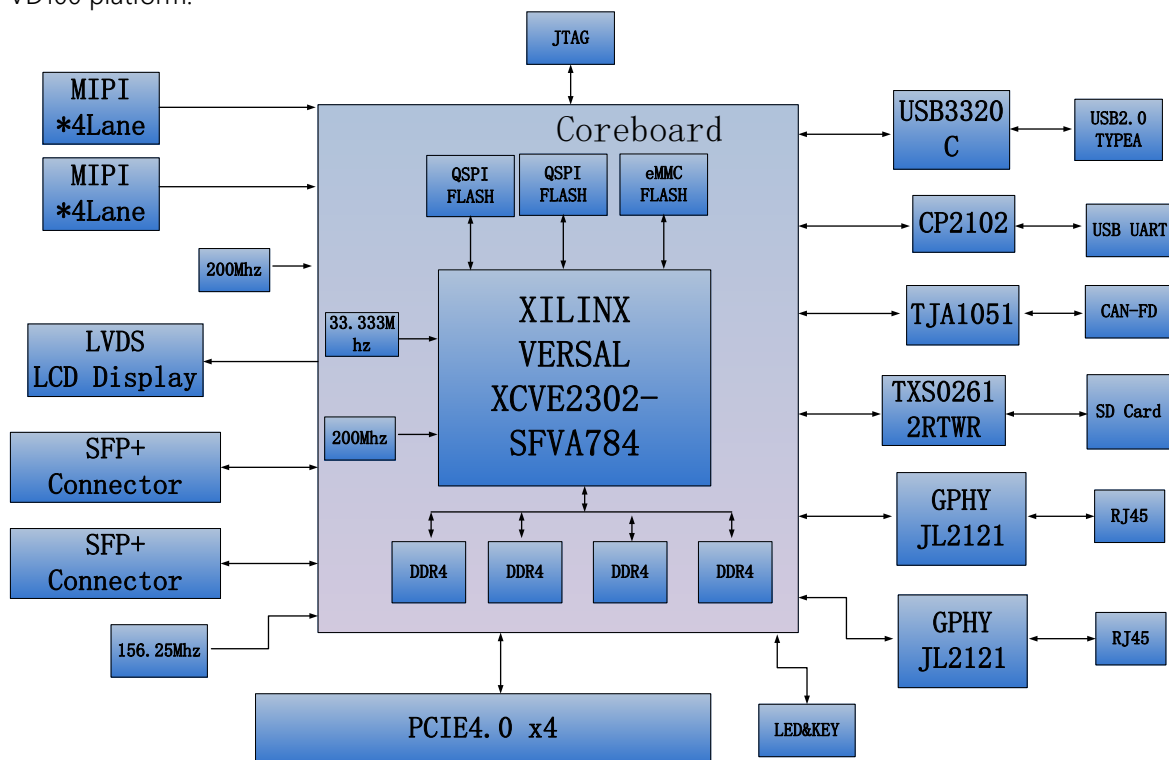


Figure 2: Structure of VD100

Through Figure 2, we can see the functions that our development platform can achieve.

- **Versal AI VE2302 SOM**

It is composed of VE2302 + 4GB DDR4 + 8G EMMC + 512Mb QSPI FLASH. In addition, there are two high-precision SiTime's crystal oscillators, one is single-ended 33.3333MHz, and the other is differential 200MHz, which provide stable clock input for VE2302 system and logic unit.

- **10/100M/1,000M Ethernet RJ-45 interface**

The JL2121 Ethernet PHY chip of JLSemi is used to provide network communication services for users.

JL2121 chip supports 10/100/1,000 Mbps network transmission rate; Full-duplex and adaptive.

- **USB Uart Debug interface**

The 1×Uart to USB interface is used to communicate with the computer, which is convenient for users to debug. The serial port chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface.

- **PCIe x4 interface**

It supports PCI Express 3.0 standard and provides standard PCIe x4 high-speed data transmission interface.

- **Micro SD deck**

1×Micro SD deck for storing OS images and file systems.

- **USB2.0 interface**

One high-speed USB2.0 interface can be used to connect USB peripherals such as mouse, keyboard, and U disk to the development board.

- **MIPI interface**

2×MIPI interfaces support MIPI 4xLane and can be connected to ALINX's MIPI camera (AN5010).

- **LVDS interface**

1×LVDS interface for connecting the LVDS display screen of ALINX.

- **2×SFP+ Optical Fiber interfaces**

Two high-speed transceivers of the GTY transceiver are connected to the sending and receiving of the two optical modules to realize two high-speed optical fiber communication interfaces. The receiving and sending speed of each optical fiber data communication is up to 12.5Gb/s.

- **CAN communication interface**

1×CAN/CAN FD bus interface, TJA1051T chip of TI company is selected, and 3-pin green wiring terminal is used for the interface.

- **12-pin PMOD expansion port**

One 12-pin expansion IO port with a pitch of 2.54 mm is reserved. The expansion port includes 2 channels of 3.3 V power supply, 2 channels of ground and 8 channels of 3.3 V IO ports.

- **JTAG interface**

10-pin 2.54mm standard JTAG port for downloading and debugging of VE2302 program.

- **Key**

There are two user buttons on the base board, one is connected to the MIO of PS and the other is connected to the IO of PL.

- **Led**

5 LEDs (2 on SOM and 3 on base board).

Part 2: VE2302 SOM

Part 2.1: Introduction

V100 (SOM model, the same below) SOM is a high-performance module developed based on XCVE2302-SFVA784-1LP-E-S chip of Versal ACAP series of XILINX. It has the characteristics of high performance, low latency, edge computing and low power consumption, and is suitable for data center, video image processing and high-speed data processing, etc.

This module uses four MT40A512M16LY-062E chips of MICRON. The DDR4 chip has 64-bit data bus bandwidth and 4GB capacity; DDR4 SDRAM can run at a maximum speed of 1600MHz (data rate of 3200Mbps). In addition, two 256MBit QSPI FLASH chips and one 8GB EMMC chip are integrated on the module for boot storage configuration and system files.

The PS side of this module expands 53 MIOs of 1.8 V level standard, the PL side expands 22 standard IOs of 3.3 V level, 54 standard IO ports of 1.8 V level, 30 standard IOs of 1.2 V level and 8 pairs of GTY high-speed RX/TX differential signals. Moreover, the wiring between the FPGA chip and the interface is processed with equal length and difference, and the size of the module is only 65 * 60 (mm), which is very suitable for secondary development.



Figure 3: Front view of V100 module

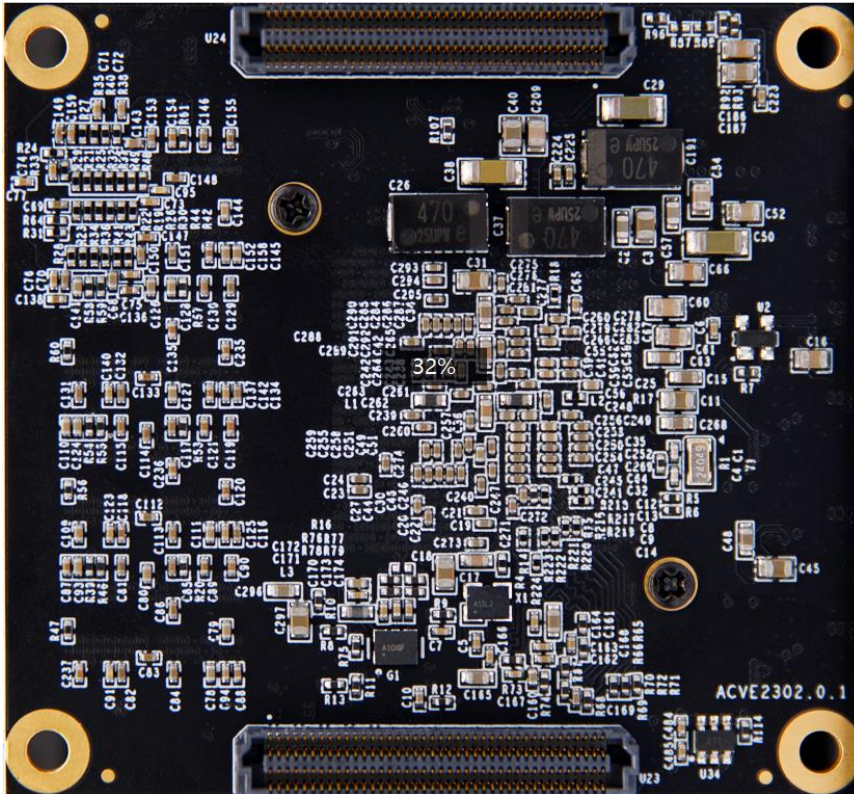
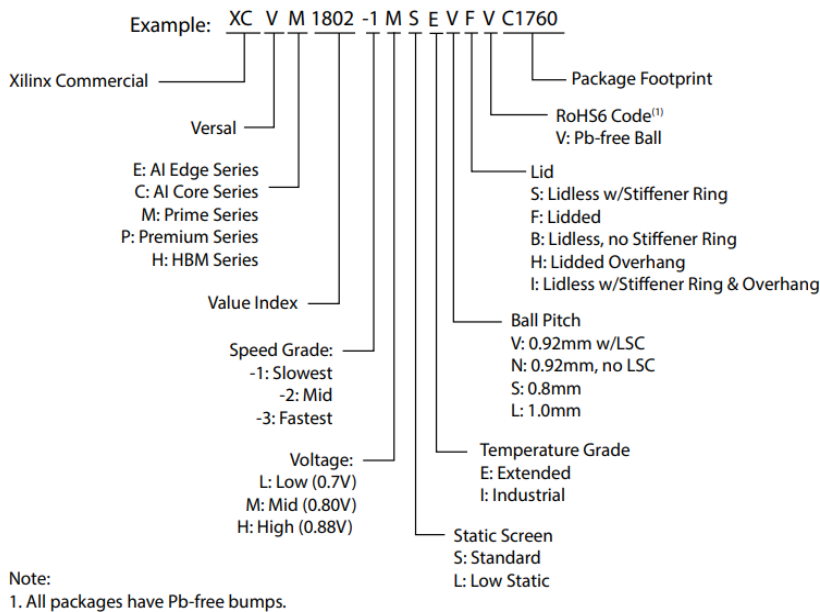


Figure 4: Back view of V100 module

Part 2.2: VE2302

As mentioned earlier, the Versal ACAP model we use is XCVE2302-SFVA784-1LP-E-S, speed class 1, operating temperature 0~100°C, and package SFVA784. The chip naming convention for Versal ACAP is as follows:



DS950_03_101922

Figure 5: Versal Ordering Information

The VE2302 chip integrates four ARM Cortex™ -A72 processors and two Cortex-R5F processors, as well as 34 AI Engines-ML acceleration units and 464 DSP processing units. The internal resources of the VE2302 are as follows:

| | VE2002 | VE2102 | VE2202 | VE2302 | VE1752 | VE2602 | VE2802 |
|---------------------------------|--|--------|------------|------------|-------------------|-------------------|-------------------|
| AI Engines-ML | 8 | 12 | 24 | 34 | 0 | 152 | 304 |
| AI Engines | 0 | 0 | 0 | 0 | 304 | 0 | 0 |
| AIE/AIE-ML Data Memory (Mb) | 4 | 6 | 12 | 17 | 76 | 76 | 152 |
| AIE-ML Shared Memory (Mb) | 48 | 48 | 68 | 68 | 0 | 304 | 304 |
| AIE to NoC Interface Tiles | 2 | 2 | 6 | 6 | 12 | 12 | 12 |
| AIE to PL Interface Tiles | 7 | 7 | 12 | 12 | 27 | 28 | 28 |
| DSP Engines | 90 | 176 | 324 | 464 | 1,312 | 984 | 1,312 |
| System Logic Cells | 43,750 | 80,080 | 229,688 | 328,720 | 981,120 | 820,313 | 1,139,040 |
| CLB Flip-Flops | 40,000 | 73,216 | 210,000 | 300,544 | 897,024 | 750,000 | 1,041,408 |
| LUTs | 20,000 | 36,608 | 105,000 | 150,272 | 448,512 | 375,000 | 520,704 |
| Distributed RAM (Mb) | 0.6 | 1.1 | 3.2 | 4.6 | 13.7 | 11.4 | 15.9 |
| Block RAM Blocks | 24 | 47 | 108 | 155 | 954 | 476 | 600 |
| Block RAM (Mb) | 0.8 | 1.7 | 3.8 | 5.4 | 33.5 | 16.7 | 21.1 |
| UltraRAM Blocks | 24 | 47 | 108 | 155 | 462 | 224 | 264 |
| UltraRAM (Mb) | 6.8 | 13.2 | 30.4 | 43.6 | 129.9 | 63.0 | 74.3 |
| Accelerator RAM (Mb) | 32 | 32 | 32 | 32 | 0 | 0 | 0 |
| APU | Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC | | | | | | |
| RPU | Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC | | | | | | |
| Memory | 256KB On-Chip Memory w/ECC | | | | | | |
| Connectivity | Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2) | | | | | | |
| NoC to PL Master/ Slave Ports | 2 | 2 | 5 | 5 | 21 | 21 | 21 |
| DDR Bus Width | 64 | 64 | 64 | 64 | 192 | 192 | 192 |
| DDR Memory Controllers (DDRM/C) | 1 | 1 | 1 | 1 | 3 | 3 | 3 |
| PCIe w/DMA & CCIX (CPM4) | - | - | - | - | 1 x Gen4x16, CCIX | - | - |
| PCIe w/DMA & CCIX (CPM5) | - | - | - | - | - | 1 x Gen4x16, CCIX | 1 x Gen4x16, CCIX |
| PCIe (PLPCIe4) | - | - | 1 x Gen4x8 | 1 x Gen4x8 | 4 x Gen4x8 | - | - |
| PCIe (PLPCIe5) | - | - | - | - | - | 4 x Gen4x8 | 4 x Gen4x8 |
| 40G Multirate Ethernet MAC | 0 | 0 | 1 | 1 | 2 | 2 | 2 |
| XPIO | 216 | 216 | 216 | 216 | 486 | 486 | 486 |
| HDIO | 0 | 0 | 22 | 22 | 44 | 44 | 44 |
| GTY Transceivers ⁽¹⁾ | 0 | 0 | 0 | 0 | 44 | 0 | 0 |
| GTP Transceivers ⁽¹⁾ | 0 | 0 | 8 | 8 | 0 | 32 ⁽²⁾ | 32 ⁽²⁾ |
| Video Decoder Engines (VDEs) | - | - | - | - | - | 2 | 4 |

Figure 6: Internal Resources of VE2302

Part 2.3: Clock Configuration

The V100 module provides a reference clock and an RTC real-time clock for the PS system and the PL logic respectively, so that the PS system and the PL logic can work independently. The schematic diagram of the clock circuit design is shown in Figure 7 below:

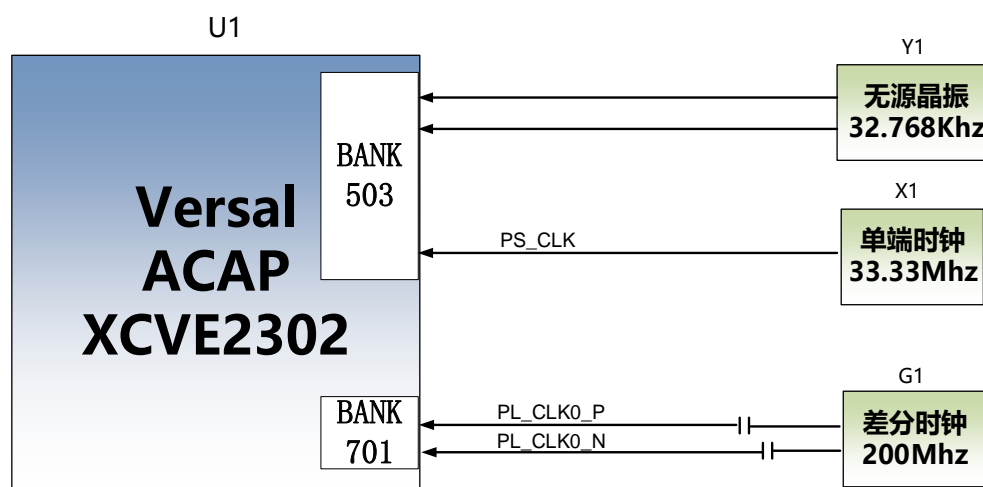


Figure 7: SOM Clock Source

- **PS system RTC real-time clock**

The passive crystal Y1 on the module provides a 32.768KHz real-time clock source for the PS system. The crystal is connected to the pins of RTC _ PADI _ 503 and RTC _ PADO _ 503 of bank 503 of the VE2302 chip.

- **PS system clock source**

The X1 crystal on the module provides a 33.333MHz clock input to the PS system. The input of the clock is connected to the pin PS _ REF _ CLK _ 503 of BANK503 of the VE2302 chip.

- **PL system clock source**

A differential 200MHz PL system clock source is provided on module for the reference clock of the DDR4 controller. The crystal output is connected to the global clock (GC) of PL BANK701, which can be used to drive the DDR4 controller and user logic circuits in the FPGA.

PL clock pin assignment

| Signal name | VE2302 pin name | VE2302 pin number |
|-------------|--------------------------------|-------------------|
| PL_CLK0_N | IO_L24N_GC_XCC_N8P1_M0P103_701 | AC23 |
| PL_CLK0_P | IO_L24P_GC_XCC_N8P0_M0P102_701 | AB23 |

Table 1: PL Clock pin Assignment

Part 2.4: DDR4 DRAM

The V100 module is equipped with four Micron 1GB DDR4 chips, model MT40A512M16LY-062E. Four DDR4 chips are hung on the XPIO of BANK700, 701 and 702, forming a 64-bit data bus bandwidth and a capacity of 4GB. DDR4 SDRAM can run up to 1600MHz (3200Mbps data rate). The specific configuration of DDR4 SDRAM is shown in Table 2 below.

| Tag number | Chip model | Capacity | Manufacturer |
|-----------------|--------------------|--------------|--------------|
| U5, U8, U9, U10 | MT40A512M16LY-062E | 512M x 16bit | Micron |

Table 2: DDR4 SDRAM Configuration

The hardware design of DDR4 needs to strictly consider the signal integrity. We have fully considered the matching resistor/terminal resistor, trace impedance control, and trace equal length control during circuit design and PCB design to ensure the high-speed and stable operation of DDR4. The hardware connection mode of DDR4 is shown in Figure 8:

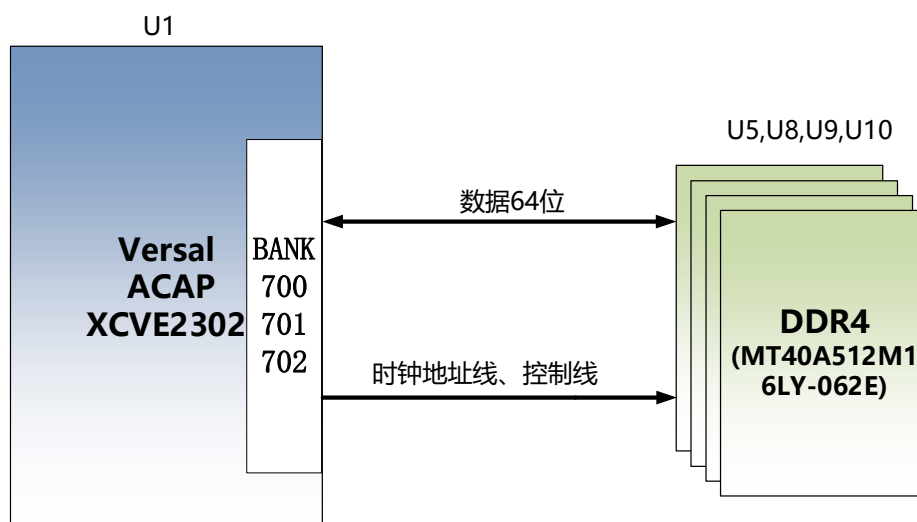


Figure 8: DDR4 DRAM Schematic

DDR4 SDRAM pin assignment

| Signal name | Pin name | Pin number |
|---------------|-------------------------------|------------|
| PL_DDR4_A0 | IO_L18P_XCC_N6P0_M0P36_700 | AB12 |
| PL_DDR4_A1 | IO_L17N_N5P5_M0P35_700 | AE22 |
| PL_DDR4_A2 | IO_L17P_N5P4_M0P34_700 | AD22 |
| PL_DDR4_A3 | IO_L20P_N6P4_M0P40_700 | AB15 |
| PL_DDR4_A4 | IO_L12P_GC_XCC_N4P0_M0P24_700 | AD12 |
| PL_DDR4_A5 | IO_L26P_N8P4_M0P52_700 | AE17 |
| PL_DDR4_A6 | IO_L24P_GC_XCC_N8P0_M0P48_700 | AD16 |
| PL_DDR4_A7 | IO_L6N_GC_XCC_N2P1_M0P13_700 | AG11 |
| PL_DDR4_A8 | IO_L25N_N8P3_M0P51_700 | AE14 |
| PL_DDR4_A9 | IO_L19P_N6P2_M0P38_700 | AB14 |
| PL_DDR4_A10 | IO_L21N_XCC_N7P1_M0P43_700 | AB17 |
| PL_DDR4_A11 | IO_L25P_N8P2_M0P50_700 | AE13 |
| PL_DDR4_A12 | IO_L0N_XCC_N0P1_M0P1_700 | AH12 |
| PL_DDR4_A13 | IO_L24N_GC_XCC_N8P1_M0P49_700 | AD15 |
| PL_DDR4_CLK_N | IO_L15N_XCC_N5P1_M0P31_700 | AD19 |
| PL_DDR4_CLK_P | IO_L15P_XCC_N5P0_M0P30_700 | AC19 |
| PL_DDR4_BA0 | IO_L20N_N6P5_M0P41_700 | AC16 |
| PL_DDR4_BA1 | IO_L12N_GC_XCC_N4P1_M0P25_700 | AD11 |
| PL_DDR4_WE_B | IO_L16N_N5P3_M0P33_700 | AD21 |
| PL_DDR4_CAS_B | IO_L14N_N4P5_M0P29_700 | AD17 |
| PL_DDR4_CS_B | IO_L14P_N4P4_M0P28_700 | AC17 |
| PL_DDR4_ACT_B | IO_L18N_XCC_N6P1_M0P37_700 | AC11 |
| PL_DDR4_RAS_B | IO_L19N_N6P3_M0P39_700 | AC13 |
| PL_DDR4_BG0 | IO_L21P_XCC_N7P0_M0P42_700 | AB18 |
| PL_DDR4_ODT | IO_L23N_N7P5_M0P47_700 | AC22 |

| | | |
|----------------|-------------------------------|------|
| PL_DDR4_CKE | IO_L23P_N7P4_M0P46_700 | AB21 |
| PL_DDR4_RST | IO_L25P_N8P2_M0P104_701 | AC24 |
| PL_DDR4_DQS0_N | IO_L9N_GC_XCC_N3P1_M0P19_700 | AG16 |
| PL_DDR4_DQS0_P | IO_L9P_GC_XCC_N3P0_M0P18_700 | AG17 |
| PL_DDR4_DQS1_N | IO_L3N_XCC_N1P1_M0P7_700 | AH19 |
| PL_DDR4_DQS1_P | IO_L3P_XCC_N1P0_M0P6_700 | AG20 |
| PL_DDR4_DQS2_N | IO_L6N_GC_XCC_N2P1_M0P67_701 | AD27 |
| PL_DDR4_DQS2_P | IO_L6P_GC_XCC_N2P0_M0P66_701 | AC28 |
| PL_DDR4_DQS3_N | IO_L3N_XCC_N1P1_M0P61_701 | AF23 |
| PL_DDR4_DQS3_P | IO_L3P_XCC_N1P0_M0P60_701 | AF24 |
| PL_DDR4_DQS4_N | IO_L15N_XCC_N5P1_M0P85_701 | AA23 |
| PL_DDR4_DQS4_P | IO_L15P_XCC_N5P0_M0P84_701 | Y24 |
| PL_DDR4_DQS5_N | IO_L21N_XCC_N7P1_M0P97_701 | Y27 |
| PL_DDR4_DQS5_P | IO_L21P_XCC_N7P0_M0P96_701 | Y28 |
| PL_DDR4_DQS6_N | IO_L0N_XCC_N0P1_M0P109_702 | U28 |
| PL_DDR4_DQS6_P | IO_L0P_XCC_N0P0_M0P108_702 | U27 |
| PL_DDR4_DQS7_N | IO_L9N_GC_XCC_N3P1_M0P127_702 | N27 |
| PL_DDR4_DQS7_P | IO_L9P_GC_XCC_N3P0_M0P126_702 | P26 |
| PL_DDR4_DM0 | IO_L6P_GC_XCC_N2P0_M0P12_700 | AG12 |
| PL_DDR4_DM1 | IO_L0P_XCC_N0P0_M0P0_700 | AH13 |
| PL_DDR4_DM2 | IO_L9P_GC_XCC_N3P0_M0P72_701 | AE28 |
| PL_DDR4_DM3 | IO_L0P_XCC_N0P0_M0P54_701 | AD24 |
| PL_DDR4_DM4 | IO_L12P_GC_XCC_N4P0_M0P78_701 | V22 |
| PL_DDR4_DM5 | IO_L18P_XCC_N6P0_M0P90_701 | V28 |
| PL_DDR4_DM6 | IO_L3P_XCC_N1P0_M0P114_702 | N28 |
| PL_DDR4_DM7 | IO_L6P_GC_XCC_N2P0_M0P120_702 | U25 |
| PL_DDR4_DQ0 | IO_L8P_N2P4_M0P16_700 | AF14 |
| PL_DDR4_DQ1 | IO_L10N_N3P3_M0P21_700 | AG18 |
| PL_DDR4_DQ2 | IO_L8N_N2P5_M0P17_700 | AG15 |
| PL_DDR4_DQ3 | IO_L10P_N3P2_M0P20_700 | AF18 |
| PL_DDR4_DQ4 | IO_L7P_N2P2_M0P14_700 | AF13 |
| PL_DDR4_DQ5 | IO_L11N_N3P5_M0P23_700 | AF19 |
| PL_DDR4_DQ6 | IO_L7N_N2P3_M0P15_700 | AG13 |
| PL_DDR4_DQ7 | IO_L11P_N3P4_M0P22_700 | AE19 |
| PL_DDR4_DQ8 | IO_L2P_N0P4_M0P4_700 | AH17 |
| PL_DDR4_DQ9 | IO_L4P_N1P2_M0P8_700 | AG21 |
| PL_DDR4_DQ10 | IO_L2N_N0P5_M0P5_700 | AH18 |
| PL_DDR4_DQ11 | IO_L4N_N1P3_M0P9_700 | AH20 |
| PL_DDR4_DQ12 | IO_L1P_N0P2_M0P2_700 | AH14 |
| PL_DDR4_DQ13 | IO_L5N_N1P5_M0P11_700 | AH22 |
| PL_DDR4_DQ14 | IO_L1N_N0P3_M0P3_700 | AH15 |
| PL_DDR4_DQ15 | IO_L5P_N1P4_M0P10_700 | AG22 |

| | | |
|--------------|-------------------------|------|
| PL_DDR4_DQ16 | IO_L8N_N2P5_M0P71_701 | AF26 |
| PL_DDR4_DQ17 | IO_L7N_N2P3_M0P69_701 | AE26 |
| PL_DDR4_DQ18 | IO_L10N_N3P3_M0P75_701 | AH27 |
| PL_DDR4_DQ19 | IO_L8P_N2P4_M0P70_701 | AE27 |
| PL_DDR4_DQ20 | IO_L11N_N3P5_M0P77_701 | AG27 |
| PL_DDR4_DQ21 | IO_L7P_N2P2_M0P68_701 | AD26 |
| PL_DDR4_DQ22 | IO_L11P_N3P4_M0P76_701 | AG26 |
| PL_DDR4_DQ23 | IO_L10P_N3P2_M0P74_701 | AG28 |
| PL_DDR4_DQ24 | IO_L1N_N0P3_M0P57_701 | AE24 |
| PL_DDR4_DQ25 | IO_L1P_N0P2_M0P56_701 | AD25 |
| PL_DDR4_DQ26 | IO_L5P_N1P4_M0P64_701 | AH24 |
| PL_DDR4_DQ27 | IO_L2P_N0P4_M0P58_701 | AF25 |
| PL_DDR4_DQ28 | IO_L4P_N1P2_M0P62_701 | AG23 |
| PL_DDR4_DQ29 | IO_L2N_N0P5_M0P59_701 | AG25 |
| PL_DDR4_DQ30 | IO_L4N_N1P3_M0P63_701 | AH23 |
| PL_DDR4_DQ31 | IO_L5N_N1P5_M0P65_701 | AH25 |
| PL_DDR4_DQ32 | IO_L17P_N5P4_M0P88_701 | Y22 |
| PL_DDR4_DQ33 | IO_L13P_N4P2_M0P80_701 | V23 |
| PL_DDR4_DQ34 | IO_L16P_N5P2_M0P86_701 | Y23 |
| PL_DDR4_DQ35 | IO_L13N_N4P3_M0P81_701 | W24 |
| PL_DDR4_DQ36 | IO_L16N_N5P3_M0P87_701 | AA22 |
| PL_DDR4_DQ37 | IO_L14P_N4P4_M0P82_701 | V24 |
| PL_DDR4_DQ38 | IO_L17N_N5P5_M0P89_701 | AA21 |
| PL_DDR4_DQ39 | IO_L14N_N4P5_M0P83_701 | W25 |
| PL_DDR4_DQ40 | IO_L19P_N6P2_M0P92_701 | V25 |
| PL_DDR4_DQ41 | IO_L20P_N6P4_M0P94_701 | W27 |
| PL_DDR4_DQ42 | IO_L22P_N7P2_M0P98_701 | AA28 |
| PL_DDR4_DQ43 | IO_L19N_N6P3_M0P93_701 | W26 |
| PL_DDR4_DQ44 | IO_L20N_N6P5_M0P95_701 | Y26 |
| PL_DDR4_DQ45 | IO_L23P_N7P4_M0P100_701 | AA26 |
| PL_DDR4_DQ46 | IO_L22N_N7P3_M0P99_701 | AB28 |
| PL_DDR4_DQ47 | IO_L23N_N7P5_M0P101_701 | AB26 |
| PL_DDR4_DQ48 | IO_L2P_N0P4_M0P112_702 | P27 |
| PL_DDR4_DQ49 | IO_L5P_N1P4_M0P118_702 | K27 |
| PL_DDR4_DQ50 | IO_L2N_N0P5_M0P113_702 | R28 |
| PL_DDR4_DQ51 | IO_L4N_N1P3_M0P117_702 | L28 |
| PL_DDR4_DQ52 | IO_L1P_N0P2_M0P110_702 | R27 |
| PL_DDR4_DQ53 | IO_L5N_N1P5_M0P119_702 | K28 |
| PL_DDR4_DQ54 | IO_L1N_N0P3_M0P111_702 | T28 |
| PL_DDR4_DQ55 | IO_L4P_N1P2_M0P116_702 | M27 |
| PL_DDR4_DQ56 | IO_L8P_N2P4_M0P124_702 | P25 |
| PL_DDR4_DQ57 | IO_L10N_N3P3_M0P129_702 | L26 |

| | | |
|--------------|-------------------------|-----|
| PL_DDR4_DQ58 | IO_L8N_N2P5_M0P125_702 | R26 |
| PL_DDR4_DQ59 | IO_L10P_N3P2_M0P128_702 | M26 |
| PL_DDR4_DQ60 | IO_L7P_N2P2_M0P122_702 | T25 |
| PL_DDR4_DQ61 | IO_L11N_N3P5_M0P131_702 | K26 |
| PL_DDR4_DQ62 | IO_L7N_N2P3_M0P123_702 | T26 |
| PL_DDR4_DQ63 | IO_L11P_N3P4_M0P130_702 | J25 |

Table 3: DDR4 SDRAM pin Assignment

Part 2.5: QSPI Flash

The SOM uses two 256Mbit QSPI FLASH chips, model MT25QU256ABA1EW9-0SIT, which uses 1.8 V CMOS voltage standard. Because of its non-volatile nature, QSPI FLASH can be used as a boot image for FPGA systems in use. These images mainly include FPGA bit files, soft-core application code and other user data files.

See the following table 4 for the specific model and relevant parameters of QSPI FLASH.

| Tag number | Type of chip | Capacity | Manufacturer |
|------------|-----------------------|----------|--------------|
| U3, U4 | MT25QU256ABA1EW9-0SIT | 256M Bit | Micron |

Table 4: Model and Parameters of QSPI Flash

QSPI FLASH is connected to the XPIO port of BANK500, the PS part of Versal ACAP chip. In the system design, it is necessary to configure the MIO port function of these PS ends as QSPI FLASH interface.

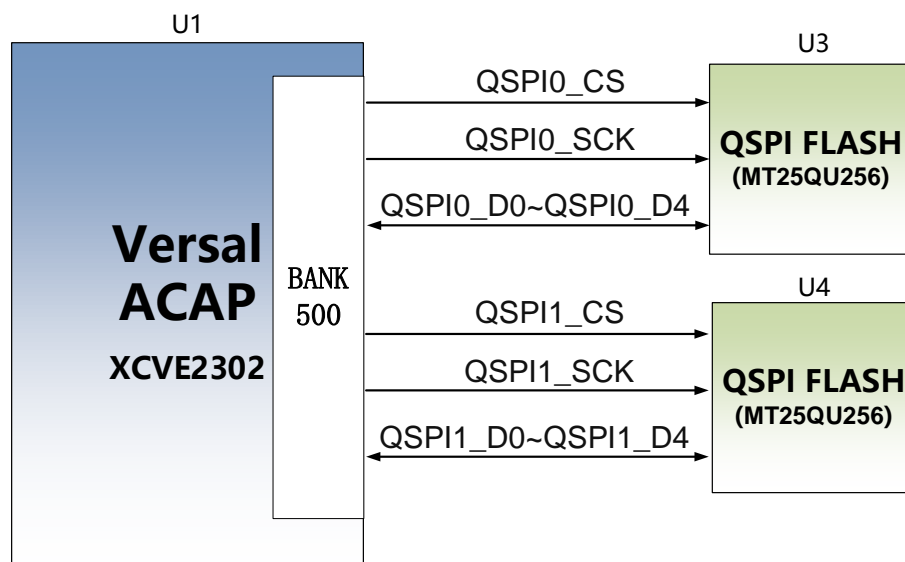


Figure 9: QSPI Flash Connection Diagram

Configure chip pin assignment

| Signal name | Pin name | Pin number |
|-----------------|--------------|------------|
| MIO0_QSPI0_SCLK | PMC_MIO0_500 | AA1 |
| MIO1_QSPI0_IO1 | PMC_MIO1_500 | AB1 |

| | | |
|------------------|---------------|-----|
| MIO2_QSPI0_IO2 | PMC_MIO2_500 | AD1 |
| MIO3_QSPI0_IO3 | PMC_MIO3_500 | AE1 |
| MIO4_QSPI0_IO0 | PMC_MIO4_500 | AF1 |
| MIO5_QSPI0_SS_B | PMC_MIO5_500 | AG1 |
| MIO7_QSPI1_SS_B | PMC_MIO7_500 | AG2 |
| MIO8_QSPI1_IO0 | PMC_MIO8_500 | AE2 |
| MIO9_QSPI1_IO1 | PMC_MIO9_500 | AD2 |
| MIO10_QSPI1_IO2 | PMC_MIO10_500 | AC2 |
| MIO11_QSPI1_IO3 | PMC_MIO11_500 | AB2 |
| MIO12_QSPI1_SCLK | PMC_MIO12_500 | AA3 |

Table 5: Configure Chip pin Assignment

Part 2.6: eMMC Flash

The V100 module is equipped with a large-capacity 8GB eMMC FLASH chip, model MTFC8GAKAJCN-4M, which supports the HS-MMC interface of the JEDEC e-MMC V5.0 standard, and the level supports 1.8 V or 3.3 V. The data width of eMMC FLASH and ACAP connections is 8 bits. Because of its large capacity and non-volatile characteristics, eMMC FLASH can be used as a large-capacity storage device in ACAP system, such as storing ARM applications, system files and other user data files. See Table 6 for the specific model and relevant parameters of eMMC FLASH.

| Tag number | Type of chip | Capacity | Manufacturer |
|------------|-----------------|----------|--------------|
| U8 | MTFC8GAKAJCN-4M | 8G Byte | Micron |

Table 6: Model and parameters of eMMC Flash

eMMC FLASH is connected to PMC MIO port of BANK501 of PS part of Versal ACAP, and these PMC MIO ports shall be configured as EMMC interfaces in system design. Figure 10 shows the part of eMMC Flash in the schematic diagram.

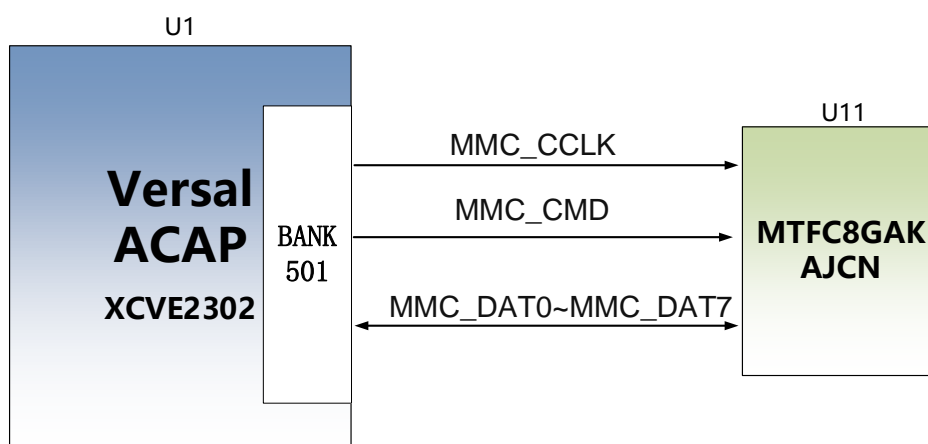


Figure 10: eMMC Flash Connection Diagram

Configure chip pin assignment

| Signal name | Pin name | Pin number |
|-------------|---------------|------------|
| MMC_CCLK | PMC_MIO38_501 | AE8 |
| MMC_CMD | PMC_MIO40_501 | AB8 |
| MMC_DAT0 | PMC_MIO41_501 | AA8 |
| MMC_DAT1 | PMC_MIO42_501 | AA9 |
| MMC_DAT2 | PMC_MIO43_501 | AC9 |
| MMC_DAT3 | PMC_MIO44_501 | AD9 |
| MMC_DAT4 | PMC_MIO45_501 | AE9 |
| MMC_DAT5 | PMC_MIO46_501 | AF9 |
| MMC_DAT6 | PMC_MIO47_501 | AF10 |
| MMC_DAT7 | PMC_MIO48_501 | AD10 |
| MMC_RSTN | PMC_MIO49_501 | AC10 |

Table 7: Configure Chip pin Assignment

Part 2.7: LEDs

The V100 module has a red power supply indicator (PWR) and a configuration LED (DONE). The power indicator lights up when the module is powered on, and the configuration LED lights up when the FPGA configuration program is on. Schematic diagram of hardware connection of LED lamp is shown in Figure 11:

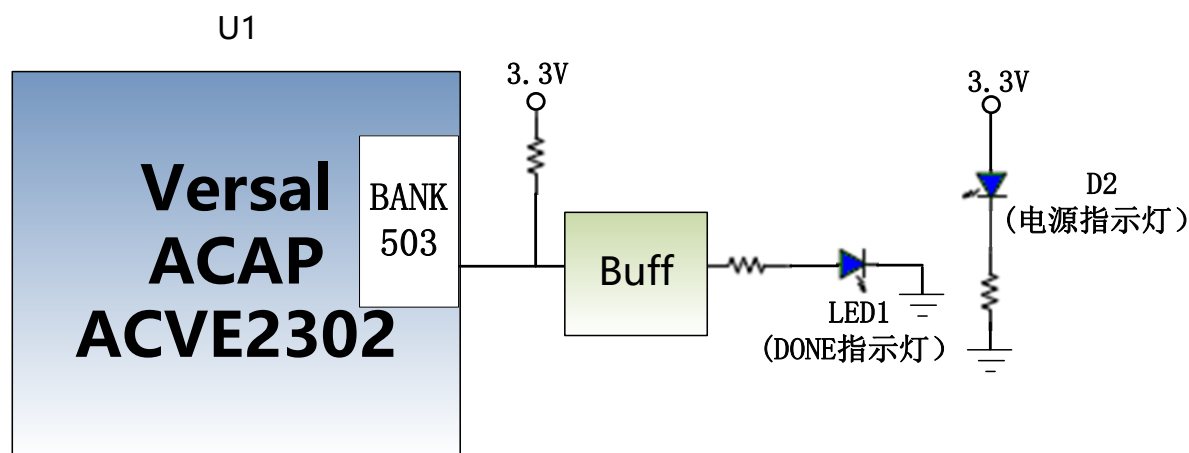


Figure 11: Schematic diagram of hardware connection of led lamp on development board

Part 2.8: Power Supply

The V100 module power supply voltage is 7.5V to 15 V (12 V typical), and the module is powered by connecting the baseboard. The MYMGM1R824ELA5RA power supply chip on the module provides 0.7V core power supply for XCVE2302. In addition, the power supply of BANK503, BANK700 and BANK302 is generated by DCDC chip TLV62130RGT. Power for the BANK703 and GTY transceivers is generated by the LDO chip.

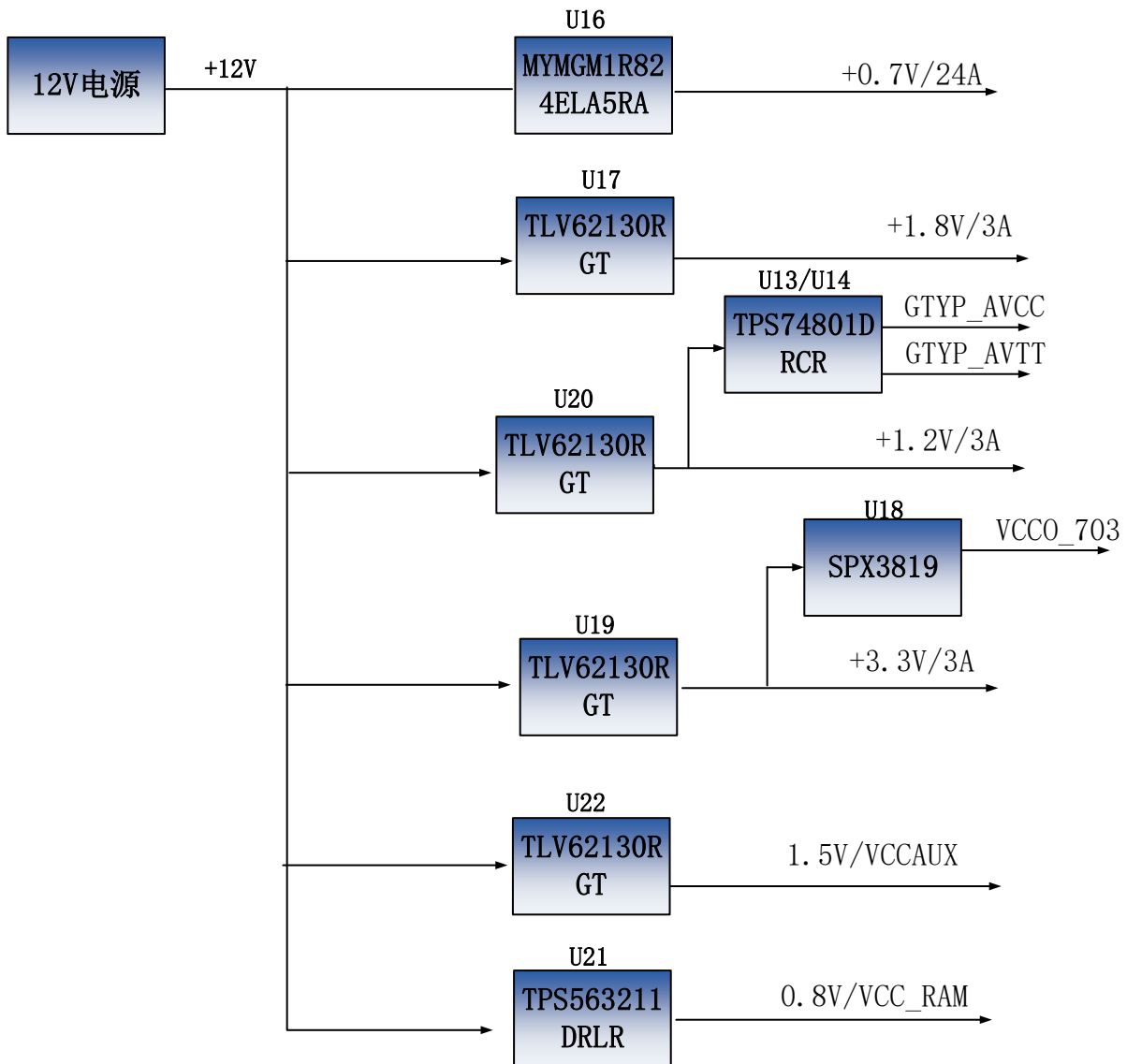


Figure 12: Power Supply

Because the power supply of the Versal ACAP FPGA has a power-on sequence requirement, in the circuit design, we have designed the power-on sequence according to the power supply requirement of the chip as follows:

- VCCIO503(3.3V), VCCO302(3.3V), VCCIO_501/502/503 (1.8V), VCCIO700/701/702(1.2V)
- VCCINT/VCC_PMC/VCC_PSF/P/VCC_PSLP (0.7V)
- VCCBRAM/VCC_SOC/VCC_IO (0.8V)
- VCCBRAM/VCC_SOC/VCC_IO (0.8V)
- GTYP_AVCC (0.9V)
- GTYP_AVTT (1.2V)

Part 2.9: Expansion Interface

A total of two high-speed expansion ports are extended on the back of the module.

Two 160-pin inter-board connectors (Samtec: ADF6-40-03.5-L-4-2-A-TR) are used to connect to the base board. The IO port of the FPGA is connected to these two expansion ports through differential wiring. The

PIN spacing of the connector is 0.5mm, and high-speed data communication is realized with the female connector configuration of the base board.

- **Expansion port U23_AB**

The 160-pin connector U23 is used to connect the VCCIN power supply (+ 12V) of the base board, the ground wire, and the ordinary IO of the FPGA. It should be noted here that the A and B columns of U23 are connected to the IO ports of BANK702 and PS. Pin assignment of U23_AB expansion port is shown in Table 8:

| U23 pin | Signal Name | FPGA Pin number | Level standard | U23 Pin | Signal Name | FPGA Pin number | Level standard |
|---------|-------------|-----------------|----------------|---------|-------------|-----------------|----------------|
| A1 | B702_L17_N | J24 | 1.2V | B1 | B702_L12_N | T24 | 1.2V |
| A2 | B702_L17_P | K23 | 1.2V | B2 | B702_L12_P | U23 | 1.2V |
| A3 | GND | - | Ground | B3 | GND | - | Ground |
| A4 | B702_L25_N | L25 | 1.2V | B4 | B702_L16_N | K24 | 1.2V |
| A5 | B702_L25_P | L24 | 1.2V | B5 | B702_L16_P | L23 | 1.2V |
| A6 | GND | - | Ground | B6 | GND | - | Ground |
| A7 | B702_L24_N | N24 | 1.2V | B7 | B702_L21_N | M21 | 1.2V |
| A8 | B702_L24_P | N23 | 1.2V | B8 | B702_L21_P | N21 | 1.2V |
| A9 | GND | - | Ground | B9 | GND | - | Ground |
| A10 | B702_L22_N | L22 | 1.2V | B10 | B302_L5_N | C12 | 3.3V |
| A11 | B702_L22_P | K21 | 1.2V | B11 | B302_L5_P | D11 | 3.3V |
| A12 | GND | - | Ground | B12 | GND | - | Ground |
| A13 | B302_L2_N | D14 | 3.3V | B13 | B302_L0_N | E14 | 3.3V |
| A14 | B302_L2_P | E13 | 3.3V | B14 | B302_L0_P | F14 | 3.3V |
| A15 | GND | - | Ground | B15 | GND | - | Ground |
| A16 | PS_MIO31 | AD6 | 1.8V | B16 | PS_MIO35 | AC7 | 1.8V |
| A17 | PS_MIO25 | Y4 | 1.8V | B17 | PS_MIO37 | AE7 | 1.8V |
| A18 | GND | - | Ground | B18 | GND | - | Ground |
| A19 | PS_MIO26 | AA5 | 1.8V | B19 | PS_MIO22 | AD4 | 1.8V |
| A20 | PS_MIO33 | AA6 | 1.8V | B20 | PS_MIO19 | AH4 | 1.8V |
| A21 | GND | - | Ground | B21 | GND | - | Ground |
| A22 | PS_MIO32 | AB6 | 1.8V | B22 | PS_MIO20 | AF4 | 1.8V |
| A23 | PS_MIO27 | AB5 | 1.8V | B23 | PS_MIO28 | AC5 | 1.8V |
| A24 | GND | - | Ground | B24 | GND | - | Ground |
| A25 | PS_MIO14 | AC3 | 1.8V | B25 | PS_MIO23 | AC4 | 1.8V |
| A26 | PS_MIO13 | AB3 | 1.8V | B26 | PS_MIO24 | AA4 | 1.8V |
| A27 | GND | - | Ground | B27 | GND | - | Ground |
| A28 | LPD_MIO24 | Y8 | 1.8V | B28 | LPD_MIO4 | Y2 | 1.8V |
| A29 | LPD_MIO23 | Y7 | 1.8V | B29 | LPD_MIO3 | Y1 | 1.8V |
| A30 | GND | - | Ground | B30 | GND | - | Ground |

| | | | | | | | |
|-----|----------|------|--------|-----|-----------|------|--------|
| A31 | LPD_MIO5 | W2 | 1.8V | B31 | LPD_MIO18 | W5 | 1.8V |
| A32 | LPD_MIO2 | W1 | 1.8V | B32 | LPD_MIO12 | W4 | 1.8V |
| A33 | GND | - | Ground | B33 | GND | - | Ground |
| A34 | LPD_MIO7 | U2 | 1.8V | B34 | LPD_MIO1 | U1 | 1.8V |
| A35 | LPD_MIO6 | V2 | 1.8V | B35 | LPD_MIO13 | V4 | 1.8V |
| A36 | GND | - | Ground | B36 | GND | - | Ground |
| A37 | FPGA_TDI | AG10 | 1.8V | B37 | FPGA_TCK | AH10 | 1.8V |
| A38 | FPGA_TMS | AH9 | 1.8V | B38 | FPGA_TDO | AF8 | 1.8V |
| A39 | GND | - | Ground | B39 | GND | - | Ground |
| A40 | +12V | | +12V | B40 | +12V | | +12V |

Table 8: Pin assignment of expansion port U23_AB

- Expansion port U23_CD

The pin assignment of U23B expansion port is shown in Table 9:

| U23 pin | Signal Name | FPGA Pin number | Level standard | U23 Pin | Signal Name | FPGA Pin number | Level standard |
|---------|-------------|-----------------|----------------|---------|-------------|-----------------|----------------|
| C1 | B702_L13_N | R24 | 1.2V | D1 | B702_L14_N | P24 | 1.2V |
| C2 | B702_L13_P | T23 | 1.2V | D2 | B702_L14_P | R23 | 1.2V |
| C3 | GND | - | Ground | D3 | GND | - | Ground |
| C4 | B702_L26_N | M25 | 1.2V | D4 | B702_L18_N | U22 | 1.2V |
| C5 | B702_L26_P | N25 | 1.2V | D5 | B702_L18_P | V21 | 1.2V |
| C6 | GND | - | Ground | D6 | GND | - | Ground |
| C7 | B702_L23_N | J22 | 1.2V | D7 | B702_L19_N | R22 | 1.2V |
| C8 | B702_L23_P | J21 | 1.2V | D8 | B702_L19_P | T21 | 1.2V |
| C9 | GND | - | Ground | D9 | GND | - | Ground |
| C10 | B702_L15_N | M23 | 1.2V | D10 | B702_L20_N | P22 | 1.2V |
| C11 | B702_L15_P | M22 | 1.2V | D11 | B702_L20_P | R21 | 1.2V |
| C12 | GND | - | Ground | D12 | GND | - | Ground |
| C13 | B302_L3_N | D12 | 3.3V | D13 | B302_L4_N | E11 | 3.3V |
| C14 | B302_L3_P | E12 | 3.3V | D14 | B302_L4_P | F11 | 3.3V |
| C15 | GND | - | Ground | D15 | GND | - | Ground |
| C16 | PS_MIO34 | AB7 | 1.8V | D16 | B302_L6_N | C10 | 3.3V |
| C17 | PS_MIO30 | AE6 | 1.8V | D17 | B302_L6_P | D10 | 3.3V |
| C18 | GND | - | Ground | D18 | GND | - | Ground |
| C19 | PS_MIO29 | AD5 | 1.8V | D19 | PS_MIO15 | AE3 | 1.8V |
| C20 | PS_MIO18 | AH3 | 1.8V | D20 | PS_MIO21 | AE4 | 1.8V |
| C21 | GND | - | Ground | D21 | GND | - | Ground |
| C22 | PS_MIO17 | AG3 | 1.8V | D22 | PS_MIO51 | AA10 | 1.8V |
| C23 | PS_MIO16 | AF3 | 1.8V | D23 | PS_MIO50 | AB10 | 1.8V |
| C24 | GND | - | Ground | D24 | GND | - | Ground |

| | | | | | | | |
|-----|-----------|-----|--------|-----|-----------|-----|--------|
| C25 | LPD_MIO22 | T6 | 1.8V | D25 | PS_MIO36 | AD7 | 1.8V |
| C26 | LPD_MIO15 | T5 | 1.8V | D26 | LPD_MIO20 | W6 | 1.8V |
| C27 | GND | - | Ground | D27 | GND | - | Ground |
| C28 | LPD_MIO19 | Y6 | 1.8V | D28 | LPD_MIO21 | U6 | 1.8V |
| C29 | LPD_MIO16 | U5 | 1.8V | D29 | LPD_MIO25 | Y9 | 1.8V |
| C30 | GND | - | Ground | D30 | GND | - | Ground |
| C31 | LPD_MIO11 | Y3 | 1.8V | D31 | LPD_MIO8 | T3 | 1.8V |
| C32 | LPD_MIO17 | V5 | 1.8V | D32 | LPD_MIO14 | T4 | 1.8V |
| C33 | GND | - | Ground | D33 | GND | - | Ground |
| C34 | LPD_MIO10 | V3 | 1.8V | D34 | LPD_MIO0 | T1 | 1.8V |
| C35 | VCC_BATT | | - | D35 | LPD_MIO9 | U3 | 1.8V |
| C36 | GND | - | Ground | D36 | GND | - | Ground |
| C37 | PS_MODE0 | AG8 | 3.3V | D37 | PS_MODE2 | AG6 | 3.3V |
| C38 | PS_MODE1 | AG7 | 3.3V | D38 | PS_MODE3 | AG5 | 3.3V |
| C39 | GND | - | Ground | D39 | GND | - | Ground |
| C40 | +12V | | +12V | D40 | +12V | | +12V |

Table 9: Pin assignment of expansion port U23_CD

- Expansion port U24_AB

The 160-pin connector U24 is used to extend the ordinary IO of BANK302 and BANK703 of the FPGA, as well as the transceiver. See Table 10 for pin assignment of U24_AB expansion port:

| U24 pin | Signal Name | FPGA Pin number | Level standard | U24 Pin | Signal Name | FPGA Pin number | Level standard |
|---------|-------------|-----------------|----------------|---------|-------------|-----------------|----------------|
| A1 | GND | - | Ground | B1 | GND | - | Ground |
| A2 | 104_TX2_N | C4 | 1.2V | B2 | 104_TX0_N | E4 | 1.2V |
| A3 | 104_TX2_P | C5 | 1.2V | B3 | 104_TX0_P | E5 | 1.2V |
| A4 | GND | - | Ground | B4 | GND | - | Ground |
| A5 | 104_TX3_N | B7 | 1.2V | B5 | 104_TX1_N | D7 | 1.2V |
| A6 | 104_TX3_P | B8 | 1.2V | B6 | 104_TX1_P | D8 | 1.2V |
| A7 | GND | - | Ground | B7 | GND | - | Ground |
| A8 | 104_CLK1_N | F6 | 1.2V | B8 | 104_CLK0_N | H6 | 1.2V |
| A9 | 104_CLK1_P | F7 | 1.2V | B9 | 104_CLK0_P | H7 | 1.2V |
| A10 | GND | - | Ground | B10 | GND | - | Ground |
| A11 | 103_TX2_N | J4 | 1.2V | B11 | 103_TX3_N | G4 | 1.2V |
| A12 | 103_TX2_P | J5 | 1.2V | B12 | 103_TX3_P | G5 | 1.2V |
| A13 | GND | - | Ground | B13 | GND | - | Ground |
| A14 | 103_TX0_N | N4 | 1.2V | B14 | 103_TX1_N | L4 | 1.2V |
| A15 | 103_TX0_P | N5 | 1.2V | B15 | 103_TX1_P | L5 | 1.2V |
| A16 | GND | - | Ground | B16 | GND | - | Ground |
| A17 | GND | - | Ground | B17 | GND | - | Ground |

| | | | | | | | |
|-----|------------|-----|--------|-----|------------|-----|--------|
| A18 | B302_L10_N | A14 | 3.3V | B18 | B302_L9_N | A13 | 3.3V |
| A19 | B302_L10_P | B13 | 3.3V | B19 | B302_L9_P | B12 | 3.3V |
| A20 | GND | - | Ground | B20 | GND | - | Ground |
| A21 | B302_L1_N | C13 | 3.3V | B21 | B703_L20_N | D21 | 1.5V |
| A22 | B302_L1_P | C14 | 3.3V | B22 | B703_L20_P | D20 | 1.5V |
| A23 | GND | - | Ground | B23 | GND | - | Ground |
| A24 | B703_L21_N | C21 | 1.5V | B24 | B703_L18_N | H22 | 1.5V |
| A25 | B703_L21_P | B20 | 1.5V | B25 | B703_L18_P | G21 | 1.5V |
| A26 | GND | - | Ground | B26 | GND | - | Ground |
| A27 | B703_L16_N | B23 | 1.5V | B27 | B703_L24_N | F24 | 1.5V |
| A28 | B703_L16_P | C23 | 1.5V | B28 | B703_L24_P | F23 | 1.5V |
| A29 | GND | - | Ground | B29 | GND | - | Ground |
| A30 | B703_L8_N | E26 | 1.5V | B30 | B703_L26_N | D26 | 1.5V |
| A31 | B703_L8_P | F26 | 1.5V | B31 | B703_L26_P | D25 | 1.5V |
| A32 | GND | - | Ground | B32 | GND | - | Ground |
| A33 | B703_L1_N | G28 | 1.5V | B33 | B703_L7_N | G26 | 1.5V |
| A34 | B703_L1_P | H27 | 1.5V | B34 | B703_L7_P | G25 | 1.5V |
| A35 | GND | - | Ground | B35 | GND | - | Ground |
| A36 | B703_L6_N | J26 | 1.5V | B36 | B703_L0_N | H28 | 1.5V |
| A37 | B703_L6_P | H25 | 1.5V | B37 | B703_L0_P | J27 | 1.5V |
| A38 | GND | - | Ground | B38 | GND | - | Ground |
| A39 | B703_L5_N | B28 | 1.5V | B39 | B703_L12_N | H24 | 1.5V |
| A40 | B703_L5_P | C27 | 1.5V | B40 | B703_L12_P | H23 | 1.5V |

Table 10: Pin assignment of expansion port U24_AB

- Expansion port U24_CD

Pin assignment of U24_CD expansion port is shown in Table 11:

| U24 pin | Signal Name | FPGA Pin number | Level standard | U24 Pin | Signal Name | FPGA Pin number | Level standard |
|---------|-------------|-----------------|----------------|---------|-------------|-----------------|----------------|
| C1 | GND | - | Ground | D1 | GND | - | Ground |
| C2 | 104_RX1_N | D1 | 1.2V | D2 | 104_RX0_N | F1 | 1.2V |
| C3 | 104_RX1_P | D2 | 1.2V | D3 | 104_RX0_P | F2 | 1.2V |
| C4 | GND | - | Ground | D4 | GND | - | Ground |
| C5 | 104_RX3_N | A4 | 1.2V | D5 | 104_RX2_N | B1 | 1.2V |
| C6 | 104_RX3_P | A5 | 1.2V | D6 | 104_RX2_P | B2 | 1.2V |
| C7 | GND | - | Ground | D7 | GND | - | Ground |
| C8 | 103_CLK1_N | K6 | 1.2V | D8 | 103_CLK0_N | M6 | 1.2V |
| C9 | 103_CLK1_P | K7 | 1.2V | D9 | 103_CLK0_P | M7 | 1.2V |
| C10 | GND | - | Ground | D10 | GND | - | Ground |
| C11 | 103_RX2_N | K1 | 1.2V | D11 | 103_RX3_N | H1 | 1.2V |

| | | | | | | | |
|-----|------------|-----|--------|-----|------------|-----|--------|
| C12 | 103_RX2_P | K2 | 1.2V | D12 | 103_RX3_P | H2 | 1.2V |
| C13 | GND | - | Ground | D13 | GND | - | Ground |
| C14 | 103_RX1_N | M1 | 1.2V | D14 | 103_RX0_N | P1 | 1.2V |
| C15 | 103_RX1_P | M2 | 1.2V | D15 | 103_RX0_P | P2 | 1.2V |
| C16 | GND | - | Ground | D16 | GND | - | Ground |
| C17 | GND | - | Ground | D17 | GND | - | Ground |
| C18 | B302_L8_N | A11 | 3.3V | D18 | B302_L7_N | A10 | 3.3V |
| C19 | B302_L8_P | B11 | 3.3V | D19 | B302_L7_P | B10 | 3.3V |
| C20 | GND | - | Ground | D20 | GND | - | Ground |
| C21 | B703_L19_N | F21 | 1.5V | D21 | B703_L13_N | G23 | 1.5V |
| C22 | B703_L19_P | E20 | 1.5V | D22 | B703_L13_P | F22 | 1.5V |
| C23 | GND | - | Ground | D23 | GND | - | Ground |
| C24 | B703_L14_N | E23 | 1.5V | D24 | B703_L22_N | A21 | 1.5V |
| C25 | B703_L14_P | E22 | 1.5V | D25 | B703_L22_P | A20 | 1.5V |
| C26 | GND | - | Ground | D26 | GND | - | Ground |
| C27 | B703_L9_N | B25 | 1.5V | D27 | B703_L23_N | B22 | 1.5V |
| C28 | B703_L9_P | C25 | 1.5V | D28 | B703_L23_P | C22 | 1.5V |
| C29 | GND | - | Ground | D29 | GND | - | Ground |
| C30 | B703_L25_N | F25 | 1.5V | D30 | B703_L17_N | A24 | 1.5V |
| C31 | B703_L25_P | E24 | 1.5V | D31 | B703_L17_P | A23 | 1.5V |
| C32 | GND | - | Ground | D32 | GND | - | Ground |
| C33 | B703_L15_N | C24 | 1.5V | D33 | B703_L10_N | A26 | 1.5V |
| C34 | B703_L15_P | D24 | 1.5V | D34 | B703_L10_P | A25 | 1.5V |
| C35 | GND | - | Ground | D35 | GND | - | Ground |
| C36 | B703_L2_N | F28 | 1.5V | D36 | B703_L11_N | B27 | 1.5V |
| C37 | B703_L2_P | G27 | 1.5V | D37 | B703_L11_P | B26 | 1.5V |
| C38 | GND | - | Ground | D38 | GND | - | Ground |
| C39 | B703_L4_N | C28 | 1.5V | D39 | B703_L3_N | E28 | 1.5V |
| C40 | B703_L4_P | D27 | 1.5V | D40 | B703_L3_P | E27 | 1.5V |

Table 11: Pin assignment of expansion port U24_CD

Part 2.10: Structure Diagram

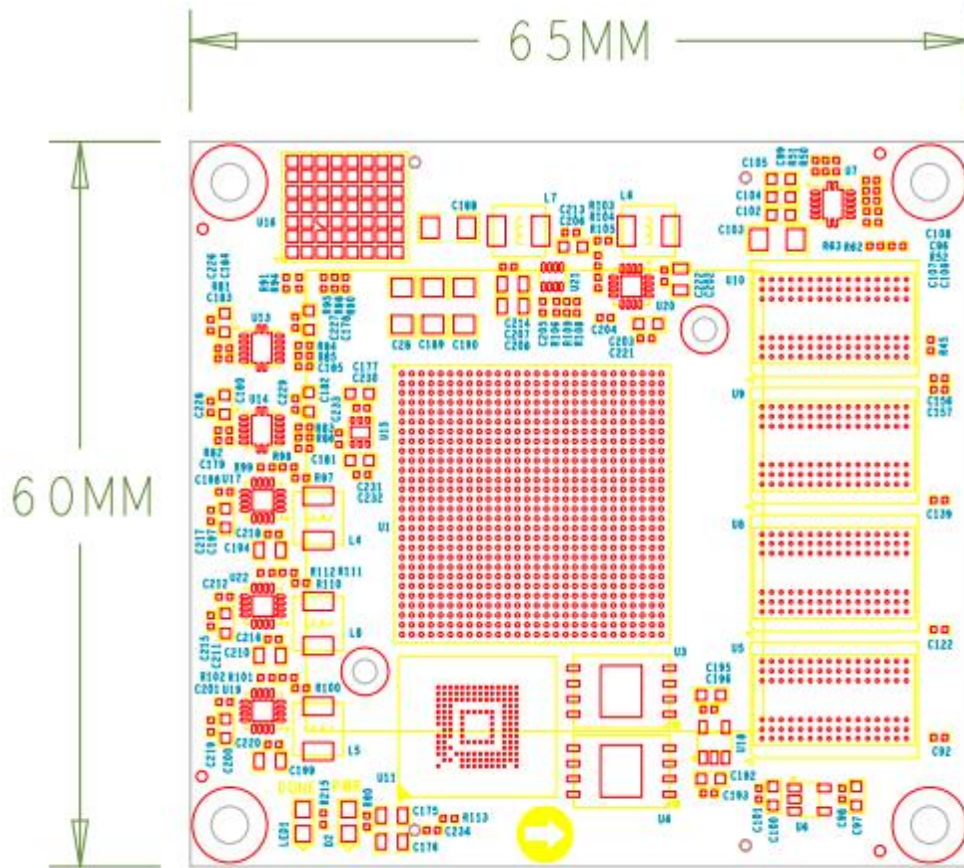


Figure 13: Front View (TOP View)

Part 3: Baseboard

Part 3.1: Introduction

Through the previous function introduction, we can understand the functions of the expansion board.

- 2×Gigabit Ethernet RJ-45 interface
- PCIe3.0×4 connector
- 2×SFP + high-speed optical fiber interface
- 1×USB Uart debugging interface
- 1×USB HOST interface
- 1×LVDS display interface
- 2×MIPI camera interface
- 1×Micro SD deck
- JTAG debug port
- 1×Temperature sensor
- 1×EEPROM
- 1×CANFD communication interface
- 1×22-pin expansion port

Part 3.2: Gigabit Ethernet Interface

There are two Gigabit Ethernet interfaces on the VD100 base board, one is connected to the PS end, and the other is connected to the PL end. It provides users with network communication services through the industrial Ethernet GPHY chip (JL2121-N040I) of JL Semiconductor. JL2121 chip supports 10/100/1,000 Mbps network transmission rate and communicates with MAC layer of FPGA through RGMII interface. JL2121D supports MDI/MDX self-adaptation, various speed self-adaptation and Master/Slave self-adaptation and supports register management of PHY by MDIO bus.

When the JL2121 is powered on, it will detect the level state of some specific IOs to determine its own operating mode. Table 12 describes the default setting information after the GPHY chip is powered on.

| Configure the Pin | Explain | Configuration value |
|-------------------------------------|-------------------------------|---------------------|
| RXD3_ADR0 RXC_ADR1 RXCTL_ADR2 | PHY Address for MDIO/MDC Mode | PHY Address is 001 |
| RXD1_TXDLY | TX clock 2 ns delay | Delay |
| RXD0_RXDLY | RX clock 2 ns delay | Delay |

Table 12: Default configuration values of PHY chip

When the network is connected to Gigabit Ethernet, the data transmission between FPGA and PHY chip JL2121 is communicated through RGMII bus. The transmission clock is 125Mhz, and the data is sampled at the rising edge and falling edge of the clock.

When the network is connected to 100M Ethernet, the data transmission of FPGA and PHY chip JL2121 is

communicated through RMII bus, and the transmission clock is 25 Mhz. Data is sampled on the rising and falling edges of the clock.

The design diagram of Gigabit Ethernet is shown in Figure 14:

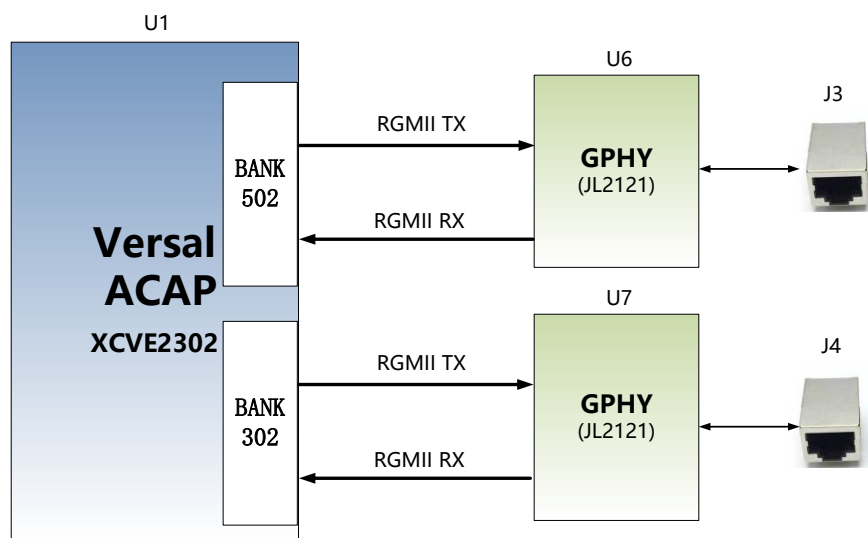


Figure 14: Design of Gigabit Ethernet Interface

The Gigabit Ethernet pin assignments are as follows:

| Signal name | Pin name | Pin number | Remark |
|-------------|-----------|------------|---------------------------------------|
| PHY1_TXCK | LPD_MIO0 | T1 | Ethernet 1RGMII Transmit Clock |
| PHY1_TXD0 | LPD_MIO1 | U1 | Ethernet 1 send data bit0 |
| PHY1_TXD1 | LPD_MIO2 | W1 | Ethernet 1 send data bit1 |
| PHY1_TXD2 | LPD_MIO3 | Y1 | Ethernet 1 send data bit2 |
| PHY1_TXD3 | LPD_MIO4 | Y2 | Ethernet 1 send data bit3 |
| PHY1_TXCTL | LPD_MIO5 | W2 | Ethernet 1 transmit enable signal |
| PHY1_RXCK | LPD_MIO6 | V2 | Ethernet 1RGMII Receive Clock |
| PHY1_RXD0 | LPD_MIO7 | U2 | Ethernet 1 receive data Bit0 |
| PHY1_RXD1 | LPD_MIO8 | T3 | Ethernet 1 receive data Bit1 |
| PHY1_RXD2 | LPD_MIO9 | U3 | Ethernet 1 receive data Bit2 |
| PHY1_RXD3 | LPD_MIO10 | V3 | Ethernet 1 receive data Bit3 |
| PHY1_RXCTL | LPD_MIO11 | Y3 | Ethernet 1 receives data valid signal |
| PHY1_MDIO | PS_MIO51 | AA10 | Ethernet 1MDIO management data |
| PHY1_MDC | PS_MIO50 | AB10 | Ethernet 1MDIO management clock |
| PHY1_RESET | LPD_MIO15 | T5 | Ethernet 1 reset signal |
| PHY2_TXCK | B302_L9_N | A13 | Ethernet 2 RGMII transmit clock |
| PHY2_TXD0 | B302_L8_N | A11 | Ethernet 2 sends data bit0 |
| PHY2_TXD1 | B302_L8_P | B11 | Ethernet 2 send data bit1 |
| PHY2_TXD2 | B302_L7_N | A10 | Ethernet 2 send data bit2 |
| PHY2_TXD3 | B302_L7_P | B10 | Ethernet 2 send data bit3 |
| PHY2_TXCTL | B302_L9_P | B12 | Ethernet 2 send enable signal |
| PHY2_RXCK | B302_L6_P | D10 | Ethernet 2 RGMII Receive Clock |
| PHY2_RXD0 | B302_L5_N | C12 | Ethernet 2 receive data Bit0 |
| PHY2_RXD1 | B302_L5_P | D11 | Ethernet 2 receive data Bit1 |

| | | | |
|------------|------------|-----|---------------------------------------|
| PHY2_RXD2 | B302_L10_N | A14 | Ethernet 2 receive data Bit2 |
| PHY2_RXD3 | B302_L10_P | B13 | Ethernet 2 receive data Bit3 |
| PHY2_RXCTL | B302_L6_N | C10 | Ethernet 2 receives data valid signal |
| PHY2_MDIO | B302_L1_P | C14 | Ethernet 2 MDIO Management Data |
| PHY2_MDC | B302_L1_N | C13 | Ethernet 2 MDIO management clock |
| PHY2_RESET | B703_L12_P | H23 | Ethernet 2 reset signal |

Table 13: Gigabit Ethernet pin assignments

Part 3.3: PCIe3.0X4 Interface

An industrial-grade high-speed data transmission PCIe 3.0 x4 interface is provided on the VD100 base board, and the form factor of the PCIE card meets the requirements of the standard PCIe card electrical specification, so that the PCIE card can be directly used on an x4 PCIe slot of a common PC.

The receiving and transmitting signals of the PCIe interface are directly connected to the GTY transceiver of the FPGA. The TX signals and RX signals of the four channels are connected to the FPGA in the form of differential signals. The communication rate of a single channel can be up to 8G bit bandwidth. The PCIe reference clock is provided by the PCIe slot of the PC to the development board, and the reference clock frequency is 100Mhz.

The design diagram of the PCIe interface of the development board is shown in Figure 15 below, in which the TX transmit signal and the reference clock CLK signal are connected in AC coupling mode.

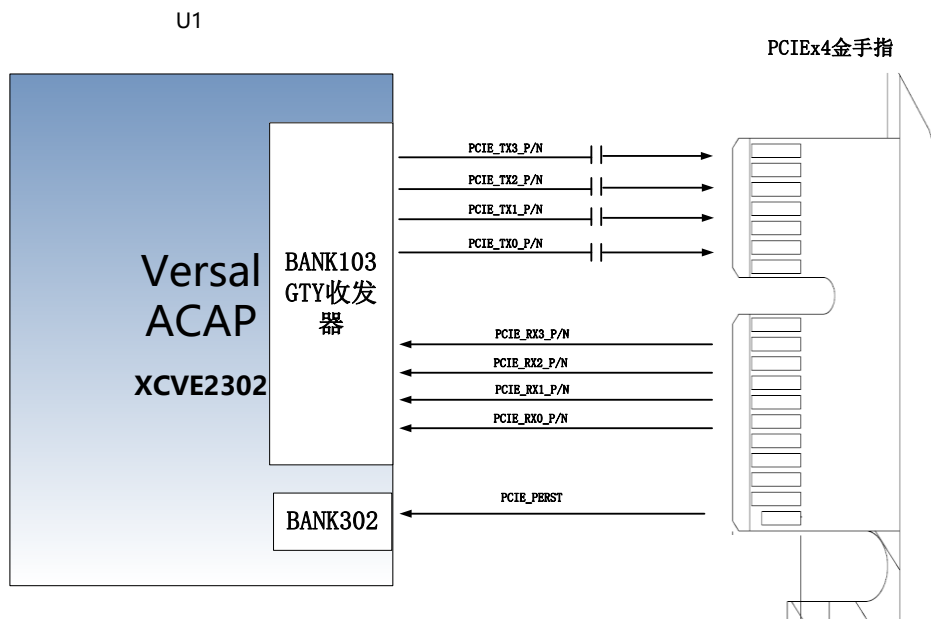


Figure 15: Schematic diagram of PCIe x4 design

The PCIe x4 interface FPGA pin assignments are as follows:

| Network name | FPGA pins | Remark |
|--------------|-----------|--|
| PCIE_RX0_P | P2 | PCIE channel 0 data reception Positive |
| PCIE_RX0_N | P1 | PCIE channel 0 data receiving Negative |
| PCIE_RX1_P | M2 | PCIE channel 1 data reception Positive |

| | | |
|------------|-----|---|
| PCIE_RX1_N | M1 | PCIE Channel 1 Data Receive Negative |
| PCIE_RX2_P | K2 | PCIE channel 2 data reception Positive |
| PCIE_RX2_N | K1 | PCIE Channel 2 Data Receive Negative |
| PCIE_RX3_P | H2 | PCIE channel 3 data reception Positive |
| PCIE_RX3_N | H1 | PCIE Channel 3 Data Reception Negative |
| PCIE_TX0_P | N5 | PCIE channel 0 data sending Positive |
| PCIE_TX0_N | N4 | PCIE channel 0 data transmission Negative |
| PCIE_TX1_P | L5 | PCIE channel 1 data transmission Positive |
| PCIE_TX1_N | L4 | PCIE channel 1 data transmission Negative |
| PCIE_TX2_P | J5 | PCIE channel 2 data transmission Positive |
| PCIE_TX2_N | J4 | PCIE channel 2 data transmission Negative |
| PCIE_TX3_P | G5 | PCIE channel 3 data transmission Positive |
| PCIE_TX3_N | G4 | PCIE channel 3 data transmission Negative |
| PCIE_CLK_P | M7 | PCIE reference clock Positive |
| PCIE_CLK_N | M6 | Reference clock Negative for PCIE |
| PCIE_PERST | B13 | PCIE reset signal |

Table 14: PCIe x4 interface FPGA pin assignments

Part 3.4: SFP+ Fiber Interface

There are two SFP + optical fiber interfaces on the VD100 development board. Users can buy SFP optical modules (1.25G, 2.5G and 10G optical modules on the market) and insert them into these two optical fiber interfaces for optical data communication. The two channels of optical fiber interfaces are respectively connected with the two channels of RX/TX of the GTY transceiver of BANK104 of the FPGA, the TX signal and the RX signal are connected with the FPGA and the optical module through a blocking capacitor in a differential signal mode, and the data rate of each channel of TX sending and RX receiving is up to 10Gb/s. The reference clock for the GTY transceiver of BANK104 is provided by a 156.25Mhz differential crystal oscillator.

The schematic diagram of FPGA and SFP fiber design is shown in Figure 16 below:

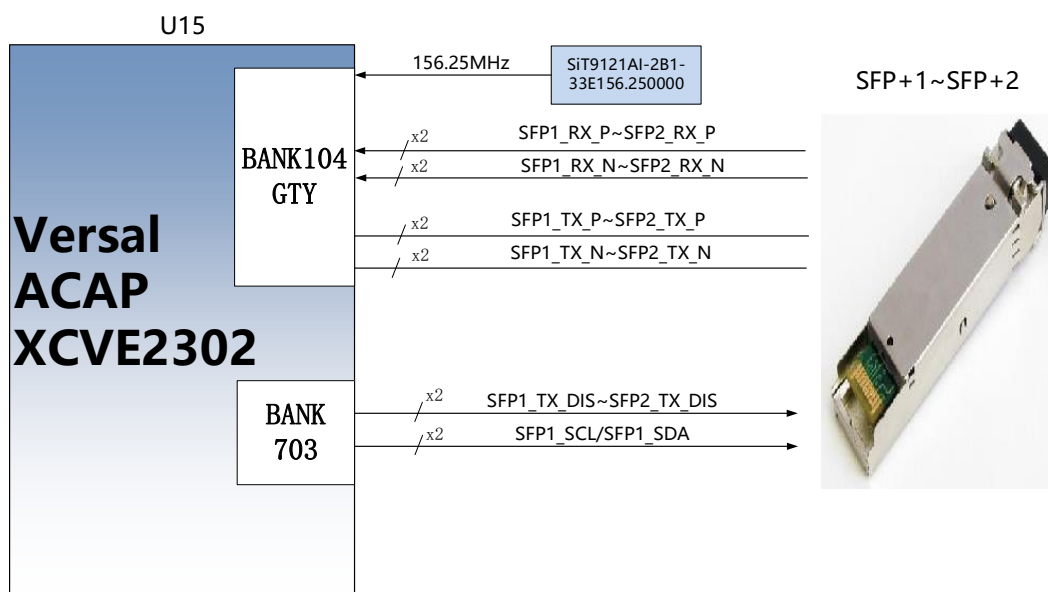


Figure 16: Schematic Diagram of Optical Fiber Design

The first optical interface FPGA pin assignment is as follows:

| Network name | FPGA pins | Remark |
|--------------|-----------|---|
| SFP1_TX_P | E5 | SFP optical module data sending Positive |
| SFP1_TX_N | E4 | SFP optical module data sending Negative |
| SFP1_RX_P | F2 | SFP optical module data receiving Positive |
| SFP1_RX_N | F1 | SFP optical module data receiving Negative |
| SFP1_TX_DIS | D26 | SFP optical module light emission disable, low active |
| SFP1_SCL | D21 | I2C clock signal |
| SFP1_SDA | D20 | I2C Data Signal |

Table 15: The first optical interface FPGA pin assignment

The second optical interface FPGA pin assignment is as follows:

| Network name | FPGA pins | Remark |
|--------------|-----------|---|
| SFP2_TX_P | D8 | SFP optical module data sending Positive |
| SFP2_TX_N | D7 | SFP optical module data sending Negative |
| SFP2_RX_P | D2 | SFP optical module data receiving Positive |
| SFP2_RX_N | D1 | SFP optical module data receiving Negative |
| SFP2_TX_DIS | D25 | SFP optical module light emission disable, low active |
| SFP_CLK_N | H6 | FPGA Input Clock Negative |
| SFP_CLK_P | H7 | FPGA Input Clock Positive |

Table 16: The second optical interface FPGA pin assignment

Part 3.5: USB to Serial Port

The VD100 base board is equipped with an Uart to USB interface connected to the PS side. The conversion chip uses Silicon Labs CP2102GM USB-UAR chip, and the USB interface uses MINI USB interface, which can be connected to the USB port of the PC with a USB cable for serial data communication.

The schematic diagram of USB Uart circuit design is shown in Figure 17.

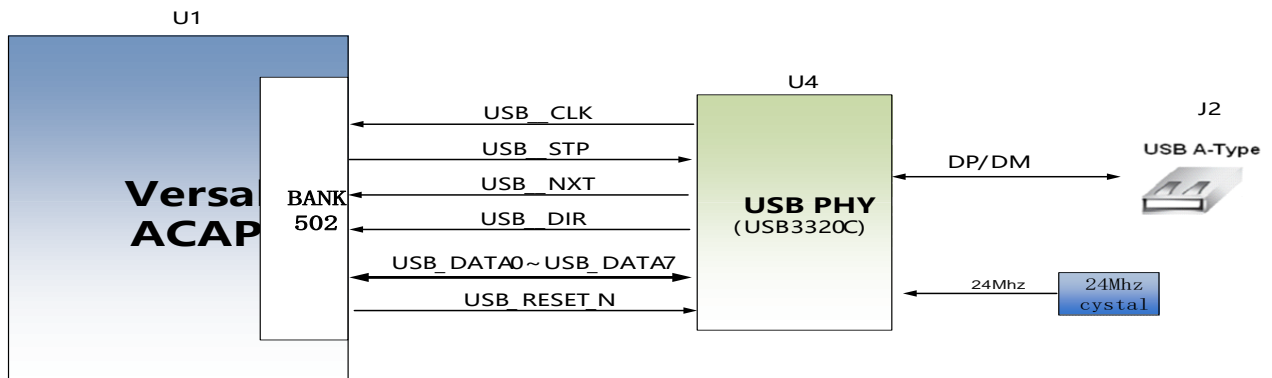


Figure 17: Schematic diagram of USB to serial port

UART-to-serial FPGA pin assignment:

| Signal name | FPGA pin name | FPGA pin number | Remark |
|-------------|---------------|-----------------|------------------|
| PS_UART0_RX | LPD_MIO16 | U5 | Uart Data Input |
| PS_UART0_TX | LPD_MIO17 | V5 | Uart Data Output |

Table 17: UART-to-serial FPGA pin assignment

Part 3.6: USB2.0 Interface

There is one USB2.0 interface on the VD100 base board, which supports HOST working mode. USB2.0 is connected to the external USB3320C chip through the ULPI interface to achieve high-speed USB2.0 data communication.

USB interface is flat USB interface (USB Type A), which is convenient for users to connect different USB Slave peripherals (such as USB mouse, keyboard, or U disk) at the same time. The schematic diagram of USB2.0 connection is shown in Figure 18:

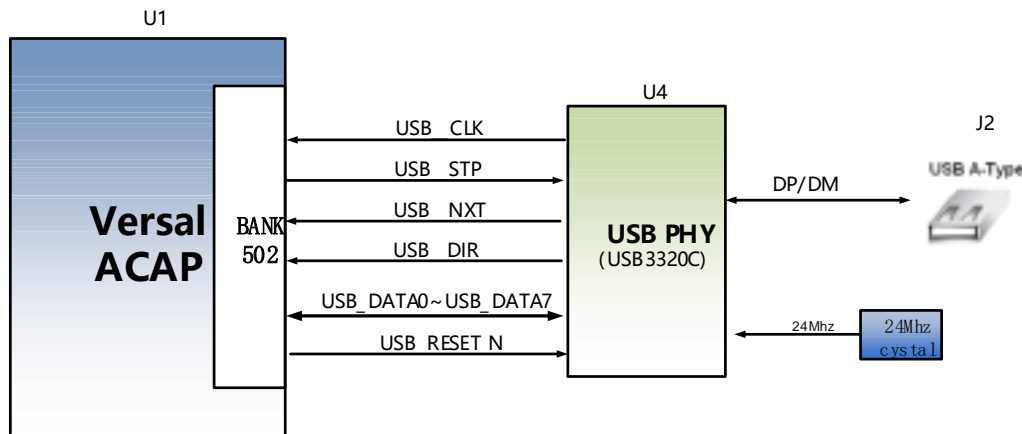


Figure 18: Schematic diagram of USB3.0 interface

USB interface pin assignment:

| Signal name | Pin name | Pin number | Remark |
|-------------|----------|------------|------------------------------|
| USB_DATA0 | PS_MIO14 | AC3 | USB2.0 Data Bit0 |
| USB_DATA1 | PS_MIO15 | AE3 | USB2.0 Data Bit1 |
| USB_DATA2 | PS_MIO16 | AF3 | USB2.0 Data Bit2 |
| USB_DATA3 | PS_MIO17 | AG3 | USB2.0 Data Bit3 |
| USB_DATA4 | PS_MIO19 | AH4 | USB2.0 Data Bit4 |
| USB_DATA5 | PS_MIO20 | AF4 | USB2.0 Data Bit5 |
| USB_DATA6 | PS_MIO21 | AE4 | USB2.0 Data Bit6 |
| USB_DATA7 | PS_MIO22 | AD4 | USB2.0 Data Bit 7 |
| USB_STP | PS_MIO24 | AA4 | USB2.0 stop signal |
| USB_DIR | PS_MIO23 | AC4 | USB2.0 data direction signal |
| USB_CLK | PS_MIO18 | AH3 | USB2.0 clock signal |
| USB_NXT | PS_MIO25 | Y4 | USB2.0 next data signal |
| USB_RESET_N | PS_MIO13 | AB3 | USB2.0 reset signal |

Table 18: USB interface pin assignment

Part 3.7: LVDS Display Interface

The base board contains a LVDS display interface, which can be used to connect our 7-inch display module (AN7000). The LVDS interface is a 40-pin FPC connector, which has four pairs of LVDS data and one pair of clock, and other control signals are connected to the differential IO pin of BANK703 through the level conversion chip, and the level standard is 1.5V.

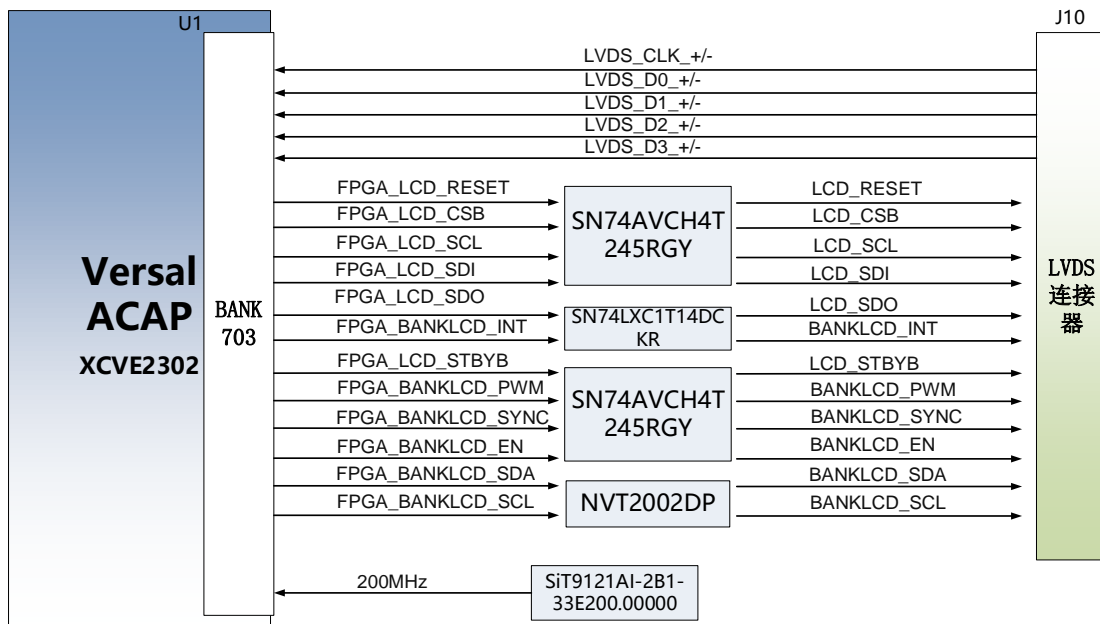


Figure 19: LVDS Interface Design Schematic Diagram

LVDS interface pin assignment:

| Signal name | Pin name | Pin number | Remark |
|--------------|------------|------------|--|
| LVDS_CLK- | B703_L17_N | A24 | LVDS screen input clock negative |
| LVDS_CLK+ | B703_L17_P | A23 | LVDS screen input clock positive |
| LVDS_D0- | B703_L13_N | G23 | Input data DATA0 of LVDS screen is negative. |
| LVDS_D0+ | B703_L13_P | F22 | Data DATA0 input by LVDS screen is positive |
| LVDS_D1- | B703_L22_N | A21 | LVDS screen input data DATA 1 negative |
| LVDS_D1+ | B703_L22_P | A20 | Data DATA1 input by LVDS screen is positive |
| LVDS_D2- | B703_L23_N | B22 | Data DATA2 input by LVDS screen is negative. |
| LVDS_D2+ | B703_L23_P | C22 | Data DATA2 input by LVDS screen is positive |
| LVDS_D3- | B703_L10_N | A26 | Input data DATA3 of LVDS screen is negative. |
| LVDS_D3+ | B703_L10_P | A25 | Data DATA3 input by LVDS screen is positive |
| FPGA_LCD_SDI | B703_L11_N | B27 | LCD panel serial interface address and SPI data input |
| FPGA_LCD_CSB | B703_L11_P | B26 | LCD screen serial interface chip SPI chip selection signal |
| FPGA_LCD_SCL | B703_L3_N | E28 | LCD panel serial interface SPI clock |

| | | | |
|-------------------|------------|-----|---|
| FPGA_LCD_SDO | B703_L9_N | B25 | LCD screen serial interface SPI data output |
| FPGA_LCD_RESET | B703_L3_P | E27 | LCD screen reset signal |
| FPGA_LCD_STBYB | B703_L25_N | F25 | LCD screen mode setting signal |
| FPGA_BANKLCD_SDA | B703_L12_N | H24 | Backlight I2C data |
| FPGA_BANKLCD_SCL | B703_L14_P | E22 | Backlight I2C clock |
| FPGA_BANKLCD_INT | B703_L9_P | C25 | Backlight fault interrupt signal |
| FPGA_BANKLCD_EN | B703_L25_P | E24 | Backlight enable signal |
| FPGA_BANKLCD_PWM | B703_L15_N | C24 | Backlight brightness adjustment signal |
| FPGA_BANKLCD_SYNC | B703_L15_P | D24 | Backlight synchronous boost input |
| LVDS_CLK_N | B703_L24_N | F24 | FPGA Input Clock Negative |
| LVDS_CLK_P | B703_L24_P | F23 | FPGA input clock positive |

Table 19: LVDS interface pin assignment

Part 3.8: MIPI Interface

The VD100 base board contains two MIPI 4 Lane camera interfaces, which can be used to connect our MIPI OS05A20 camera module (AN5020). The MIPI interface is a 20-pin FPC connector, which is the data of four LANEs and a pair of clocks and is connected to the differential IO pin of BANK702, with a level standard of 1.2V. Other control signals are connected to the IO pin of BANK703 through level conversion, with a level standard of 1.5V.

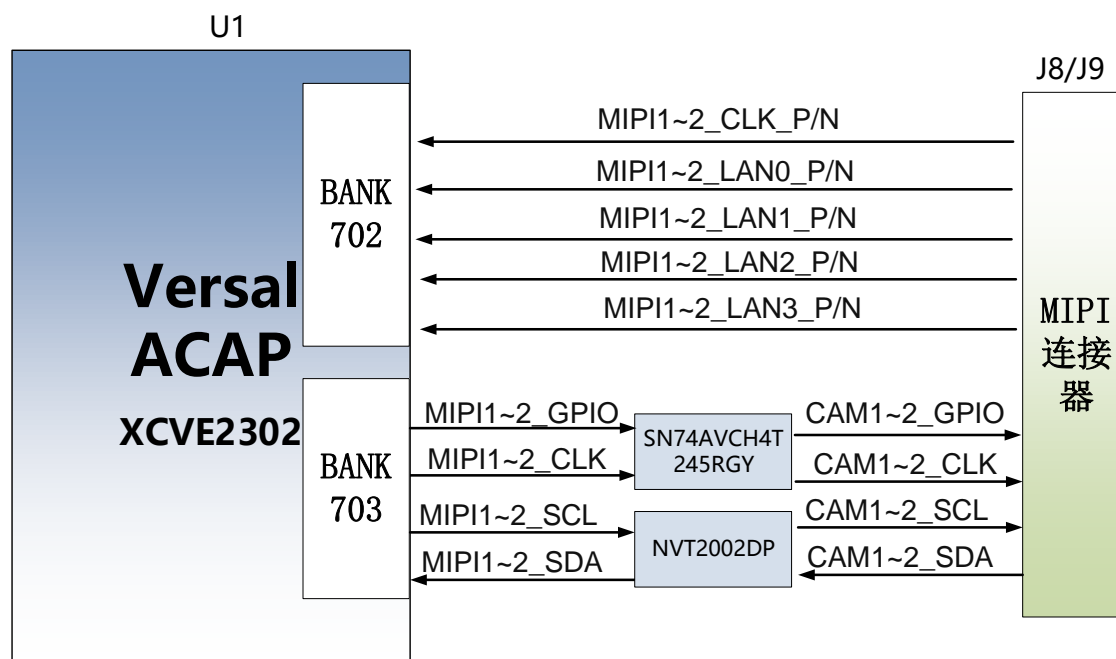


Figure 20: Schematic Diagram of MIPI Interface Design

MIPI interface pin assignment:

| Signal name | Pin name | Pin number | Remark |
|--------------|------------|------------|---------------------------------|
| MIPI1_CLK_N | B702_L12_N | T24 | MIPI1 Input Clock Negative |
| MIPI1_CLK_P | B702_L12_P | U23 | MIPI1 Input Clock Positive |
| MIPI1_LAN0_N | B702_L13_N | R24 | MIPI1 Input Data LANE0 Negative |
| MIPI1_LAN0_P | B702_L13_P | T23 | MIPI1 Input Data LANE0 Positive |

| | | | |
|--------------|------------|-----|---------------------------------|
| MIPI1_LAN1_N | B702_L14_N | P24 | MIPI1 input data LANE1 negative |
| MIPI1_LAN1_P | B702_L14_P | R23 | MIPI1 Input Data LANE1 Positive |
| MIPI1_LAN2_N | B702_L16_N | K24 | MIPI1 input data LANE2 negative |
| MIPI1_LAN2_P | B702_L16_P | L23 | MIPI1 input data LANE2 positive |
| MIPI1_LAN3_N | B702_L15_N | M23 | MIPI1 input data LANE3 negative |
| MIPI1_LAN3_P | B702_L15_P | M22 | MIPI1 input data LANE3 positive |
| MIPI1_SDA | B703_L2_N | F28 | I2C data for MIPI1 camera |
| MIPI1_SCL | B703_L2_P | G27 | I2C clock for MIPI1 camera |
| MIPI1_GPIO | B703_L7_N | G26 | GPIO control of MIPI1 camera |
| MIPI1_CLK | B703_L7_P | G25 | Clock input for MIPI1 camera |
| MIPI2_CLK_N | B702_L18_N | U22 | MIPI2 Input Clock Negative |
| MIPI2_CLK_P | B702_L18_P | V21 | MIPI2 Input Clock Positive |
| MIPI2_LAN0_N | B702_L19_N | R22 | MIPI2 Input Data LANE0 Negative |
| MIPI2_LAN0_P | B702_L19_P | T21 | MIPI2 Input Data LANE0 Positive |
| MIPI2_LAN1_N | B702_L20_N | P22 | MIPI2 input data LANE1 negative |
| MIPI2_LAN1_P | B702_L20_P | R21 | MIPI2 Input Data LANE1 Positive |
| MIPI2_LAN2_N | B702_L21_N | M21 | MIPI2 input data LANE2 negative |
| MIPI2_LAN2_P | B702_L21_P | N21 | MIPI2 input data LANE2 positive |
| MIPI2_LAN3_N | B702_L22_N | L22 | MIPI2 input data LANE3 negative |
| MIPI2_LAN3_P | B702_L22_P | K21 | MIPI2 input data LANE3 positive |
| MIPI2_SDA | B703_L4_N | C28 | I2C data for MIPI2 camera |
| MIPI2_SCL | B703_L4_P | D27 | I2C clock for MIPI2 camera |
| MIPI2_GPIO | B703_L0_N | H28 | GPIO control of MIPI2 camera |
| MIPI2_CLK | B703_L0_P | J27 | Clock input for MIPI2 camera |

Table 20: MIPI interface pin assignment

Part 3.9: SD Card

The VD100 base board includes a Micro-type SD card interface to provide user access to the SD card memory, which is used to store the BOOT program of the XCVE2302 chip, the Linux operating system kernel, the file system, and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of the XCVE2302. Because the VCCIO of the 501 is set to 1.8V, but the data level of the SD card is 3.3V, we connect it through the TXS02612 level shifter. The schematic diagram of the XCVE2302 PS and SD card connectors is shown in Figure 21.

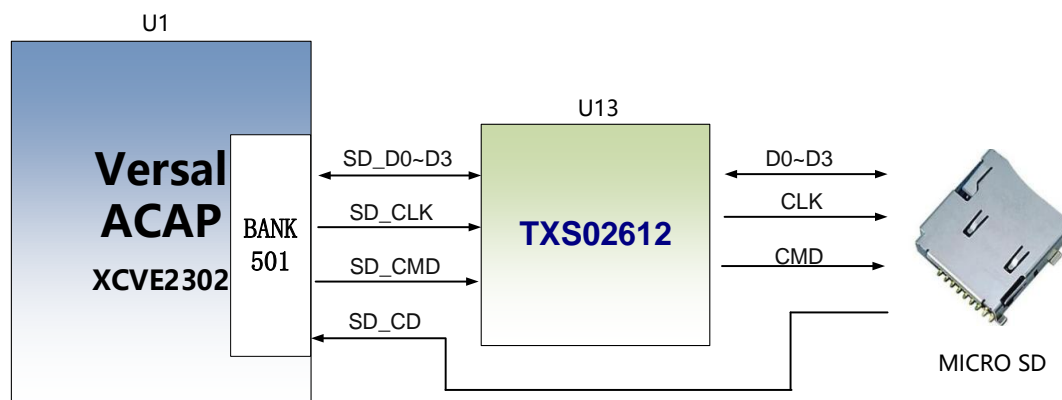


Figure 21: SD card connection diagram

SD card slot pin assignment:

| Signal name | Pin name | Pin number | Remark |
|-------------|----------|------------|--------------------------|
| SD_CLK | PS_MIO26 | AA5 | SD clock signal |
| SD_CD | PS_MIO28 | AC5 | SD card detection signal |
| SD_CMD | PS_MIO29 | AD5 | SD command signal |
| SD_D0 | PS_MIO30 | AE6 | SD Data 0 |
| SD_D1 | PS_MIO31 | AD6 | SD Data 1 |
| SD_D2 | PS_MIO32 | AB6 | SD Data 2 |
| SD_D3 | PS_MIO33 | AA6 | SD Data 3 |

Table 21: SD card slot pin assignment

Part 3.10: EEPROM 24LC04 & Temperature Sensor

The VD100 development board is equipped with an EEPROM with a model of 24LC04 and a capacity of 4Kbit (2 * 256 * 8 bit), which is connected to the PS terminal for communication through the IIC bus. In addition, there is a high-precision, low-power, digital temperature sensor chip on the board. The model is LM75 of ON Semiconductor Company. The temperature accuracy of LM75 chip is 0.5 degrees. The EEPROM and temperature sensor are mounted on the Bank501 MIO of the Versal ACAP via the I2C bus. Figure 22 shows the principle diagram of EEPROM and temperature sensor.

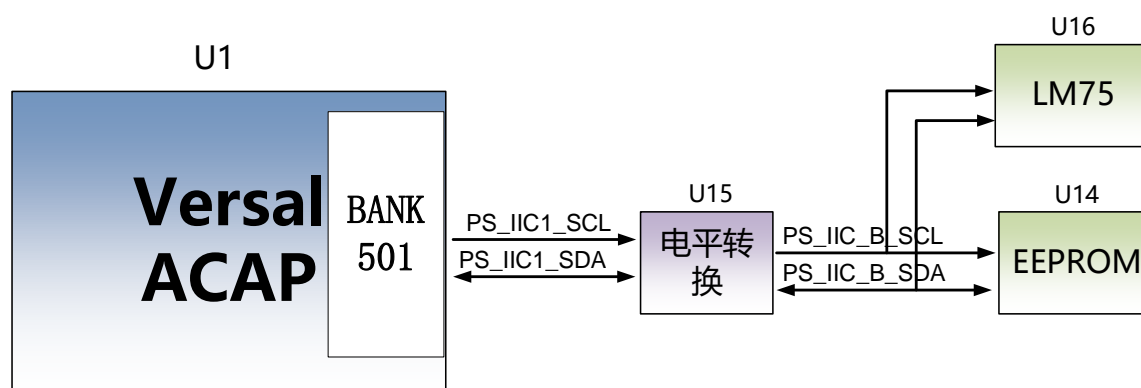


Figure 22: Schematic diagram of EEPROM and sensor

The EEPROM communication pins are assigned as follows:

| Signal name | Pin name | Pin number | Remark |
|-------------|----------|------------|------------------|
| PS_IIC1_SCL | PS_MIO34 | AB7 | I2C clock signal |
| PS_IIC1_SDA | PS_MIO35 | AC7 | I2C Data Signal |

Table 22: EEPROM communication pins assignment

Part 3.11: JTAG Interface

A JTAG interface is reserved on the development board for downloading FPGA programs or solidified programs to FLASH. To avoid the damage to the FPGA caused by hot plugging, we add a protection diode on the JTAG signal to ensure that the voltage of the signal is within the acceptable range of the FPGA to avoid the damage to the FPGA.

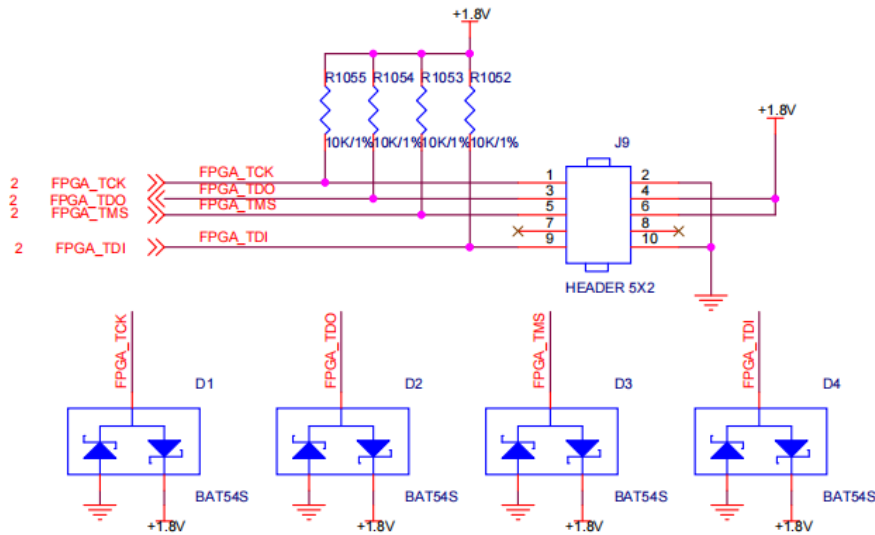


Figure 23: Schematic diagram of JTAG interface

Be careful not to hot plug when plugging the JTAG cable.

Part 3.12: CANFD Communication Interface

There is one CAN/CANFD communication interface on the VD100 base board, which is connected to the MIO interface of BANK502 at the PS system end. The TJA1051T/3/1J chip of NXP Company is selected as the CANFD transceiver chip to provide CAN communication services for users.

Figure 24 is the connection diagram of CAN transceiver chip at PS end.

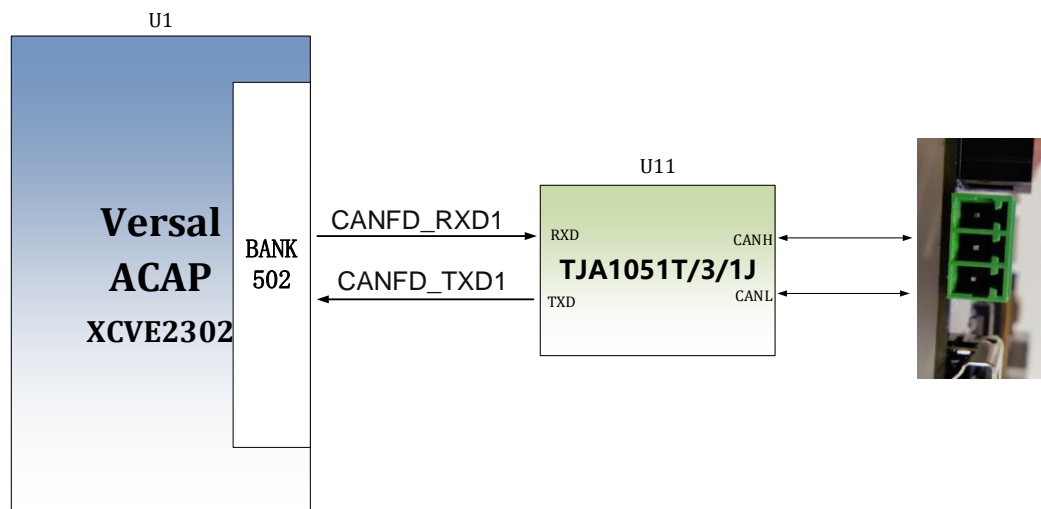


Figure 24: Schematic diagram of connection of CAN transceiver chip at PS end

The CAN communication pins are assigned as follows:

| Signal name | Pin name | Pin number | Remark |
|-------------|-----------|------------|--------------------|
| CANFD_TXD1 | LPD_MIO23 | Y7 | CAN1 transmitter |
| CANFD_RXD1 | LPD_MIO22 | T6 | CAN1 receiving end |

Table 23: CAN communication pins assignment

Part 3.13: PMOD Expansion Port

One expansion port J55 of PMOD with standard spacing of 12-pin 2.54 mm is reserved on the base board for connecting external modules or equipment. The expansion port has 2 channels of 3.3V power supply, 2 channels of ground and 8 channels of IO port. The standard level for IO is 3.3V.

Do not connect directly to the IO of a 5V device to avoid burning out the FPGA. If you want to connect the IO of 5V device, you need to connect the level conversion chip.

The circuit of the expansion port (55) is shown in Figure 25.

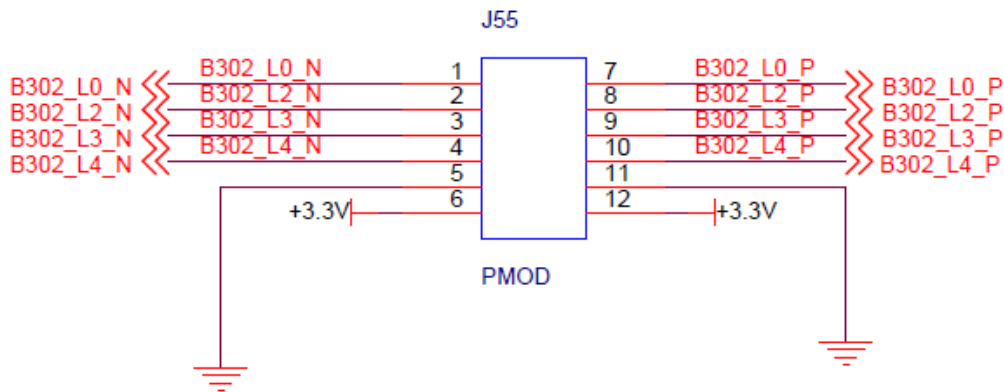


Figure 25: Schematic Diagram of Expansion Port J55

Pin assignment of J55 expansion port FPGA:

| J55 pin number | FPGA Pin name | FPGA Pin number | J55 pin number | FPGA Pin name | FPGA Pin number |
|----------------|---------------|-----------------|----------------|---------------|-----------------|
| 1 | B302_L0_N | E14 | 7 | B302_L0_P | F14 |
| 2 | B302_L2_N | D14 | 8 | B302_L2_P | E13 |
| 3 | B302_L3_N | D12 | 9 | B302_L3_P | E12 |
| J4 | B302_L4_N | E11 | 10 | B302_L4_P | F11 |
| 5 | Ground | - | 11 | Ground | - |
| 6 | +3.3V | - | 12 | +3.3V | - |

Table 24: J55 expansion port pins assignment

Part 3.14: Keys

The base board contains two user keys KEY 1 ~ KEY2, both of which are connected to the common IO of the FPGA, one of which is connected to the PL end and the other to the PS end. The low level of the key is valid. When the key is pressed, the IO input voltage of the FPGA is low. When no key is pressed, the IO input voltage of the FPGA is high. The circuit of the key part is as shown in Figure 26.

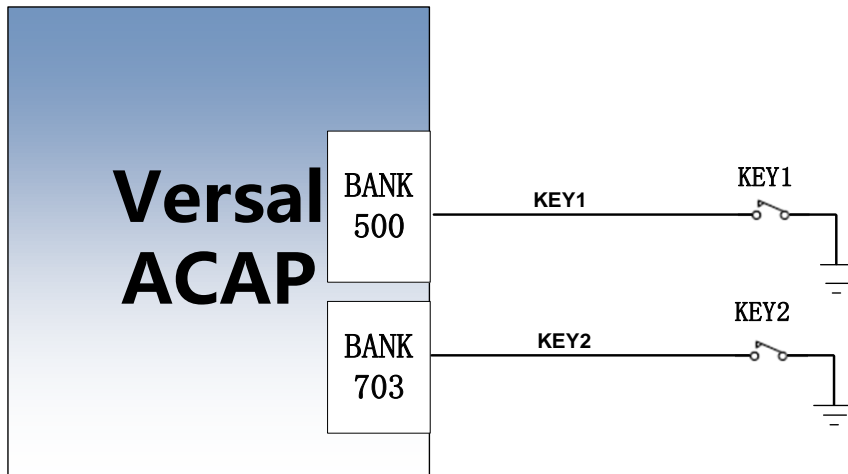


Figure 26: Schematic diagram of key hardware design

Key FPGA pin assignment

| Signal name | FPGA pin name | FPGA pin number | Remark |
|-------------|---------------|-----------------|------------|
| PS_LED1 | LPD_MIO25 | Y9 | User key 1 |
| PL_KEY1 | B703_L19_N | F21 | User key 2 |

Table 25: Key FPGA pin assignment

Part 3.15: LEDs

There are three red LEDs on the base board, one of which is the power indicator (PWR) and two of which are the user LEDs (LED 1 ~ LED 2). When power is applied to the board, the power indicator illuminates. The user LED1 and LED2 are connected to the common IO of the FPGA, one is connected to the PL terminal, and the other is connected to the PS terminal. When the IO voltage connected with the user LED is configured as high level, the user LED will be on. When the IO voltage connected is configured as low level, the user LED will be off. Schematic diagram of LED light hardware connection is shown in Figure 27.

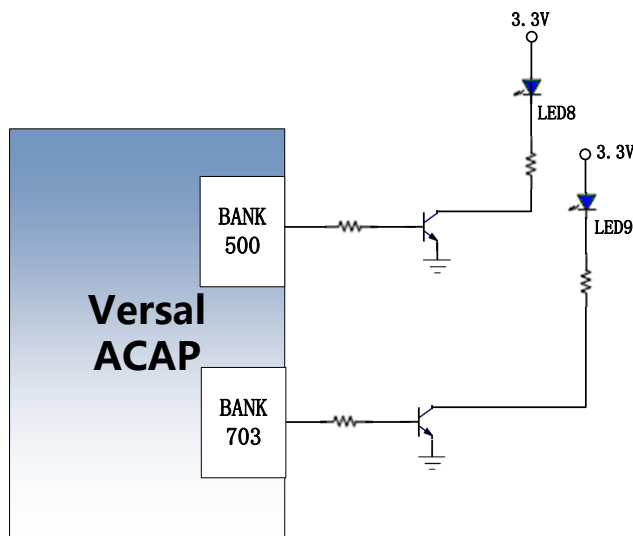


Figure 27: Schematic Diagram of LED Lamp Hardware Design

LED FPGA pin assignment

| Signal name | FPGA pin name | FPGA pin number | Remark |
|-------------|---------------|-----------------|------------------------|
| PS_LED1 | LPD_MIO25 | Y9 | User-defined indicator |
| PL_LED1 | B703_L19_P | E20 | User-defined indicator |

Table 26: LED FPGA pin assignment

Part 3.16: Power Supply

The power input voltage of the development board is DC12V. Please use the power supply of the development board. Do not use the power supply of other specifications to avoid damage to the development board. On the base board, a 3-channel DC/DC power supply chip ETA1471FT2G converts +5V, +3.3V and +1.8V, and then an LDO power supply chip SPX3819M5-1-5 converts +3.3V to +1.5 V. In addition, the +12 V power supply on the base board supplies power to the module through the inter-board connector. The power supply design on the base board is shown in Figure 28.

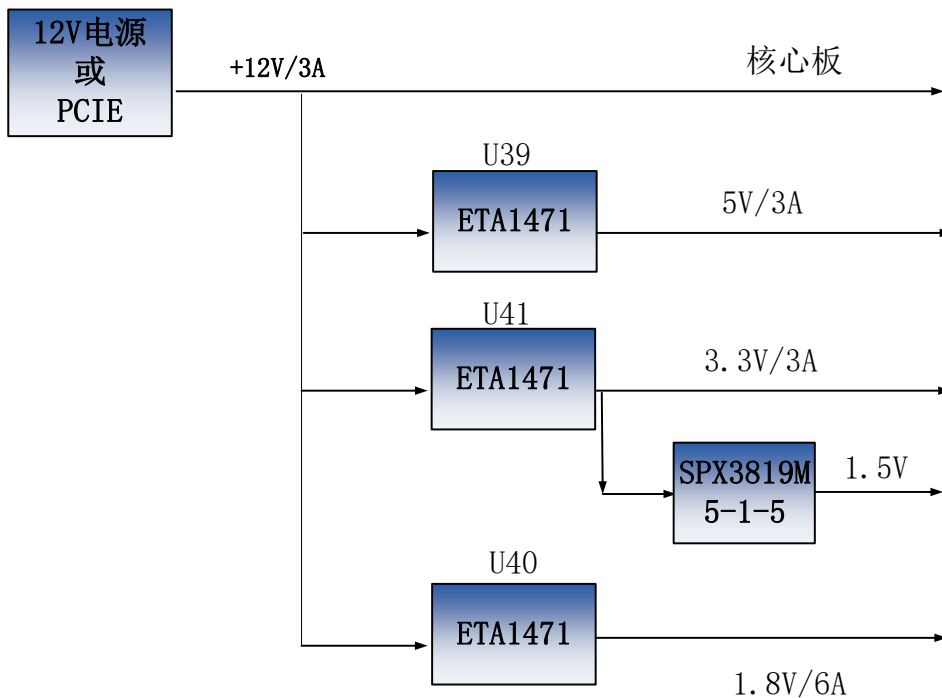


Figure 28: Power supply schematic diagram of expansion board

Part 3.17: Structural Dimension Drawing

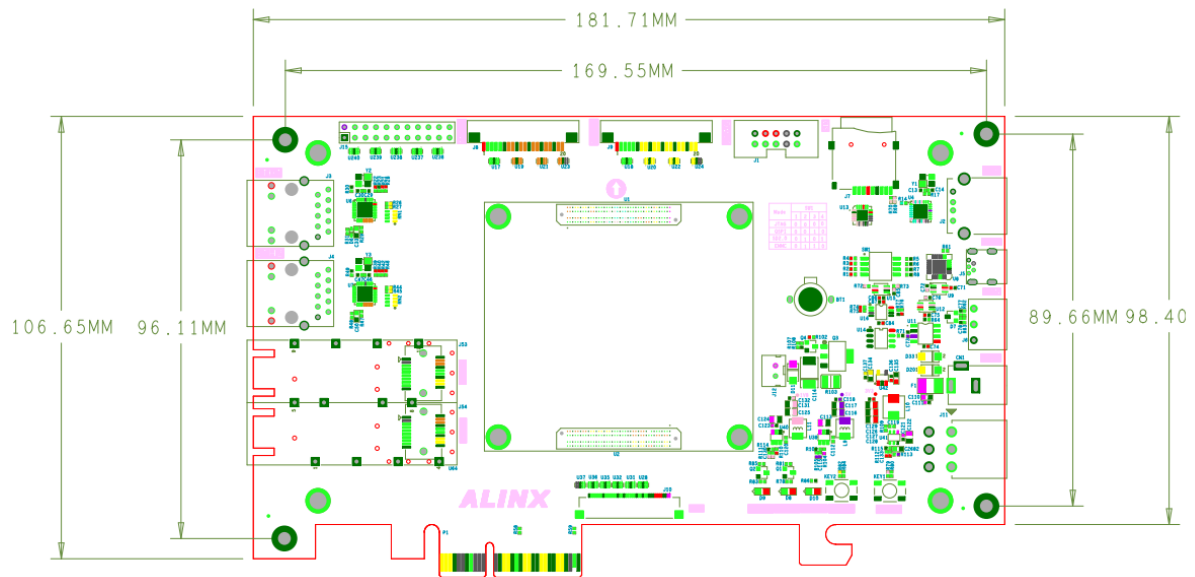


Figure 29: Front View (Top View)