Zynq UltraScale+ MPSoC Development Board

Z19

User Manual

ALINX

Table of Contents

Table of Contents 2

1. FPGA Development Board Introduction 6

2. ZYNQ Chip Introduction 9

3. DDR4 DRAM 11

4. QSPI Flash 23

5. eMMC Flash 25

6. Clock Configuration 26

7. Power Supply 28

8. M.2 Port 30

9. DP Display Port 31

10. USB3.0 Port 32

11. Gigabit Ethernet Port 33

12. Uart Port 36

13. SD Card Slot 37

14. Fiber Interface 38

15. CAN Communication Interface 45

16. 485 Communication Interface 45

17. MIPI Interface 46

18. FMC Connector 48

19. PCIE Interface 64

20. SATA Interface 66

21. SMA Interface 68

22. JTAG Debugging Interface 69

23. RTC Real-time Clock 69

24. EEPROM and Temperature Sensor 70

25. LED Light 71

26. Keys 71

27. Dip Switch Configuration 72

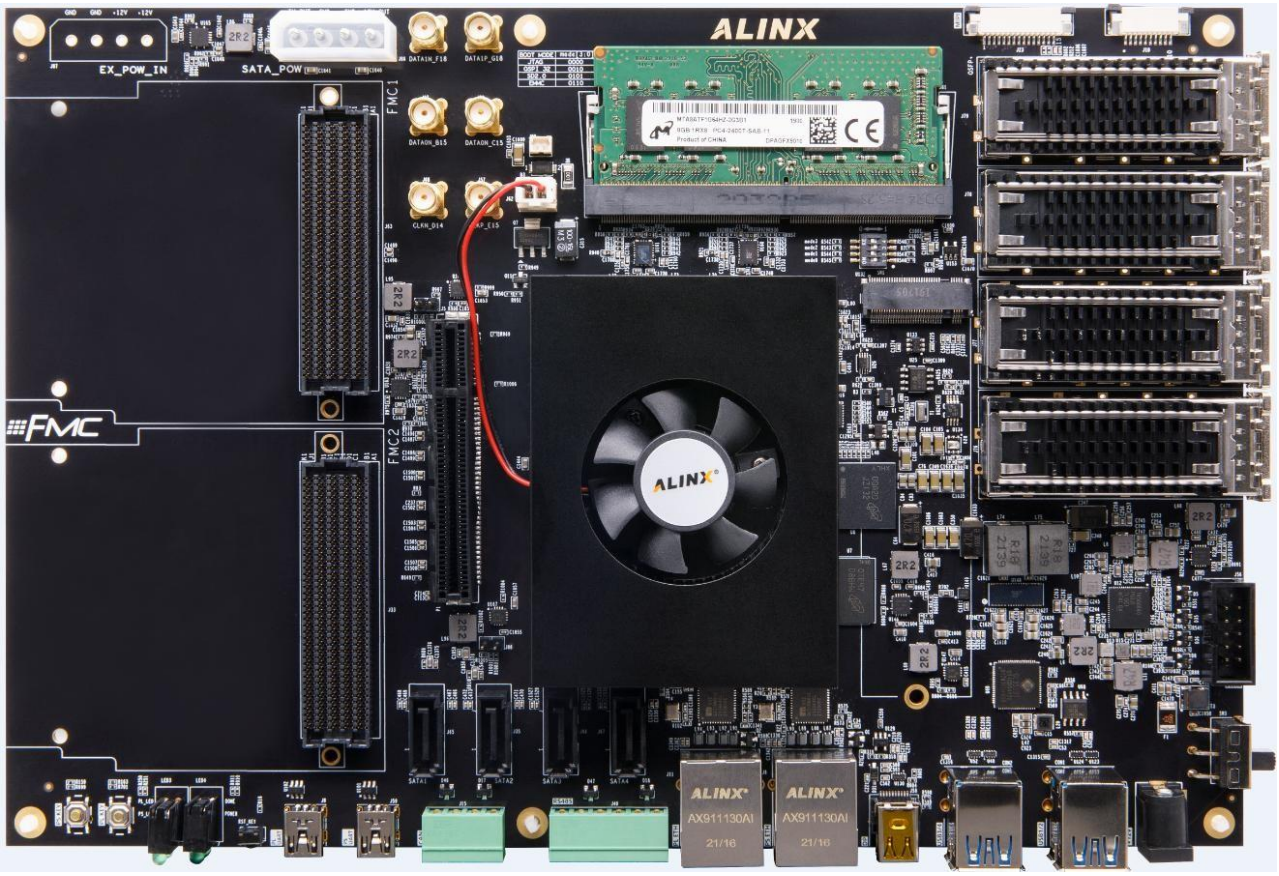
28. Fan 73

29. Structure and Dimension 74

Based on XILINX Zynq UltraScale+MPSoCs development platform, our company's development board 2021 (Model: Z19) has officially released, and we have prepared this user manual for your quick understanding of this development platform.

This MPSoCs FPGA development platform uses the solution of ZU19EG, a XILINX Zynq UltraScale+EG chip, and adopts Processing System (PS)+Programmable Logic(PL) technology to integrate quad-core ARM Cortex-A53 and FPGA programmable logic on a single chip. In addition, The PS side of the development board has 4 pieces of 2GB high-speed DDR4 SDRAM chips, one piece of 32GB eMMC memory chip, and 2 pieces of 512Mb QSPI FLASH chips; the PL side of the core board has a 260-pin DDR4 SODIMM slot (DDR4 SODIMM is sold separately).

In the design of development board, we provide users with a rich set of peripheral interfaces. For example, 2 FMC dual-width interfaces, 1 M.2 SSD interface, 1 PCIE main-mode slot, 4 SATA interfaces, 3 pairs of differential SMA interfaces, 1 mini_DP interface, 4 QSFP28 fiber interfaces, 4 USB3.0 interfaces, 2 Gigabit Ethernet interfaces, 3 UART interfaces, 1 TF card slot, 2 CAN bus interfaces, 2 RS485 interfaces and 1 MIPI camera interface and so on. It is a "professional grade" ZYNQ development platform because it meets the requirements of high-speed data exchange, data storage, video transmission and processing, deep learning, artificial intelligence and industrial control. Moreover, It provides the possibility of high-speed data transmission and exchange, pre-verification and post-application of data processing. We believe that such a product is ideal for students, engineers and other groups who are engaged in the development of MPSoCs.


ALINX
EX_POW_IN
SATA_POW
FMC1
FMC2
FMC
ALINX
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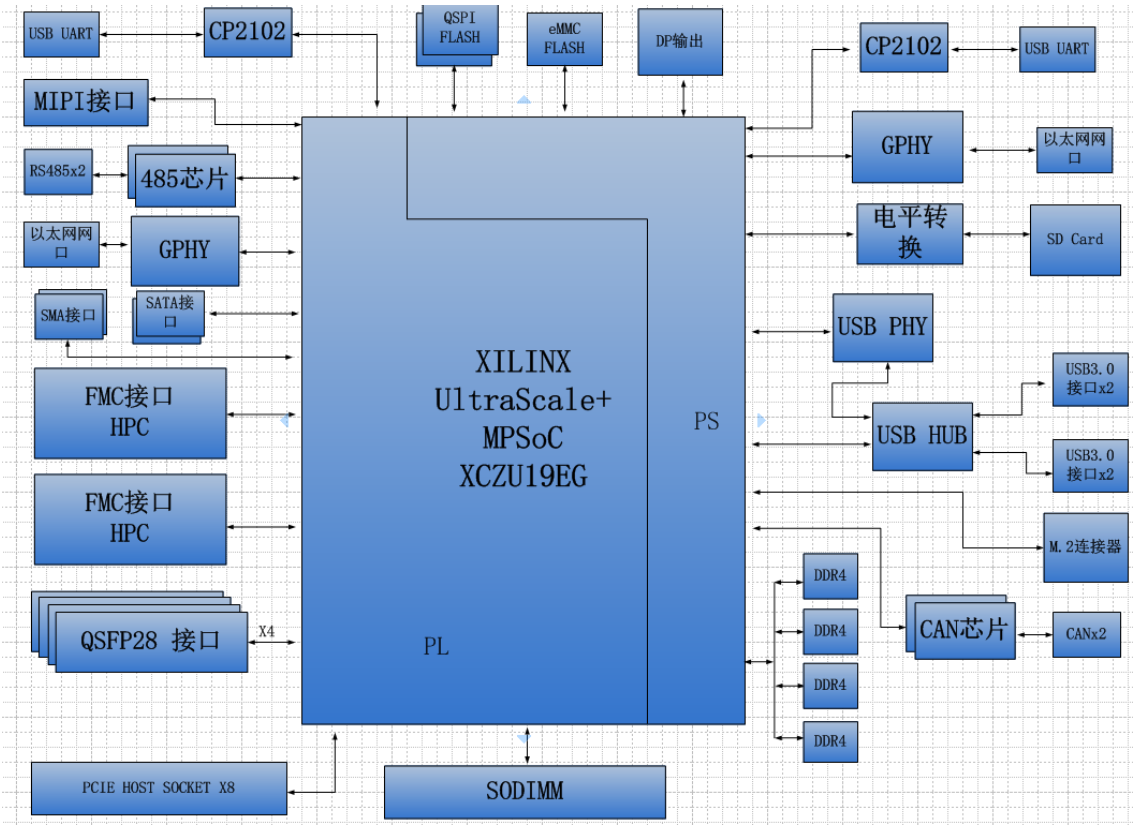
AX911130AI
21/16

1. FPGA Development Board Introduction

The Z19 MPSoCs is mainly composed of ZU19EG, 4 DDR4, DDR4 SODIMM, eMMC, and 2 QSPI FLASH. Its main chip adopts Xilinx's Zynq UltraScale+ MPSoCs series chip, model XCZU19EG--2FFVC1760I. The ZU19EG chip can be divided into a Processor System part (PS) and a Programmable Logic part (PL), and 4 pieces of DDR4 and one 260-pin DDR4 SODIMM slot are attached to the two sides respectively. The capacity of each DDR4 chip on the PS side is up to 2GB, which enables the ARM system and the FPGA system to process and store data independently. The 32GB eMMC FLASH memory chip and 2 pieces of 512Mb QSPI FLASH chips on the PS side are used to statically store the MPSoCs' operating system, file system and user data.

The Z19 MPSoCs is extended with a rich set of peripheral interfaces, including 2 FMC dual-width interfaces, 1 M.2 SSD interface, 1 PCIE main mode slot, 4 SATA interfaces, 3 pairs of differential SMA interfaces, 1 mini_DP interface, 4 QSFP28 fiber interfaces, 4 USB3.0 interfaces, 2 Gigabit Ethernet interfaces, 3 UART interfaces, 1 TF card slot, 2 CAN bus interfaces, 2 RS485 interfaces and 1 MIPI camera interface and some key LEDs.

The following is the structure diagram of the whole development system:



With this diagram, we can see the interfaces and functions that our development platform contains.

- Xilinx ARM+FPGA chip XCZU19EG -- 2FFVC1760I
- DDR4

  Four large-capacity 2GB (8GB in total) high-speed DDR4 SDRAM chips on the PS side.

  One 260-pin DDR4 SODIMM slot on the PI side.
- eMMC

A 32GB eMMC FLASH memory chip is mounted on the PS side for users to store operating system files or other user data.

- QSPI FLASH

Two 512Mbit QSPI FLASH memory chips, which can be used to store Uboot files, system files and user data of ZYNQ chip.

- PCIe x8 slot

One standard PCIEx8 main mode slot is used for PCIEx8 communication, which can be used to connect PCIE boards of PCIE x8, x4, x2, x1 to realize PCIE data communication. It supports PCI Express 2.0 standard, and the single channel of communication rate can be as high as 5GBaud.

- SMA interface

  Six SMA interfaces lead to a total of three pairs of differential signals.
- SATA interface

  Four SATA interfaces for connecting peripherals such as hard disks.
- DP output port

One standard Display Port output display port for displaying video image. The maximum output is 4K@30Hz or 1080P@60Hz.

- USB3.0 interface

Four USB3.0 HOST interfaces of TYPE A are used to connect external USB peripherals, such as mouse, keyboard, U disk and others.

- Gigabit Ethernet interface

Two 10/100M/1000M Ethernet RJ45 interfaces, one each for PS and PL, for Ethernet data exchange with computers or other network devices.

- Uart interface

Two Uart to USB interfaces, one each for PS and PL, for communication with PC for user-friendly debugging. The serial chip adopts the USB-UART chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface.

One ps uart is routed through a 1mm spaced 10pin FPC interface for connecting peripherals such as the serial screen.

- 4 QSFP28 fiber interface

Four independent transmission and reception channels, each capable of 25Gbps operation at 100 meters of the OM4 MMF, with an overall data rate of 100Gbps.

- MicroSD card holder

One MicroSD card used to store operating system images and file systems.

- FMC expansion port

Two standard FMC HPC expansion ports that comply with standard dual-width FMC standards. You can externally connect XILINX or our various FMC modules (HDMI input/output module, binocular camera module, high-speed AD module, etc.).

- CAN communication interface

Two CAN bus interfaces adopt SN65HVD232 chip of TI company and use 4-pin green terminals.

- 485 communication interface

Two 485 communication interfaces adopt MAX3485 chip of MAXIM company and use 6-pin green terminals.

- MIPI interface

Two LANE MIPI camera input interfaces for connecting to the MIPI camera module (AN5641).

- JTAG Debugging interface

One 10-pin 2.54mm standard JTAG interface for FPGA program download and debugging. Users can debug and download ZU9EG system through XILINX downloader.

- Temperature and humidity sensor

An on-board temperature and humidity sensor chip (LM75) is used to detect the ambient temperature and humidity of the board.

- EEPROM

One piece of EEPROM 24LC04 with IIC interface.

- RTC Real-Time Clock

One built-in RTC real-time clock.

- LED light

Two dual side-mounted LEDs, including 1 power indicator, 1 DONE configuration indicator, and 2 user indicators.

- Keys

3 buttons, 1 side-mounted reset button, 2 user buttons.

2. ZYNQ Chip Introduction

The development board uses chips (model: XCZU19EG-2FFVC1760I) from Xilinx's Zynq UltraScale+ MPSoCs EG series. The ZU19EG chip's PS system integrates four ARM Cortex™-A53 processors with a speed of up to 1.3Ghz with Level 2 Cache support; in addition, the ZU9EG also contains two Cortex-R5 processors with a speed of up to 533Mhz.

The ZU19EG chip supports 32-bit or 64-bit DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 memory chips, and has rich high-speed interfaces on the PS side, such as PCIE Gen2, USB3.0, SATA 3.1, and DisplayPort. It also supports USB2.0, Gigabit Ethernet, SD/SDIO, I2C, CAN, UART, GPIO and other interfaces. The PL side contains a wealth of programmable logic unit, DSP and internal RAM. Figure 2-2-1 detailed the Overall Block Diagram of the ZU19EG chip:

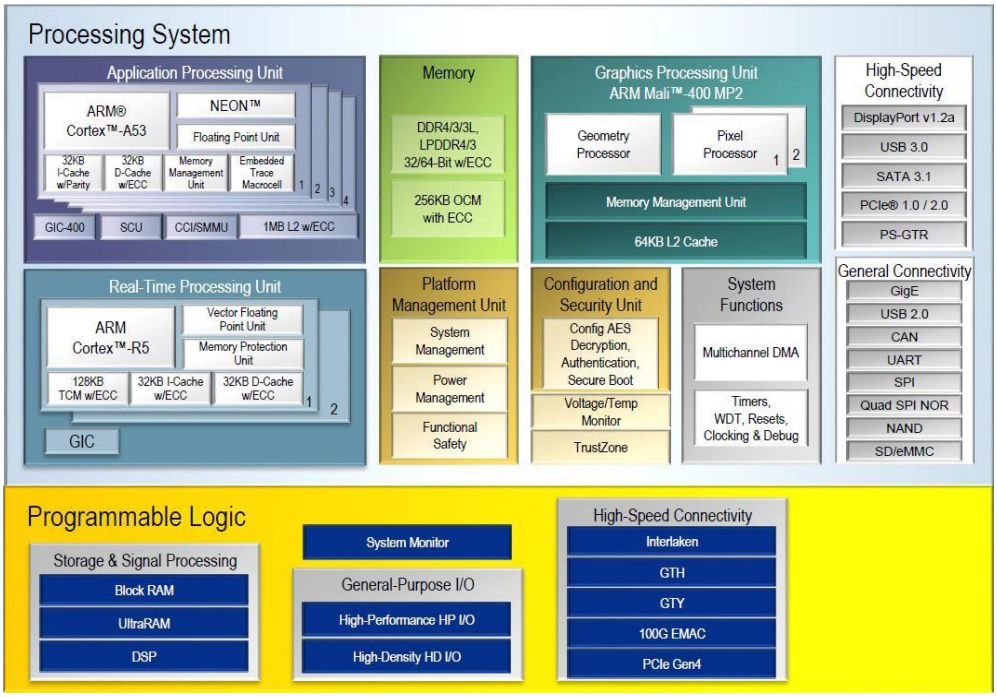


Figure 2-2-1 Overall block diagram of ZYNQ ZU19EG chip

The main parameters of the PS system are as follows:

- ARM quad-core Cortex™-A53 processor with a speed of up to 1.3GHz, each CPU 32KB level 1 instruction and data cache, 1MB level 2 cache, shared by 2 CPUs.
- ARM dual-core Cortex-R5 processor with a speed of up to 533MHz, each CPU 32KB level 1 instruction and data cache, and 128K tightly coupled memory.
- External memory interface: supports 32/64bit DDR4/3/3L, LPDDR4/3 interface.
- Static memory interface: supports NAND, 2xQuad-SPI FLASH.
- High-speed connection interface, supports PCIe Gen2 x 4, 2 x USB3.0, Sata 3.1, Display Port, 4 x Tri-mode, Gigabit Ethernet.

- Common connection interfaces: 2 x USB2.0, 2 x SD/SDIO, 2 x UART, 2 x CAN 2.0B, 2 x I2C, 2 x SPI, 4 x 32b GPIO.
- Power management: supports the four-part division of power supply Full/Low/PL/Battery.
- Encryption algorithm: RSA, AES, and SHA.
- System monitoring: 10-bit 1Mbps AD sampling for temperature and voltage detection.

The main parameters of the PL logic part are as follows:

- System Logic Cells: 1143K;
- CLB flip-flops: 1045K;
- CLBLUTs: 523K;
- Block RAM: 34.6Mb;
- Clock Management Units (CMTs): 11;
- DSP Slices: 1968;
- GTH 16.3Gb/s transceivers: 44.

The XCZU19EG-2FFVC1760I chip has a speed rating of -2, industrial grade, and is packaged as FFVC1760.

3. DDR4 DRAM

The Z19 development board is equipped with four Micron 2GB DDR4 chips (model MT40A1G16KD-062E), which are all mounted on the PS side, comprising a 64-bit data bus bandwidth and 8GB capacity, while a 260-pin DDR4 SODIMM slot is led on the PL side. The DDR4 SDRAM on the PS side can run at a maximum speed of 1200MHz (2400Mbps data rate) and 4 DDR4 memory systems are directly connected to the memory interface of BANK504 on the PS side. The DDR4 SODIMM slot on the PL side is connected to the interface of BANK69, 70, 71 on the FPGA. The specific configuration of DDR4 SDRAM is shown in Table 2-3-1 below.

Bit Number	Chip Model	Capacity	Manufacturer
U4,U5,U6,U7	MT40A1G16KD-062E	1G x 16bit	Micron

Table 2-3-1: DDR4 SDRAM Configuration

The hardware design of DDR4 requires strict consideration of signal integrity, so we have fully considered the matching resistance/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR4.

The hardware connection of DDR4 SDRAM on the PS Side is shown in Figure 3-1:

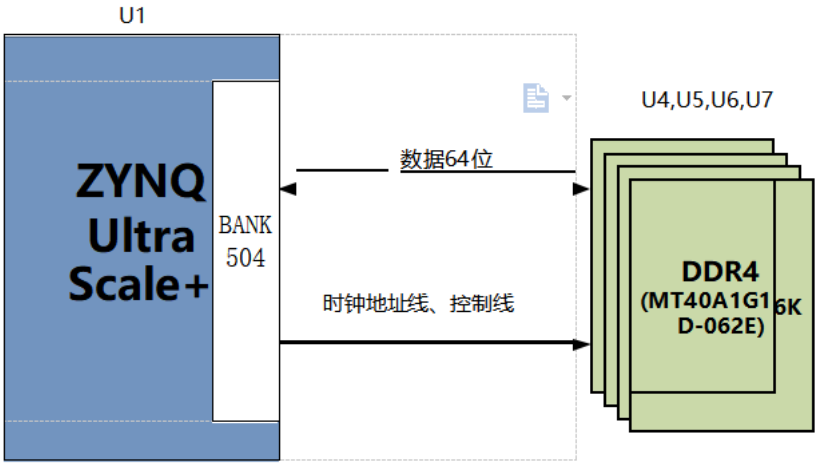


Figure 3-1: DDR4 DRAM schematic diagram

The hardware connection of DDR4 SDRAM on the Pl Side is shown in Figure 3-2:

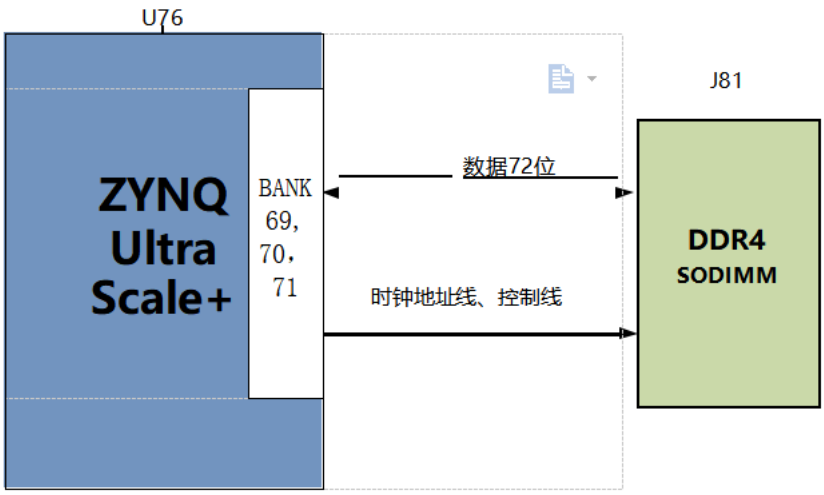


Figure 3-2: DDR4 DRAM schematic diagram

PS Side DDR4 DRAM pin assignment:

Signal Name	Pin Name	Pin Number
PS_DDR4_DQS0_N	PS_DDR_DQS_N0_504	BA30
PS_DDR4_DQS0_P	PS_DDR_DQS_P0_504	AY30
PS_DDR4_DQS1_N	PS_DDR_DQS_N1_504	AY33
PS_DDR4_DQS1_P	PS_DDR_DQS_P1_504	AY32
PS_DDR4_DQS2_N	PS_DDR_DQS_N2_504	AT30
PS_DDR4_DQS2_P	PS_DDR_DQS_P2_504	AR30
PS_DDR4_DQS3_N	PS_DDR_DQS_N3_504	AT32
PS_DDR4_DQS3_P	PS_DDR_DQS_P3_504	AR32
PS_DDR4_DQS4_N	PS_DDR_DQS_N4_504	AR40
PS_DDR4_DQS4_P	PS_DDR_DQS_P4_504	AP40
PS_DDR4_DQS5_N	PS_DDR_DQS_N5_504	AK37
PS_DDR4_DQS5_P	PS_DDR_DQS_P5_504	AJ37
PS_DDR4_DQS6_N	PS_DDR_DQS_N6_504	AU41
PS_DDR4_DQS6_P	PS_DDR_DQS_P6_504	AU40
PS_DDR4_DQS7_N	PS_DDR_DQS_N7_504	AL41
PS_DDR4_DQS7_P	PS_DDR_DQS_P7_504	AL40
PS_DDR4_DQ0	PS_DDR_DQ0_504	AV29
PS_DDR4_DQ1	PS_DDR_DQ1_504	AW30
PS_DDR4_DQ2	PS_DDR_DQ2_504	AW29
PS_DDR4_DQ3	PS_DDR_DQ3_504	AW31
PS_DDR4_DQ4	PS_DDR_DQ4_504	BB31
PS_DDR4_DQ5	PS_DDR_DQ5_504	BB30
PS_DDR4_DQ6	PS_DDR_DQ6_504	BB29

PS_DDR4_DQ7	PS_DDR_DQ7_504	BA31
PS_DDR4_DQ8	PS_DDR_DQ8_504	BB33
PS_DDR4_DQ9	PS_DDR_DQ9_504	BA32
PS_DDR4_DQ10	PS_DDR_DQ10_504	BA33
PS_DDR4_DQ11	PS_DDR_DQ11_504	BB34
PS_DDR4_DQ12	PS_DDR_DQ12_504	AV31
PS_DDR4_DQ13	PS_DDR_DQ13_504	AW32
PS_DDR4_DQ14	PS_DDR_DQ14_504	AV32
PS_DDR4_DQ15	PS_DDR_DQ15_504	AV33
PS_DDR4_DQ16	PS_DDR_DQ16_504	AN29
PS_DDR4_DQ17	PS_DDR_DQ17_504	AP29
PS_DDR4_DQ18	PS_DDR_DQ18_504	AP30
PS_DDR4_DQ19	PS_DDR_DQ19_504	AP31
PS_DDR4_DQ20	PS_DDR_DQ20_504	AT31
PS_DDR4_DQ21	PS_DDR_DQ21_504	AU30
PS_DDR4_DQ22	PS_DDR_DQ22_504	AU31
PS_DDR4_DQ23	PS_DDR_DQ23_504	AU29
PS_DDR4_DQ24	PS_DDR_DQ24_504	AV34
PS_DDR4_DQ25	PS_DDR_DQ25_504	AU33
PS_DDR4_DQ26	PS_DDR_DQ26_504	AT33
PS_DDR4_DQ27	PS_DDR_DQ27_504	AU34
PS_DDR4_DQ28	PS_DDR_DQ28_504	AN33
PS_DDR4_DQ29	PS_DDR_DQ29_504	AP32
PS_DDR4_DQ30	PS_DDR_DQ30_504	AN32
PS_DDR4_DQ31	PS_DDR_DQ31_504	AN31

PS_DDR4_DQ32	PS_DDR_DQ32_504	AN41
PS_DDR4_DQ33	PS_DDR_DQ33_504	AN42
PS_DDR4_DQ34	PS_DDR_DQ34_504	AP42
PS_DDR4_DQ35	PS_DDR_DQ35_504	AP41
PS_DDR4_DQ36	PS_DDR_DQ36_504	AN39
PS_DDR4_DQ37	PS_DDR_DQ37_504	AR38
PS_DDR4_DQ38	PS_DDR_DQ38_504	AP39
PS_DDR4_DQ39	PS_DDR_DQ39_504	AN38
PS_DDR4_DQ40	PS_DDR_DQ40_504	AL37
PS_DDR4_DQ41	PS_DDR_DQ41_504	AL38
PS_DDR4_DQ42	PS_DDR_DQ42_504	AK38
PS_DDR4_DQ43	PS_DDR_DQ43_504	AK39
PS_DDR4_DQ44	PS_DDR_DQ44_504	AJ36
PS_DDR4_DQ45	PS_DDR_DQ45_504	AL35
PS_DDR4_DQ46	PS_DDR_DQ46_504	AJ35
PS_DDR4_DQ47	PS_DDR_DQ47_504	AK35
PS_DDR4_DQ48	PS_DDR_DQ48_504	AR42
PS_DDR4_DQ49	PS_DDR_DQ49_504	AT41
PS_DDR4_DQ50	PS_DDR_DQ50_504	AT42
PS_DDR4_DQ51	PS_DDR_DQ51_504	AT40
PS_DDR4_DQ52	PS_DDR_DQ52_504	AV42
PS_DDR4_DQ53	PS_DDR_DQ53_504	AV41
PS_DDR4_DQ54	PS_DDR_DQ54_504	AV39
PS_DDR4_DQ55	PS_DDR_DQ55_504	AV38
PS_DDR4_DQ56	PS_DDR_DQ56_504	AM39

PS_DDR4_DQ57	PS_DDR_DQ57_504	AM38
PS_DDR4_DQ58	PS_DDR_DQ58_504	AM40
PS_DDR4_DQ59	PS_DDR_DQ59_504	AM41
PS_DDR4_DQ60	PS_DDR_DQ60_504	AJ42
PS_DDR4_DQ61	PS_DDR_DQ61_504	AK42
PS_DDR4_DQ62	PS_DDR_DQ62_504	AK40
PS_DDR4_DQ63	PS_DDR_DQ63_504	AK41
PS_DDR4_DM0	PS_DDR_DM0_504	AY29
PS_DDR4_DM1	PS_DDR_DM1_504	AY34
PS_DDR4_DM2	PS_DDR_DM2_504	AR29
PS_DDR4_DM3	PS_DDR_DM3_504	AR33
PS_DDR4_DM4	PS_DDR_DM4_504	AR39
PS_DDR4_DM5	PS_DDR_DM5_504	AL36
PS_DDR4_DM6	PS_DDR_DM6_504	AU39
PS_DDR4_DM7	PS_DDR_DM7_504	AL42
PS_DDR4_A0	PS_DDR_A0_504	BA38
PS_DDR4_A1	PS_DDR_A1_504	BB36
PS_DDR4_A2	PS_DDR_A2_504	BA35
PS_DDR4_A3	PS_DDR_A3_504	BB35
PS_DDR4_A4	PS_DDR_A4_504	BB38
PS_DDR4_A5	PS_DDR_A5_504	AY35
PS_DDR4_A6	PS_DDR_A6_504	AP37
PS_DDR4_A7	PS_DDR_A7_504	AT36
PS_DDR4_A8	PS_DDR_A8_504	AR35
PS_DDR4_A9	PS_DDR_A9_504	AT35

PS_DDR4_A10	PS_DDR_A10_504	AU35
PS_DDR4_A11	PS_DDR_A11_504	AU36
PS_DDR4_A12	PS_DDR_A12_504	AW36
PS_DDR4_A13	PS_DDR_A13_504	AW37
PS_DDR4_ACT_B	PS_DDR_ACT_N_504	AR37
PS_DDR4_ALERT_B	PS_DDR_ALERT_N_504	AM36
PS_DDR4_BA0	PS_DDR_BA0_504	AN37
PS_DDR4_BA1	PS_DDR_BA1_504	AN36
PS_DDR4_BG0	PS_DDR_BG0_504	AP36
PS_DDR4_CAS_B	PS_DDR_A15_504	AW34
PS_DDR4_CKE0	PS_DDR_CKE0_504	AY38
PS_DDR4_CLK0_N	PS_DDR_CK_N0_504	BA37
PS_DDR4_CLK0_P	PS_DDR_CK0_504	BA36
PS_DDR4_CS0_B	PS_DDR_CS_N0_504	AY37
PS_DDR4_ODT0	PS_DDR_ODT0_504	BB39
PS_DDR4_PARITY	PS_DDR_PARITY_504	AM35
PS_DDR4_RAS_B	PS_DDR_A16_504	AR34
PS_DDR4_RESET_B	PS_DDR_RAM_RST_N_504	AM34
PS_DDR4_WE_B	PS_DDR_A14_504	AW35

PL Side DDR4 DRAM pin assignment:

Signal Name	Pin Name	Pin Number
PL_DDR4_DQS0_N	IO_L4N_T0U_N7_DBC_AD7N_71	N19
PL_DDR4_DQS0_P	IO_L4P_T0U_N6_DBC_AD7P_71	N20
PL_DDR4_DQS1_N	IO_L10N_T1U_N7_QBC_AD4N_71	J22

PL_DDR4_DQS1_P	IO_L10P_T1U_N6_QBC_AD4P_71	K22
PL_DDR4_DQS2_N	IO_L16N_T2U_N7_QBC_AD3N_71	E20
PL_DDR4_DQS2_P	IO_L16P_T2U_N6_QBC_AD3P_71	F20
PL_DDR4_DQS3_N	IO_L22N_T3U_N7_DBC_AD0N_71	B21
PL_DDR4_DQS3_P	IO_L22P_T3U_N6_DBC_AD0P_71	C21
PL_DDR4_DQS4_N	IO_L4N_T0U_N7_DBC_AD7N_69	F30
PL_DDR4_DQS4_P	IO_L4P_T0U_N6_DBC_AD7P_69	G30
PL_DDR4_DQS5_N	IO_L10N_T1U_N7_QBC_AD4N_69	A32
PL_DDR4_DQS5_P	IO_L10P_T1U_N6_QBC_AD4P_69	B31
PL_DDR4_DQS6_N	IO_L16N_T2U_N7_QBC_AD3N_69	C34
PL_DDR4_DQS6_P	IO_L16P_T2U_N6_QBC_AD3P_69	D34
PL_DDR4_DQS7_N	IO_L22N_T3U_N7_DBC_AD0N_69	A40
PL_DDR4_DQS7_P	IO_L22P_T3U_N6_DBC_AD0P_69	A39
PL_DDR4_DQ0	IO_L3P_T0L_N4_AD15P_71	M20
PL_DDR4_DQ1	IO_L3N_T0L_N5_AD15N_71	L19
PL_DDR4_DQ2	IO_L6P_T0U_N10_AD6P_71	M22
PL_DDR4_DQ3	IO_L5P_T0U_N8_AD14P_71	P21
PL_DDR4_DQ4	IO_L2N_T0L_N3_71	L18
PL_DDR4_DQ5	IO_L2P_T0L_N2_71	M18
PL_DDR4_DQ6	IO_L5N_T0U_N9_AD14N_71	N21
PL_DDR4_DQ7	IO_L6N_T0U_N11_AD6N_71	M21
PL_DDR4_DQ8	IO_L12P_T1U_N10_GC_71	H21
PL_DDR4_DQ9	IO_L11P_T1U_N8_GC_71	H20
PL_DDR4_DQ10	IO_L8N_T1L_N3_AD5N_71	K20
PL_DDR4_DQ11	IO_L8P_T1L_N2_AD5P_71	L20

PL_DDR4_DQ12	IO_L11N_T1U_N9_GC_71	H19
PL_DDR4_DQ13	IO_L12N_T1U_N11_GC_71	G20
PL_DDR4_DQ14	IO_L9P_T1L_N4_AD12P_71	K21
PL_DDR4_DQ15	IO_L9N_T1L_N5_AD12N_71	J21
PL_DDR4_DQ16	IO_L17N_T2U_N9_AD10N_71	D21
PL_DDR4_DQ17	IO_L17P_T2U_N8_AD10P_71	E21
PL_DDR4_DQ18	IO_L14P_T2L_N2_GC_71	F23
PL_DDR4_DQ19	IO_L18N_T2U_N11_AD2N_71	D22
PL_DDR4_DQ20	IO_L15N_T2L_N5_AD11N_71	E19
PL_DDR4_DQ21	IO_L15P_T2L_N4_AD11P_71	F19
PL_DDR4_DQ22	IO_L18P_T2U_N10_AD2P_71	E22
PL_DDR4_DQ23	IO_L14N_T2L_N3_GC_71	F22
PL_DDR4_DQ24	IO_L20N_T3L_N3_AD1N_71	B20
PL_DDR4_DQ25	IO_L21P_T3L_N4_AD8P_71	A20
PL_DDR4_DQ26	IO_L24P_T3U_N10_71	B23
PL_DDR4_DQ27	IO_L24N_T3U_N11_71	A23
PL_DDR4_DQ28	IO_L20P_T3L_N2_AD1P_71	C20
PL_DDR4_DQ29	IO_L21N_T3L_N5_AD8N_71	A19
PL_DDR4_DQ30	IO_L23P_T3U_N8_71	B22
PL_DDR4_DQ31	IO_L23N_T3U_N9_71	A22
PL_DDR4_DQ32	IO_L5P_T0U_N8_AD14P_69	G28
PL_DDR4_DQ33	IO_L5N_T0U_N9_AD14N_69	F29
PL_DDR4_DQ34	IO_L2N_T0L_N3_69	H30
PL_DDR4_DQ35	IO_L2P_T0L_N2_69	J30
PL_DDR4_DQ36	IO_L6P_T0U_N10_AD6P_69	J28

PL_DDR4_DQ37	IO_L6N_T0U_N11_AD6N_69	H28
PL_DDR4_DQ38	IO_L3P_T0L_N4_AD15P_69	F31
PL_DDR4_DQ39	IO_L3N_T0L_N5_AD15N_69	F32
PL_DDR4_DQ40	IO_L9N_T1L_N5_AD12N_69	A30
PL_DDR4_DQ41	IO_L8N_T1L_N3_AD5N_69	B30
PL_DDR4_DQ42	IO_L11N_T1U_N9_GC_69	D31
PL_DDR4_DQ43	IO_L11P_T1U_N8_GC_69	E31
PL_DDR4_DQ44	IO_L9P_T1L_N4_AD12P_69	A29
PL_DDR4_DQ45	IO_L8P_T1L_N2_AD5P_69	C29
PL_DDR4_DQ46	IO_L12P_T1U_N10_GC_69	C30
PL_DDR4_DQ47	IO_L12N_T1U_N11_GC_69	C31
PL_DDR4_DQ48	IO_L15N_T2L_N5_AD11N_69	C33
PL_DDR4_DQ49	IO_L18N_T2U_N11_AD2N_69	A34
PL_DDR4_DQ50	IO_L14N_T2L_N3_GC_69	B33
PL_DDR4_DQ51	IO_L15P_T2L_N4_AD11P_69	D33
PL_DDR4_DQ52	IO_L18P_T2U_N10_AD2P_69	A33
PL_DDR4_DQ53	IO_L14P_T2L_N2_GC_69	B32
PL_DDR4_DQ54	IO_L17P_T2U_N8_AD10P_69	B35
PL_DDR4_DQ55	IO_L17N_T2U_N9_AD10N_69	A35
PL_DDR4_DQ56	IO_L21N_T3L_N5_AD8N_69	A38
PL_DDR4_DQ57	IO_L20N_T3L_N3_AD1N_69	B37
PL_DDR4_DQ58	IO_L24P_T3U_N10_69	C42
PL_DDR4_DQ59	IO_L23P_T3U_N8_69	B40
PL_DDR4_DQ60	IO_L20P_T3L_N2_AD1P_69	B36
PL_DDR4_DQ61	IO_L21P_T3L_N4_AD8P_69	A37

PL_DDR4_DQ62	IO_L24N_T3U_N11_69	B42
PL_DDR4_DQ63	IO_L23N_T3U_N9_69	B41
PL_DDR4_DQ64	IO_L24P_T3U_N10_70	A24
PL_DDR4_DQ65	IO_L21P_T3L_N4_AD8P_70	C26
PL_DDR4_DQ66	IO_L23N_T3U_N9_70	C25
PL_DDR4_DQ67	IO_L20P_T3L_N2_AD1P_70	A27
PL_DDR4_DQ68	IO_L23P_T3U_N8_70	C24
PL_DDR4_DQ69	IO_L24N_T3U_N11_70	A25
PL_DDR4_DQ70	IO_L21N_T3L_N5_AD8N_70	B27
PL_DDR4_DQ71	IO_L20N_T3L_N3_AD1N_70	A28
PL_DDR4_DM0	IO_L1P_T0L_N0_DBC_71	P18
PL_DDR4_DM1	IO_L7P_T1L_N0_QBC_AD13P_71	K19
PL_DDR4_DM2	IO_L13P_T2L_N0_GC_QBC_71	G22
PL_DDR4_DM3	IO_L19P_T3L_N0_DBC_AD9P_71	D19
PL_DDR4_DM4	IO_L1P_T0L_N0_DBC_69	K29
PL_DDR4_DM5	IO_L7P_T1L_N0_QBC_AD13P_69	E29
PL_DDR4_DM6	IO_L13P_T2L_N0_GC_QBC_69	E32
PL_DDR4_DM7	IO_L19P_T3L_N0_DBC_AD9P_69	C36
PL_DDR4_DM8	IO_L19P_T3L_N0_DBC_AD9P_70	C28
PL_DDR4_A0	IO_L1P_T0L_N0_DBC_70	P26
PL_DDR4_A1	IO_L6P_T0U_N10_AD6P_70	M23
PL_DDR4_A2	IO_L6N_T0U_N11_AD6N_70	L23
PL_DDR4_A3	IO_L11P_T1U_N8_GC_70	H25
PL_DDR4_A4	IO_L11N_T1U_N9_GC_70	H26
PL_DDR4_A5	IO_T3U_N12_70	D24

PL_DDR4_A6	IO_L4N_T0U_N7_DBC_AD7N_70	K24
PL_DDR4_A7	IO_L18N_T2U_N11_AD2N_70	E24
PL_DDR4_A8	IO_L9N_T1L_N5_AD12N_70	J24
PL_DDR4_A9	IO_L10N_T1U_N7_QBC_AD4N_70	G23
PL_DDR4_A10	IO_L16N_T2U_N7_QBC_AD3N_70	E27
PL_DDR4_A11	IO_L16P_T2U_N6_QBC_AD3P_70	E26
PL_DDR4_A12	IO_L15N_T2L_N5_AD11N_70	F28
PL_DDR4_A13	IO_L7P_T1L_N0_QBC_AD13P_70	K27
PL_DDR4_ACT_B	IO_L9P_T1L_N4_AD12P_70	J23
PL_DDR4_ALERT_B	IO_L10P_T1U_N6_QBC_AD4P_70	H23
PL_DDR4_BA0	IO_L4P_T0U_N6_DBC_AD7P_70	L24
PL_DDR4_BA1	IO_T1U_N12_70	K25
PL_DDR4_BG0	IO_L17N_T2U_N9_AD10N_70	D28
PL_DDR4_BG1	IO_L17P_T2U_N8_AD10P_70	D27
PL_DDR4_CAS_B	IO_L7N_T1L_N1_QBC_AD13N_70	J27
PL_DDR4_CKE0	IO_L18P_T2U_N10_AD2P_70	F24
PL_DDR4_CKE1	IO_T2U_N12_70	D26
PL_DDR4_CLK0_N	IO_L13N_T2L_N1_GC_QBC_70	G27
PL_DDR4_CLK0_P	IO_L13P_T2L_N0_GC_QBC_70	G26
PL_DDR4_CLK1_N	IO_L14N_T2L_N3_GC_70	E25
PL_DDR4_CLK1_P	IO_L14P_T2L_N2_GC_70	F25
PL_DDR4_CS0_B	IO_L2P_T0L_N2_70	M25
PL_DDR4_CS1_B	IO_L3N_T0L_N5_AD15N_70	N25
PL_DDR4_ODT0	IO_L5P_T0U_N8_AD14P_70	P23
PL_DDR4_ODT1	IO_L2N_T0L_N3_70	L25

PL_DDR4_PARITY	IO_L3P_T0L_N4_AD15P_70	N24
PL_DDR4_RAS_B	IO_L8N_T1L_N3_AD5N_70	J26
PL_DDR4_RST	IO_L15P_T2L_N4_AD11P_70	F27
PL_DDR4_SCL	IO_L9P_AD3P_93	E6
PL_DDR4_SDA	IO_L9N_AD3N_93	D6
PL_DDR4_WE_B	IO_L5N_T0U_N9_AD14N_70	N23

4. QSPI Flash

The FPGA core board ACU9EG is equipped with two 256MBit Quad-SPI FLASH chip to form an 8-bit bandwidth data bus, the flash model is MT25QU512ABB1EW9-0SIT, which uses the 1.8V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 4-1.

Table 4-1: QSPI FLASH Specification

Bit Number	Model	Capacity	Manufacturer
U2, U3	MT25QU512ABB1EW9-0SIT	512M bit	Micron

QSPI FLASH is connected to the GPIO interface of the BANK500 in the PS side of the ZYNQ chip. In the system design, the GPIO interface functions of these PS interfaces need to be configured as the QSPI FLASH interface. Figure 4-1 shows the QSPI Flash in the schematic.

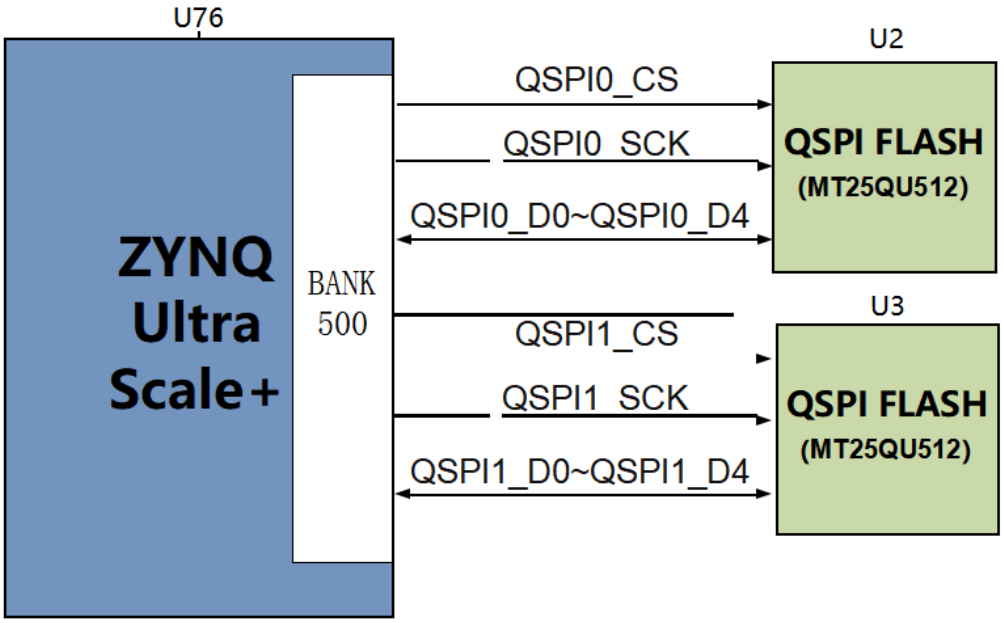


Figure 2-4-1: QSPI Flash in the schematic

Configure chip pin assignments:

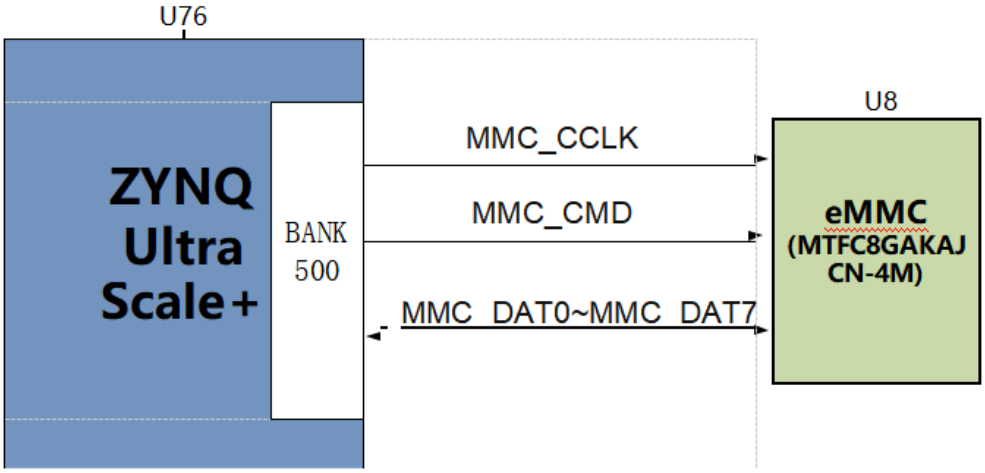
Signal Name	Pin Name	Pin Number
MIO5_QSPI0_SS_B	PS_MIO5_500	AL32
MIO0_QSPI0_SCLK	PS_MIO0_500	AM33
MIO4_QSPI0_IO0	PS_MIO4_500	AL33
MIO1_QSPI0_IO1	PS_MIO1_500	AM29
MIO2_QSPI0_IO2	PS_MIO2_500	AM31
MIO3_QSPI0_IO3	PS_MIO3_500	AM30
MIO7_QSPI1_SS_B	PS_MIO7_500	AL30
MIO12_QSPI1_SCLK	PS_MIO12_500	AJ34
MIO8_QSPI1_IO0	PS_MIO8_500	AK33
MIO9_QSPI1_IO1	PS_MIO9_500	AK34
MIO10_QSPI1_IO2	PS_MIO10_500	AK30
MIO11_QSPI1_IO3	PS_MIO11_500	AK32

5. eMMC Flash

Z19 is equipped with a large-capacity 8GB eMMC FLASH chip (MTFC32GAPALBH-IT), which supports the HS-MMC port of the JEDEC e-MMC V5.0 standard, and the level supports 1.8V or 3.3V. The data width of eMMC FLASH and ZYNQ connection is 8bit. Due to the large-capacity and non-volatile characteristics of eMMC FLASH, it can be used as a large-capacity storage device in the ZYNQ system, such as storing ARM applications, system files and other user data files The specific models and related parameters of eMMC FLASH are shown in Table 5-1.

Bit Number	Model	Capacity	Manufacturer
U19	MTFC32GAPALBH-IT	32G Byte	Micron

The eMMC FLASH is connected to the GPIO port of the BANK500 of the PS side of the ZYNQ UltraScale+. In the system design, it is necessary to configure the GPIO port function of the PS side as an EMMC port. Figure 5-1 shows the part of eMMC Flash in the schematic diagram.



Configuration Chip pin assignment:

Signal Name	Pin Name	Pin Number
MMC_CCLK	PS_MIO22_500	AH32
MMC_CMD	PS_MIO21_500	AF35

MMC_DAT0	PS_MIO13_500	AD34
MMC_DAT1	PS_MIO14_500	AJ32
MMC_DAT2	PS_MIO15_500	AD35
MMC_DAT3	PS_MIO16_500	AJ31
MMC_DAT4	PS_MIO17_500	AJ30
MMC_DAT5	PS_MIO18_500	AE34
MMC_DAT6	PS_MIO19_500	AE35
MMC_DAT7	PS_MIO20_500	AH34
MMC_RSTN	PS_MIO23_500	AG35

6. Clock Configuration

Z19 provides reference clock and RTC real-time clock for PS system and PL logic respectively, so that PS system and PL logic can work independently. The schematic diagram of the clock circuit design is shown in Figure 6-1:

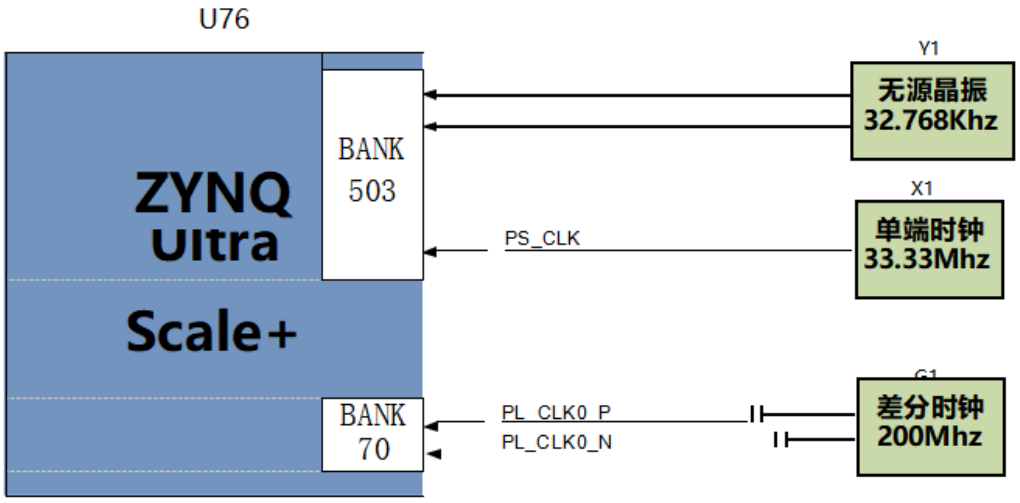


Figure 6-1: Core Board Clock Source

There are also two programmable clock chips on the board, Si5332BD11025-GM2, which provide differential clock sources for the high-speed transceiver GTX.

PS System RTC Real-Time Clock

The passive crystal Y1 on the core board provides a 32.768KHz real-time clock source for the PS system. The crystal is connected to the pins of PS_PADI_503 and PS_PADO_503 of the BANK503 of the ZYNQ chip. Figure 6-2 shows the schematic diagram.

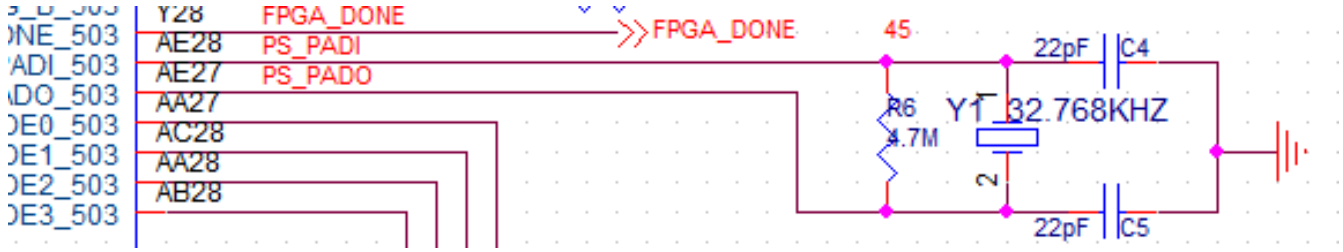


Figure 6-2: The passive crystal of RTC

Clock pin assignment:

Signal Name	Pin
PS_PADI_503	**AE28**
PS_PADO_503	**AE27**

PS system clock source:

The X1 crystal oscillator on the core board provides 33.333MHz clock input for the PS system. The input of the clock is connected to the pin of the PS_REF_CLK_503 of the BANK503 of the ZYNQ chip. Figure 6-3 shows the schematic diagram.

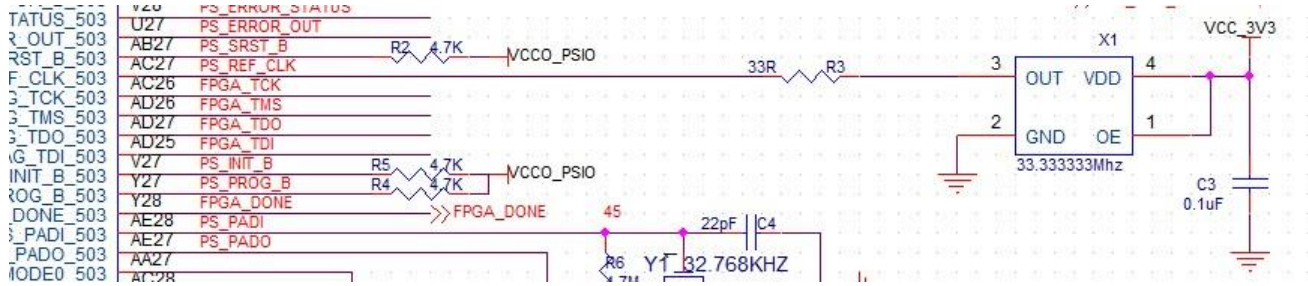


Figure 6-3: Active crystal oscillator in the PS

Clock pin assignment:

Signal Name	Pin
PS_REF_CLK	AC27

PL system clock source:

A differential 200MHz PL system clock source is provided on the board for the reference clock of the DDR4 controller. The crystal output is connected to PL BANK64's Global clock (MRCC), which can be used to drive DDR4 controllers and user logic circuits within the FPGA. Figure 6-4 shows the schematic diagram of the clock source.

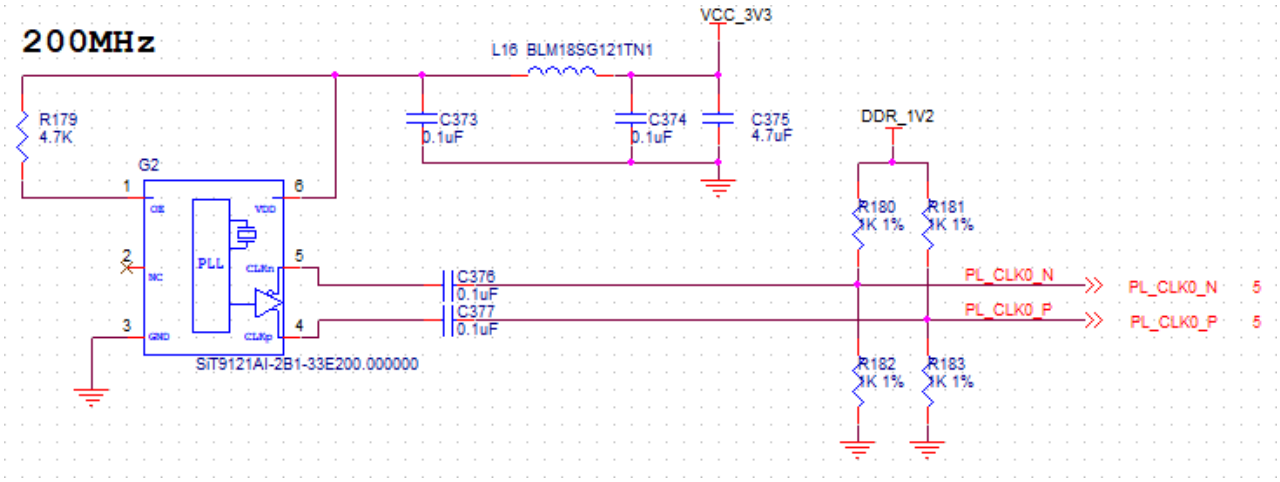


Figure 6-4: PL system clock source

PL Clock pin assignment:

Signal Name	Pin
PL_CLK0_P	H24
PL_CLK0_N	G25

7. Power Supply

The power supply voltage of the Z19 development board is +12V, and +5V, +5V_SATA, +3.3V_PCIE, +3.3V_QSFP, +1.8V power supplies are generated through

multiple-channel DCDC chip inside the board. For the ZYNQ chip's power supply, one MAX20796GFB+ power chip provides 0.85V core power supply for XCZU19EG by 60A current, and two TPS74801DRCR power chips generate 0.85V and 1.8V voltage respectively to supply power for PS_MGT part. Two MAX20812AFH+ power chips are used to generate two-channel 0.9V and two-channel 1.2V voltages respectively to power the PL-MGT part. In addition, TPS6508640, a PMIC chip, is used to generate all other power supplies required by XCZU19EG chip. Please refer to the power supply chip manual to learn the power design of TPS6508640. Figure 7-1 shows the design diagram of TPS6508640:

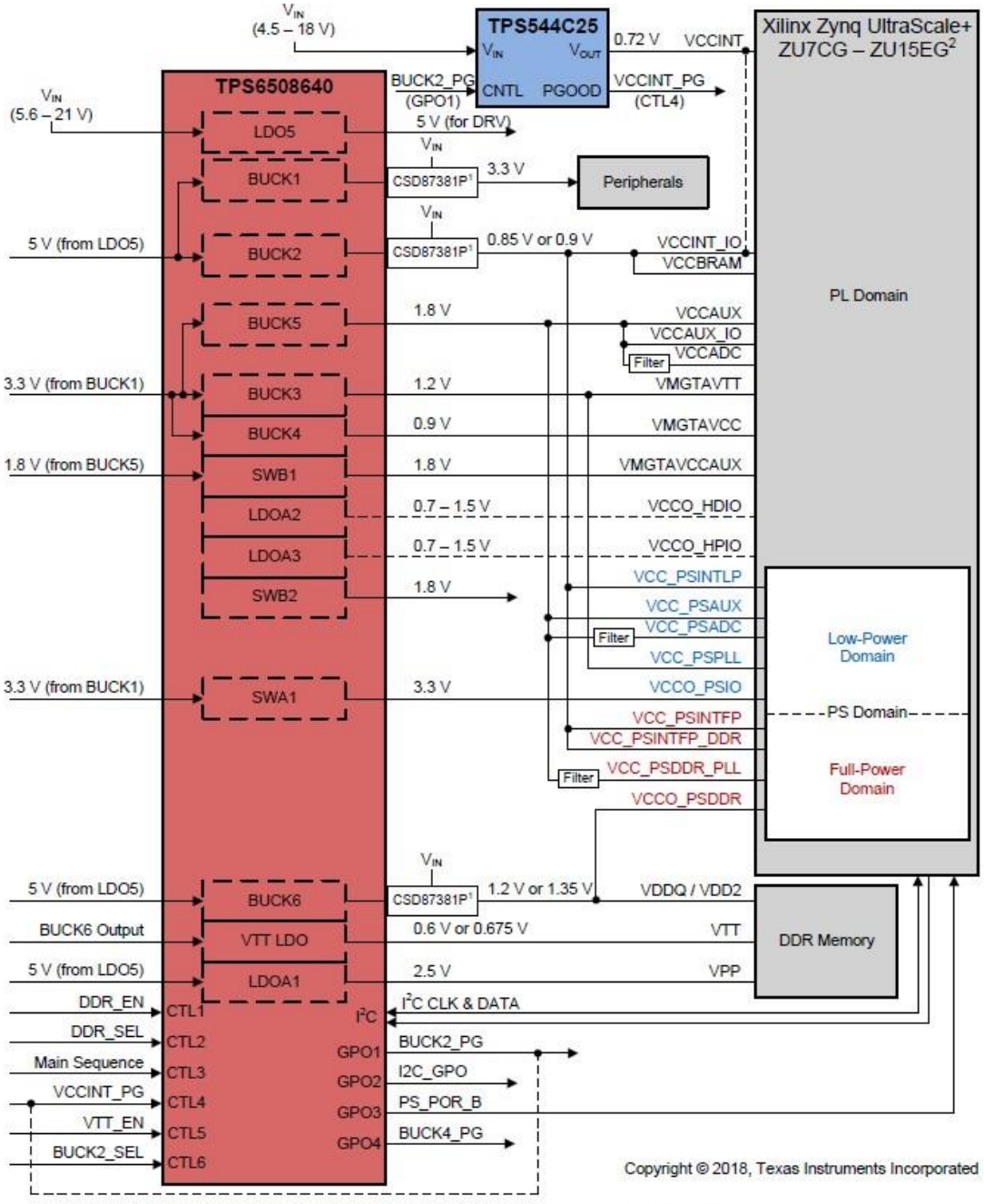


Figure 7-1: The design diagram of TPS6508640

8. M.2 Port

The Z19 development board is equipped with a PCIE x1 standard M.2 port for connecting to M.2 SSDS with communication speeds of up to 6Gbps. The M.2 port uses the M key slot and supports only PCI-E, but not SATA. You need to select a PCIE SSD when selecting an SSD.

The PCIE signal is directly connected to the BANK505 PS MGT transceiver of ZU19EG, and the 1-channel TX signal and RX signal are connected to the LANE1 of the MGT in differential signal mode. The PCIE clock is provided by the Si5332 chip and the frequency is 100Mhz. Figure 8-1 shows the M.2 circuit design.

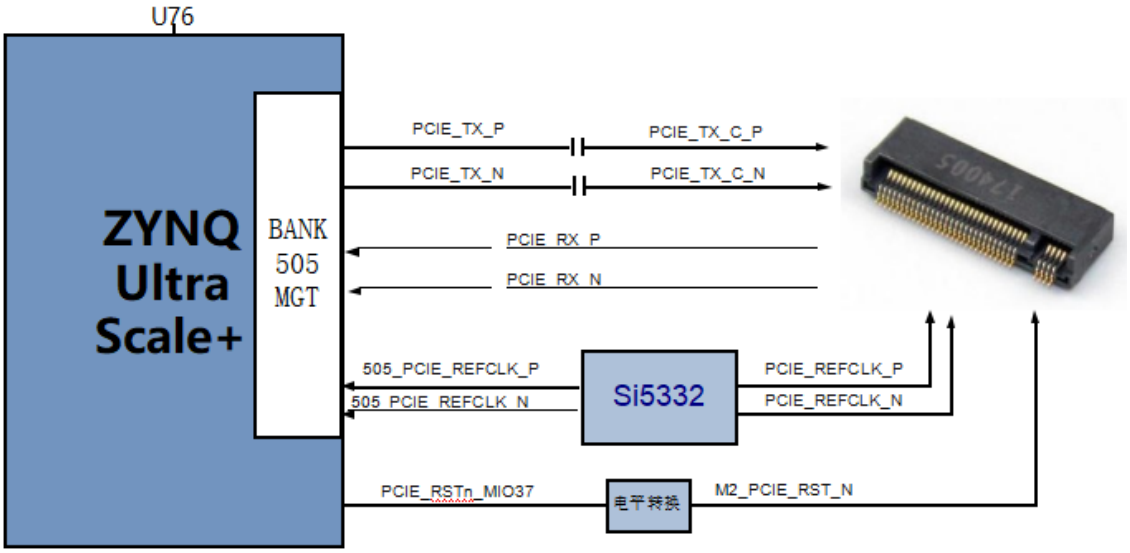


Figure 8-1: M.2 port design diagram

ZYNQ pins assignment of M.2 port is as follows:

Signal Name	Pin Name	Pin Number	Remarks
PCIE_TX_P	PS_MGTRTXP0_505	AH39	PCIE data transmission, Positive
PCIE_TX_N	PS_MGTRTXN0_505	AH40	PCIE data transmission, Negative
PCIE_RX_P	PS_MGTRRXP0_505	AG41	PCIE data reception, Positive
PCIE_RX_N	PS_MGTRRXN0_505	AG42	PCIE data reception, Negative

505_PCIE_REFCLK_P	PS_MGTREFCLK0P_505	AG37	PCIE reference clock, Positive
505_PCIE_REFCLK_N	PS_MGTREFCLK0N_505	AG38	PCIE reference clock, Negative
PCIE_RSTN_MIO37	PS_MIO37_501	N30	PCIE reset signal

9. DP Display Port

The Z19 development board is equipped with a mini DisplayPort output display port for video image display. The port supports VESA DisplayPort V1.2a output standard, up to 4K x 2K@30Fps output, Y-only, YCbCr444, YCbCr422, YCbCr420 and RGB video formats. Each color supports 6, 8, 10, or 12 bits.

The DisplayPort data transmission channel is output directly from the BANK505 PS MGT driver of ZU9EG, and the LANE2 and LANE3 TX signals of the MGT are connected to the DP connector in differential signal mode. The DisplayPort auxiliary channel is connected to the MIO pin of the PS. Figure 9-1 shows the design schematic diagram of DP output port:

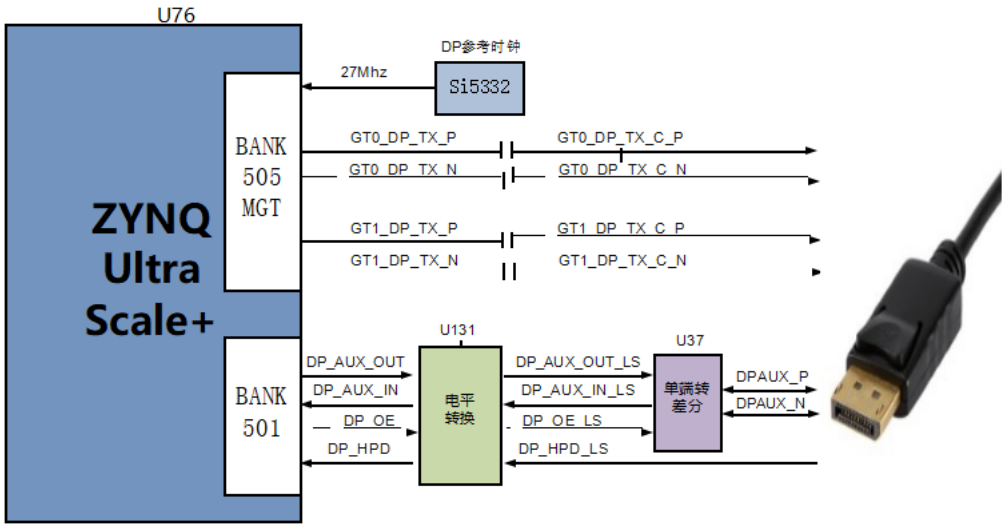


Figure 9-1: The design schematic diagram of DP output port

ZYNQ pin assignment of DisplayPort port:

Signal Name	Pin Name	Pin Number	Remarks
GT0_DP_TX_P	PS_MGTRTXP3_505	AB39	DP data, Low-level transmission, Positive

GT0_DP_TX_N	PS_MGTRTXN3_505	AB40	DP data, Low-level transmission, Negative
GT1_DP_TX_P	PS_MGTRTXP2_505	AD39	DP data, High-level transmission, Positive
GT1_DP_TX_N	PS_MGTRTXN2_505	AD40	DP data, High-level transmission, Negative
505_DP_CLKP	PS_MGTREFCLK2P_505	AC37	DP reference clock, Positive
505_DP_CLKN	PS_MGTREFCLK2N_505	AC38	DP reference clock, Negative
DP_AUX_OUT_MIO27	PS_MIO27_501	L29	DP auxiliary data output
DP_AUX_IN_MIO30	PS_MIO30_501	L30	DP auxiliary data input
DP_OE_MIO29	PS_MIO29_501	M27	DP auxiliary data output enable
DP_HPD_MIO28	PS_MIO28_501	L28	DP insertion signal detection

10. USB3.0 Port

The Z19 expansion board has four USB3.0 ports, supports HOST mode, and delivers data in a transmission speed of up to 5.0Gb/s. USB3.0 is connected through the PIPE3 port, and USB2.0 is connected to the external USB3320C chip through the ULPI port to achieve high-speed data communication between USB3.0 and USB2.0.

The USB port is flat (USB Type A), which is convenient for users to connect different USB Slave peripherals (such as USB mouse, keyboard or USB flash drive) at the same time. The figure 10-1 shows the USB3.0 connection diagram:

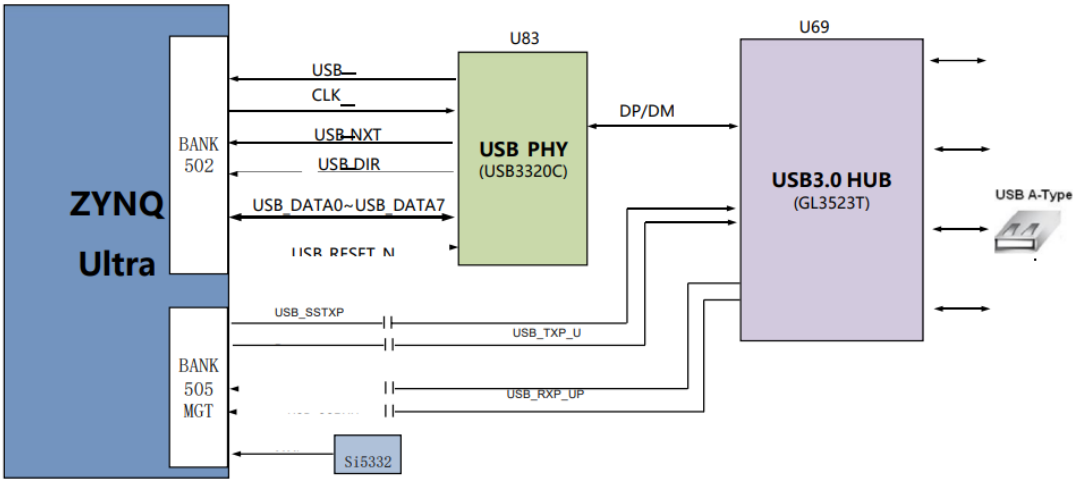


Figure 10-1: USB3.0 port diagram

Pin Assignment of USB port:

Signal Name	Pin Name	Pin Number	Remarks
USB_SSTXP	PS_MGTRTXP1_505	AF39	USB3.0 data transmission, Positive
USB_SSTXN	PS_MGTRTXN1_505	AF40	USB3.0 data transmission, Negative
USB_SSRXP	PS_MGTRRXP1_505	AE41	USB3.0 data reception, Positive
USB_SSRXN	PS_MGTRRXN1_505	AE42	USB3.0 data reception, Negative
USB_DATA0	PS_MIO56_502	AA30	USB2.0 data Bit0
USB_DATA1	PS_MIO57_502	AB30	USB2.0 data Bit1
USB_DATA2	PS_MIO54_502	Y29	USB2.0 data Bit2
USB_DATA3	PS_MIO59_502	AC31	USB2.0 data Bit3
USB_DATA4	PS_MIO60_502	AD29	USB2.0 data Bit4
USB_DATA5	PS_MIO61_502	AC32	USB2.0 data Bit5
USB_DATA6	PS_MIO62_502	AD31	USB2.0 data Bit6
USB_DATA7	PS_MIO63_502	AD30	USB2.0 data Bit7
USB_STP	PS_MIO58_502	AC29	USB2.0 stop signal
USB_DIR	PS_MIO53_502	Y30	USB2.0 data direction signal
USB_CLK	PS_MIO52_502	W29	USB2.0 clock signal
USB_NXT	PS_MIO55_502	AB29	USB2.0 next data signal
USB_RESET_N	PS_MIO44_501	R29	USB2.0 reset signal

11. Gigabit Ethernet Port

The Z19 expansion board has two Gigabit Ethernet ports, one of which is connected to the PS side and the other to the PL side. The GPHY chip uses Micrel's KSZ9031RNX Ethernet PHY chip to provide users with network communication services. The KSZ9031RNX chip supports network transmission rate of 10/100/1000 Mbps and communicates with the MAC layer of ZU9EG system through the RGMII port.

KSZ9031RNX supports MDI/MDX self-adaptive, various speed self-adaptive, Master/Slave self-adaptive, support MDIO bus for PHY register management.

KSZ9031RNX power-on will detect some specific IO level state, so as to determine its own working mode. Table 11-1 describes the default settings of the GPHY chip after it is powered on.

Configure Pin	Description	Configuration Value
PHYAD[2:0]	PHY address in MDIO/MDC mode	The PHY Address is 011
CLK125_EN	Enable 125Mhz clock output selection	Enable
LED_MODE	Enable 125Mhz clock output selection	Single LED light mode
MODE0~MODE3	Link self-adaptive and full-duplex configuration	10/100/1000 self-adaptive, fully compatible Duplex, half-duplex

Table 11-1: Default Settings of the PHY chip

When the network is connected to Gigabit Ethernet, PHY chip KSZ9031RNX will transmit data with ZYNQ through the RGMII bus with a transmission clock of 125Mhz. Data is sampled on the rising edge and falling edge of the clock.

When the network is connected to 100 Gigabit Ethernet, PHY chip KSZ9031RNX will transmit data with ZYNQ through the RGMII bus with a transmission clock of 25Mhz. Data is sampled on the rising edge and falling edge of the clock.

Figure 11-1 shows the connection between ZYNQ and Ethernet PHY chip.

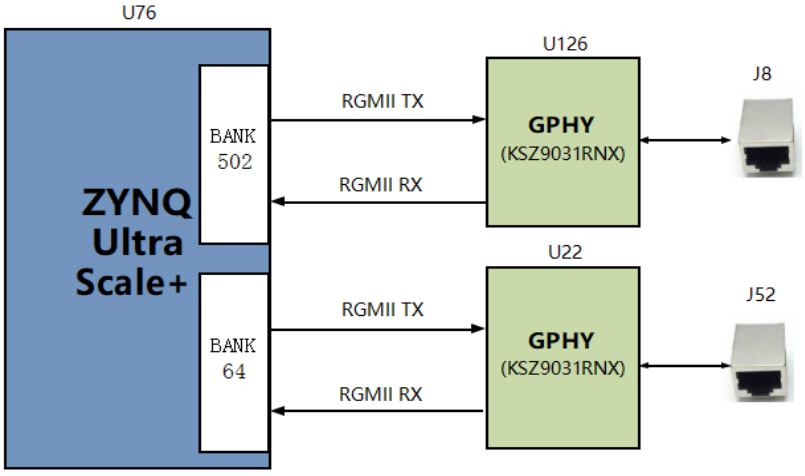


Figure 11-1: Connection between ZYNQ and GPHY

PS Gigabit Ethernet pin assignment is as follows:

Signal Name	Pin Name	Pin Number	Remarks
PHY1_TXCK	PS_MIO64_502	AD32	Ethernet 1 RGMII transmission clock
PHY1_TXD0	PS_MIO65_502	AE29	Ethernet 1 transmission data bit 0
PHY1_TXD1	PS_MIO66_502	AD33	Ethernet 1 transmission data bit 1
PHY1_TXD2	PS_MIO67_502	AE30	Ethernet 1 transmission data bit 2
PHY1_TXD3	PS_MIO68_502	AE33	Ethernet 1 transmission data bit 3
PHY1_TXCTL	PS_MIO69_502	AE32	Ethernet 1 transmission enable signal
PHY1_RXCK	PS_MIO70_502	AF30	Ethernet 1 RGMII reception clock
PHY1_RXD0	PS_MIO71_502	AF31	Ethernet 1 reception data Bit 0
PHY1_RXD1	PS_MIO72_502	AF32	Ethernet 1 reception data Bit 1
PHY1_RXD2	PS_MIO73_502	AG30	Ethernet 1 reception data Bit 2
PHY1_RXD3	PS_MIO74_502	AG33	Ethernet 1 reception data Bit 3
PHY1_RXCTL	PS_MIO75_502	AF33	Ethernet 1 reception data valid signals
PHY1_MDC	PS_MIO76_502	AH31	Ethernet 1 MDIO manage clock
PHY1_MDIO	PS_MIO77_502	AG31	Ethernet 1 MDIO manage data

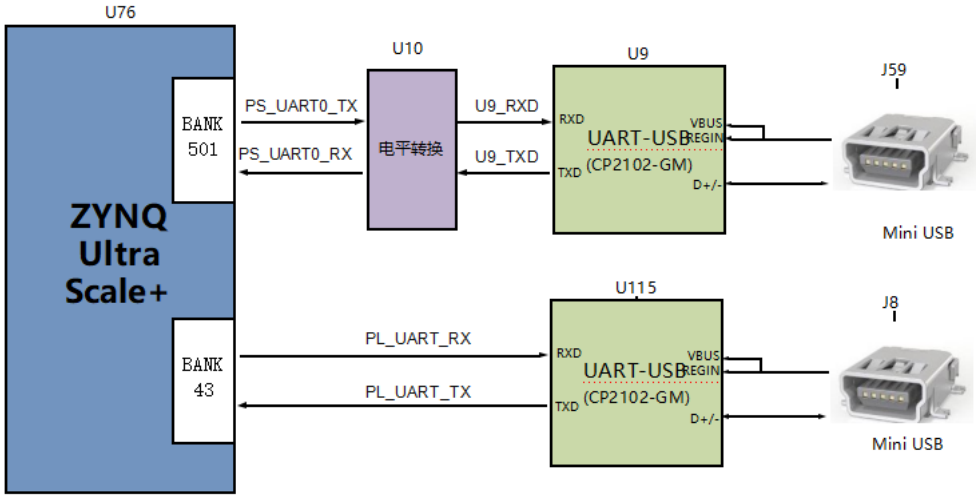
PL Gigabit Ethernet pin assignment is as follows:

Signal Name	Pin Name	Pin No.	Remarks
PHY2_TXCK	IO_L20N_T3L_N3_AD1N_64	AM20	Ethernet 2 RGMII transmission clock
PHY2_TXD0	IO_L24P_T3U_N10_64	AJ22	Ethernet 2 transmission data bit 0
PHY2_TXD1	IO_L24N_T3U_N11_64	AK22	Ethernet 2 transmission data bit 1
PHY2_TXD2	IO_L23P_T3U_N8_64	AJ21	Ethernet 2 transmission data bit 2
PHY2_TXD3	IO_L23N_T3U_N9_64	AJ20	Ethernet 2 transmission data bit 3
PHY2_TXCTL	IO_L20P_T3L_N2_AD1P_64	AM21	Ethernet 2 transmit the enable

			signal
PHY2_RXCK	IO_L14P_T2L_N2_GC_64	AT20	Ethernet 2 RMII reception clock
PHY2_RXD0	IO_L22P_T3U_N6_DBC_AD0P_64	AK20	Ethernet 2 reception data Bit 0
PHY2_RXD1	IO_L22N_T3U_N7_DBC_AD0N_64	AK19	Ethernet 2 reception data Bit 1
PHY2_RXD2	IO_L21P_T3L_N4_AD8P_64	AL22	Ethernet 2 reception data Bit 2
PHY2_RXD3	IO_L21N_T3L_N5_AD8N_64	AL21	Ethernet 2 reception data Bit 3
PHY2_RXCTL	IO_L14N_T2L_N3_GC_64	AU19	Ethernet 2 reception data valid signals
PHY2_MDC	IO_T1U_N12_64	AW21	Ethernet 2 MDIO manage clock
PHY2_MDIO	IO_T2U_N12_64	AR22	Ethernet 2 MDIO manage data
PHY2_RESET	IO_T3U_N12_64	AL20	Ethernet 2 reset signal

12. Uart Port

The Z19 expansion board is equipped with three Uart ports. Two of them are extracted from the MINI USB port through the UART to USB chip, one is connected to the PS side, and one is connected to the PL side. The conversion chip is Silicon Labs CP2102GM chip, which can be connected to the USB port of the PC with a USB cable for serial data communication. The schematic diagram of USB Uart circuit design is shown in the following figure:



The third UART port is extracted from the PS side through a FPC connector with 1-mm spacing and 10-pin, which can be used to connect peripherals such as the serial screen.

USB-to-serial ZYNQ pin assignment:

Signal Name	Pin Name	Pin Number	Remarks
PS_UART_TX	PS_MIO39_501	P29	PS Uart1 data output
PS_UART_RX	PS_MIO38_501	R27	PS Uart1 data input
PL_UART_TX	IO_L8N_HDGC_94	C3	PL Uart data output
PL_UART_RX	IO_L7P_HDGC_94	C6	PL Uart data input
PS_UART2_TX	PS_MIO32_501	M30	PS Uart1 data output
PS_UART2_RX	PS_MIO33_501	N28	PS Uart1 data input

13. SD Card Slot

The Z19 expansion board includes a Micro SD card port to provide user access to the SD card memory used to store the ZU19EG chip’ s BOOT program, the Linux operating system kernel, the file system, and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of ZU19EG, and we connect BANK 501 and SD card through the TXS02612 level converter because the VCCIO of the 501 is set to 1.8V, but the data level of the SD card is 3.3V. The schematics of the ZU19EG PS and SD card connectors are shown in Figure 13-1.

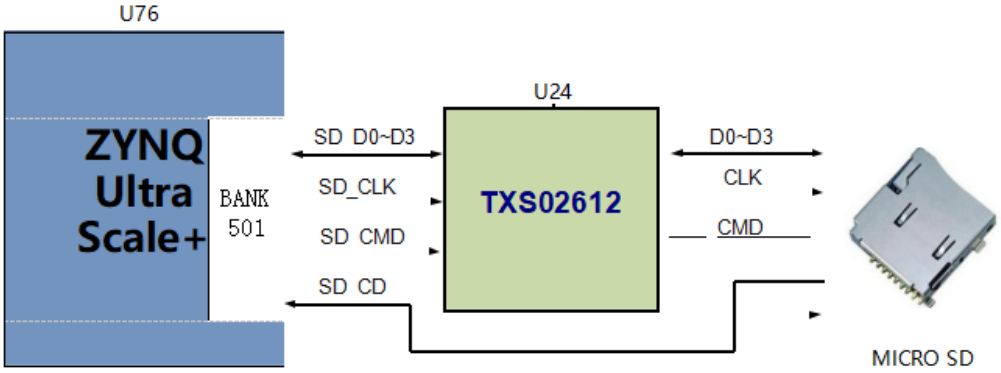


Figure 13-1: Diagram of the SD card connection

SD card slot pin assignment:

Signal Name	Pin Name	Pin Number	Remarks
SD_CMD	PS_MIO50_501	V29	SD clock signal
SD_CD	PS_MIO45_501	T29	SD command signal
SD_D0	PS_MIO46_501	U28	SD data Data0
SD_D1	PS_MIO47_501	T28	SD data Data1
SD_D2	PS_MIO48_501	V30	SD data Data2
SD_D3	PS_MIO49_501	U29	SD Data Data3
SD_CMD	PS_MIO50_501	V29	SD card detection signal

14. Fiber Interface

There are four QSFP28 fiber interfaces on the Z19 expansion board. Users can purchase the QSFP optical module and insert it into these four fiber interfaces for optical fiber data communication. The four fiber interfaces are connected to the four RX/TX channels of ZYNQ's BANK128-131 GTY transceiver, providing four separate transmission and reception channels, each capable of 25Gbps operation at 100 meters of the OM4MMF, with an overall data rate of 100Gbps. The reference clock of the BANK128-131 is 125Mhz provided by the Si5332BD11025-4 chip (can be changed to 156.25M by resistor).

Figure 14-1 shows the ZYNQ Ultrascale+ and optical fiber design.

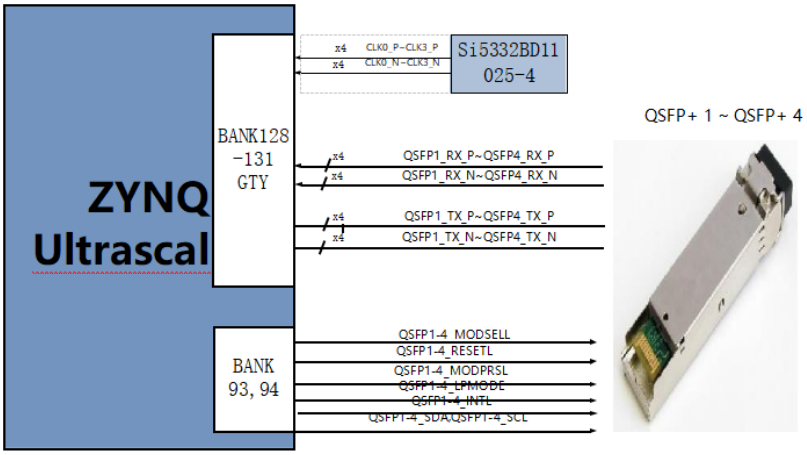


Figure 14-1: Schematic design of the optical fiber

ZYNQ pins assignments of the four fiber interfaces are as follows:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Remarks
QSFP1_RX1_N	MGTYRXN0_128	W42	Optical module 1 data reception negative 1
QSFP1_RX1_P	MGTYRXP0_128	W41	Optical module 1 data reception positive 1
QSFP1_RX2_N	MGTYRXN1_128	V40	Optical module 1 data reception negative 2
QSFP1_RX2_P	MGTYRXP1_128	V39	Optical module 1 data reception positive 2
QSFP1_RX3_N	MGTYRXN2_128	U42	Optical module 1 data reception negative 3
QSFP1_RX3_P	MGTYRXP2_128	U41	Optical module 1 data reception positive 3
QSFP1_RX4_N	MGTYRXN3_128	T40	Optical module 1 data reception negative 4
QSFP1_RX4_P	MGTYRXP3_128	T39	Optical module 1 data reception positive 4
QSFP1_TX1_N	MGTYTXN0_128	Y35	Optical module 1 data transmission negative 1
QSFP1_TX1_P	MGTYTXP0_128	Y34	Optical module 1 data transmission positive 1
QSFP1_TX2_N	MGTYTXN1_128	W37	Optical module 1 data transmission negative 2
QSFP1_TX2_P	MGTYTXP1_128	W36	Optical module 1 data transmission positive 2
QSFP1_TX3_N	MGTYTXN2_128	V35	Optical module 1 data transmission negative 3
QSFP1_TX3_P	MGTYTXP2_128	V34	Optical module 1 data transmission positive 3

QSFP1_TX4_N	MGTYTXN3_128	U37	Optical module 1 data transmission negative 4
QSFP1_TX4_P	MGTYTXP3_128	U36	Optical module 1 data transmission positive 4
128_CLK0_N	MGTREFCLK0N_128	AB35	BANK128 reference clock negative
128_CLK0_P	MGTREFCLK0P_128	AB34	BANK reference clock positive
QSFP1_SCL	IO_L3N_AD9N_93	H9	I2C clock of optical module 1
QSFP1_SDA	IO_L5P_HDGC_AD7P_93	G7	I2C data of optical module 1
QSFP1_INTL	IO_L2P_AD10P_93	J8	Optical module 1 interrupt signal
QSFP1_LPMODE	IO_L1P_AD11P_93	G6	Optical module 1 low-power selection signal
QSFP1_MODPRSL	IO_L3P_AD9P_93	J9	Optical module 1 existence indicator signal
QSFP1_MODSELL	IO_L2N_AD10N_93	H8	Optical module 1 module selection signal
QSFP1_RESETL	IO_L1N_AD11N_93	F6	Optical module 1 reset signal
QSFP2_RX1_N	MGTYRXN0_129	R42	Optical module 2 data reception negative 1
QSFP2_RX1_P	MGTYRXP0_129	R41	Optical module 2 data reception positive 1
QSFP2_RX2_N	MGTYRXN1_129	P40	Optical module 2 data reception negative 2
QSFP2_RX2_P	MGTYRXP1_129	P39	Optical module 2 data reception positive 2
QSFP2_RX3_N	MGTYRXN2_129	N42	Optical module 2 data reception negative 3
QSFP2_RX3_P	MGTYRXP2_129	N41	Optical module 2 data reception positive 3
QSFP2_RX4_N	MGTYRXN3_129	M40	Optical module 2 data reception negative 4

QSFP2_RX4_P	MGTYRXP3_129	M39	Optical module 2 data reception positive 4
QSFP2_TX1_N	MGTYTXN0_129	T35	Optical module 2 data transmission negative 1
QSFP2_TX1_P	MGTYTXP0_129	T34	Optical module 2 data transmission positive 1
QSFP2_TX2_N	MGTYTXN1_129	R37	Optical module 2 data transmission negative 2
QSFP2_TX2_P	MGTYTXP1_129	R36	Optical module 2 data transmission positive 2
QSFP2_TX3_N	MGTYTXN2_129	P35	Optical module 2 data transmission negative 3
QSFP2_TX3_P	MGTYTXP2_129	P34	Optical module 2 data transmission positive 3
QSFP2_TX4_N	MGTYTXN3_129	N37	Optical module 2 data transmission negative 4
QSFP2_TX4_P	MGTYTXP3_129	N36	Optical module 2 data transmission positive 4
129_CLK0_N	MGTREFCLK0N_129	W33	BANK129 reference clock negative
129_CLK0_P	MGTREFCLK0P_129	W32	BANK129 reference clock positive
QSFP2_SCL	IO_L4N_AD8N_93	E9	I2C clock of optical module 2
QSFP2_SDA	IO_L12P_AD0P_93	D9	I2C data of optical module 2
QSFP2_INTL	IO_L6N_HDGC_AD6N_93	F8	Optical module 2 interrupt signal
QSFP2_LPMODE	IO_L6P_HDGC_AD6P_93	G8	Optical module 2 low-power selection signal
QSFP2_MODPRSL	IO_L8P_HDGC_AD4P_93	D8	Optical module 2 existence indicator signal
QSFP2_MODSELL	IO_L5N_HDGC_AD7N_93	F7	Optical module 2 module selection signal
QSFP2_RESETL	IO_L4P_AD8P_93	F9	Optical module 2 reset signal

QSFP3_RX1_N	MGTYRXN0_130	L42	Optical module 3 data reception negative 1
QSFP3_RX1_P	MGTYRXP0_130	L41	Optical module 3 data reception positive 1
QSFP3_RX2_N	MGTYRXN1_130	K40	Optical module 3 data reception negative 2
QSFP3_RX2_P	MGTYRXP1_130	K39	Optical module 3 data reception positive 2
QSFP3_RX3_N	MGTYRXN2_130	J42	Optical module 3 data reception negative 3
QSFP3_RX3_P	MGTYRXP2_130	J41	Optical module 3 data reception positive 3
QSFP3_RX4_N	MGTYRXN3_130	H40	Optical module 3 data reception negative 4
QSFP3_RX4_P	MGTYRXP3_130	H39	Optical module 3 data reception positive 4
QSFP3_TX1_N	MGTYTXN0_130	M35	Optical module 3 data transmission negative 1
QSFP3_TX1_P	MGTYTXP0_130	M34	Optical module 3 data transmission positive 1
QSFP3_TX2_N	MGTYTXN1_130	L37	Optical module 3 data transmission negative 2
QSFP3_TX2_P	MGTYTXP1_130	L36	Optical module 3 data transmission positive 2
QSFP3_TX3_N	MGTYTXN2_130	K35	Optical module 3 data transmission negative 3
QSFP3_TX3_P	MGTYTXP2_130	K34	Optical module 3 data transmission positive 3
QSFP3_TX4_N	MGTYTXN3_130	J37	Optical module 3 data transmission negative 4
QSFP3_TX4_P	MGTYTXP3_130	J36	Optical module 3 data

			transmission positive 4
130_CLK0_N	MGTREFCLK0N_130	R33	BANK130 reference clock negative
130_CLK0_P	MGTREFCLK0P_130	R32	BANK130 reference clock positive
QSFP3_SCL	IO_L7N_HDGC_AD5N_93	D7	I2C clock of optical module 3
QSFP3_SDA	IO_L10P_AD2P_93	B7	I2C data of optical module 3
QSFP3_INTL	IO_L7P_HDGC_AD5P_93	E7	Optical module 3 interrupt signal
QSFP3_LPMODE	IO_L12N_AD0N_93	C9	Optical module 3 low-power selection signal
QSFP3_MODPRSL	IO_L10N_AD2N_93	A7	Optical module 3 existence indicator signal
QSFP3_MODSELL	IO_L8N_HDGC_AD4N_93	C8	Optical module 3 module selection signal
QSFP3_RESETL	IO_L11N_AD1N_93	A8	Optical module 3 reset signal
QSFP4_RX1_N	MGTYRXN0_131	G42	Optical module 4 data reception negative 1
QSFP4_RX1_P	MGTYRXP0_131	G41	Optical module 4 data reception positive 1
QSFP4_RX2_N	MGTYRXN1_131	F40	Optical module 4 data reception negative 2
QSFP4_RX2_P	MGTYRXP1_131	F39	Optical module 4 data reception positive 2
QSFP4_RX3_N	MGTYRXN2_131	E42	Optical module 4 data reception negative 3
QSFP4_RX3_P	MGTYRXP2_131	E41	Optical module 4 data reception positive 3
QSFP4_RX4_N	MGTYRXN3_131	D40	Optical module 4 data reception negative 4
QSFP4_RX4_P	MGTYRXP3_131	D39	Optical module 4 data reception positive 4
QSFP4_TX1_N	MGTYTXN0_131	H35	Optical module 4 data

			transmission negative 1
QSFP4_TX1_P	MGTYTXP0_131	H34	Optical module 4 data transmission positive 1
QSFP4_TX2_N	MGTYTXN1_131	G37	Optical module 4 data transmission negative 2
QSFP4_TX2_P	MGTYTXP1_131	G36	Optical module 4 data transmission positive 2
QSFP4_TX3_N	MGTYTXN2_131	F35	Optical module 4 data transmission negative 3
QSFP4_TX3_P	MGTYTXP2_131	F34	Optical module 4 data transmission positive 3
QSFP4_TX4_N	MGTYTXN3_131	E37	Optical module 4 data transmission negative 4
QSFP4_TX4_P	MGTYTXP3_131	E36	Optical module 4 data transmission positive 4
131_CLK0_N	MGTREFCLK0N_131	L33	BANK131 reference clock negative
131_CLK0_P	MGTREFCLK0P_131	L32	BANK131 reference clock positive
QSFP4_SCL	IO_L2N_AD14N_94	E4	I2C clock of optical module 4
QSFP4_SDA	IO_L4N_AD12N_94	D1	I2C data of optical module 4
QSFP4_INTL	IO_L3P_AD13P_94	E3	Optical module 4 interrupt signal
QSFP4_LPMODE	IO_L2P_AD14P_94	E5	Optical module 4 low-power selection signal
QSFP4_MODPRSL	IO_L3N_AD13N_94	E2	Optical module 4 existence indicator signal
QSFP4_MODSELL	IO_L1P_AD15P_94	F5	Optical module 4 module selection signal
QSFP4_RESETL	IO_L1N_AD15N_94	F4	Optical module 3 reset signal

15. CAN Communication Interface

There are two CAN communication interfaces on the Z19 development board, which are connected to the MIO interface of BANK501 at the end of PS system. ISO1042BDWVR chip, a CAN transceiver chip, is used to provide CAN communication services for users.

Figure 15-1 shows the connection diagram of the PS-end CAN transceiver chip:

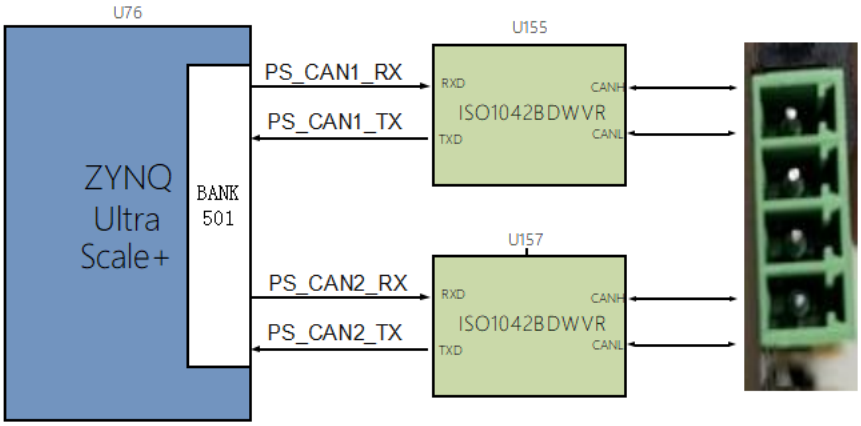


Figure 15-1: Connection diagram of the PS CAN transceiver chip

CAN communication pin assignment is as follows:

Signal Name	Pin Name	Pin Number	Remarks
CAN0_RX	PS_MIO34_501	P27	CAN0 receiver
CAN0_TX	PS_MIO35_501	N29	CAN0 sender
CAN1_RX	PS_MIO41_501	P30	CAN1 receiver
CAN1_TX	PS_MIO40_501	P28	CAN1 sender

16. 485 Communication Interface

There are two 485 communication interfaces on the Z19 development board, and they are connected to the IO interface of BANK90 and BANK91 at the PL side. ISO3088DWR chip, the 485 transceiver chip, is used to provide 485 communication services for users.

Figure 16-1 shows the connection diagram of the PL-end 485 transceiver chip.

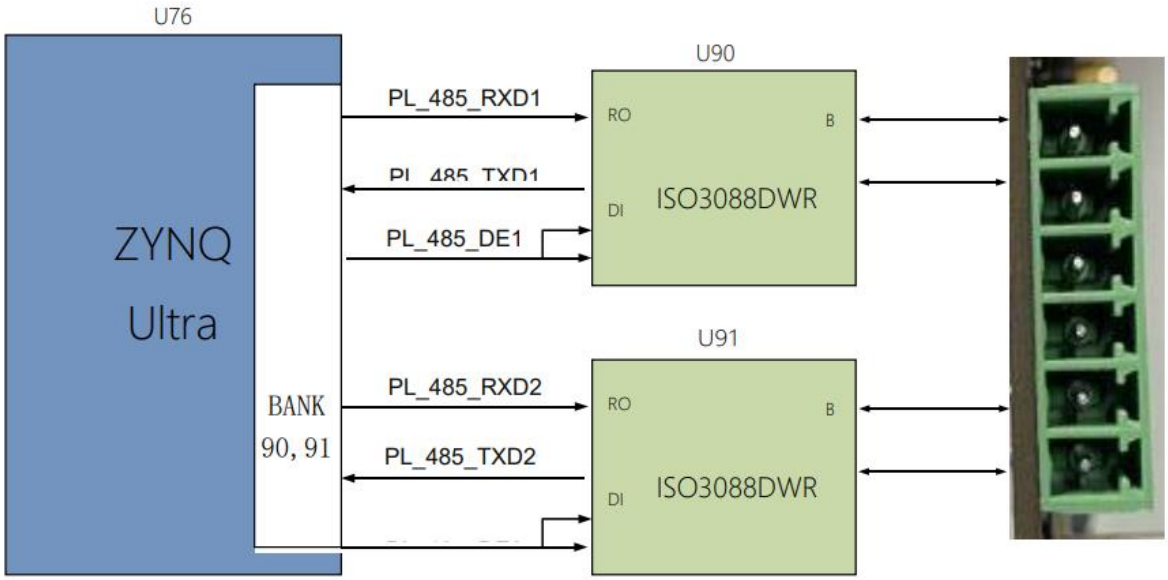


Figure 16-1: The connection diagram of the PL-end 485 transceiver chip

RS485 communication pin assignment is as follows:

Signal Name	Pin Name	Pin Number	Remarks
PL_485_DE1	IO_L11P_AD1P_90	K14	The 1st 485 send enable
PL_485_DE2	IO_L10P_AD10P_91	C10	The 2nd 485 send enable
PL_485_RXD1	IO_L11N_AD1N_90	J14	The 1st 485 receiver
PL_485_RXD2	IO_L10N_AD10N_91	B10	The 2nd 485 sender
PL_485_TXD1	IO_L9P_AD11P_91	D11	The 1st 485 receiver
PL_485_TXD2	IO_L11N_AD9N_91	B11	The 2nd 485 sender

17. MIPI Interface

The development board includes a MIPI camera interface that can be used to connect to our MIPI OV5640 camera module (AN5641). 15PIN FPC connector of MIPI interface contains 2 lanes of data and 1 pair of clocks connected to differential IO pins of BANK68; Other control signals are connected to the IO of the BANK91.

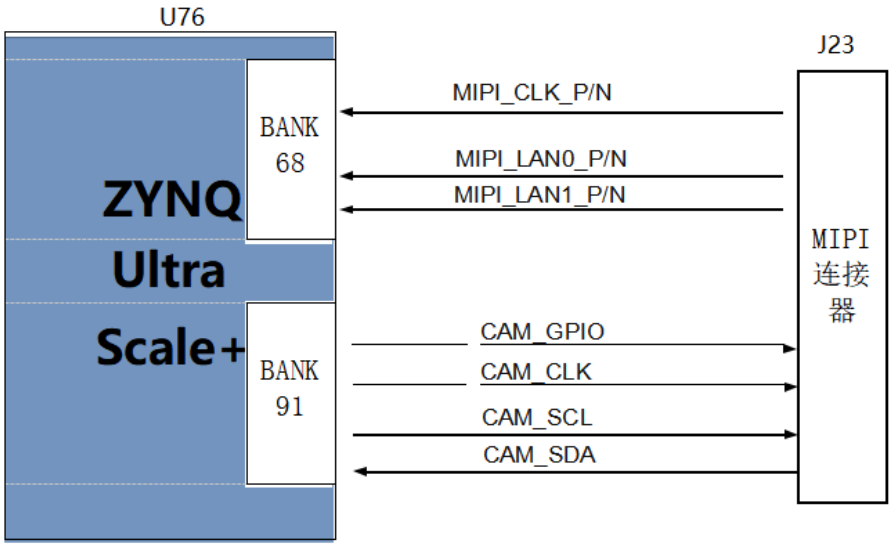


Figure 17-1: Design schematic diagram of the HDMI port

MIPI interface pin assignment:

Signal Name	Pin Name	Pin Number	Remarks
MIPI_CLK_N	IO_L1N_T0L_N1_DBC_68	N15	MIPI input clock negative
MIPI_CLK_P	IO_L1P_T0L_N0_DBC_68	P15	MIPI input clock positive
MIPI_LAN0_N	IO_L2N_T0L_N3_68	N16	MIPI input data LANE0 negative
MIPI_LAN0_P	IO_L2P_T0L_N2_68	P16	MIPI input data LANE0 positive
MIPI_LAN1_N	IO_L3N_T0L_N5_AD15N_68	M16	MIPI input data LANE1 negative
MIPI_LAN1_P	IO_L3P_T0L_N4_AD15P_68	M17	MIPI input data LANE1 positive
CAM_CLK	IO_L6P_HDGC_91	F13	Clock input of camera
CAM_GPIO	IO_L6N_HDGC_91	F12	GPIO control of camera
CAM_SCL	IO_L7N_HDGC_91	E10	I2C clock of camera
CAM_SDA	IO_L7P_HDGC_91	E11	I2C data of camera

18. FMC Connector

Z19 development board is equipped with two FMC HPC expansion ports to form the standard double-width FMC interface, which can be externally connected to XILINX or our various FMC modules (HDMI input/output module, binocular camera module, high-speed AD module, etc.). The FMC1 expansion port contains 36 pairs of differential IO signals and 8 groups of GTH transceiver signals, and the FMC2 expansion port contains 60 pairs of differential IO signals and 8 groups of GTH transceiver signals.

The 36 pairs of differential signals of the FMC1 expansion port are connected to the IO of the BANK67, 68 of the ZYNQ Ultrascale+ chip, the level standard is 1.8V or 1.2V (chose by hop cap J5), and the differential signal supports LVDS data communication. Eight sets of GTH transceiver signals are connected to BANK230 and BANK231. Figure 18-1 shows the schematic diagram of the ZYNQ Ultrascale+ and FMC1 connector.

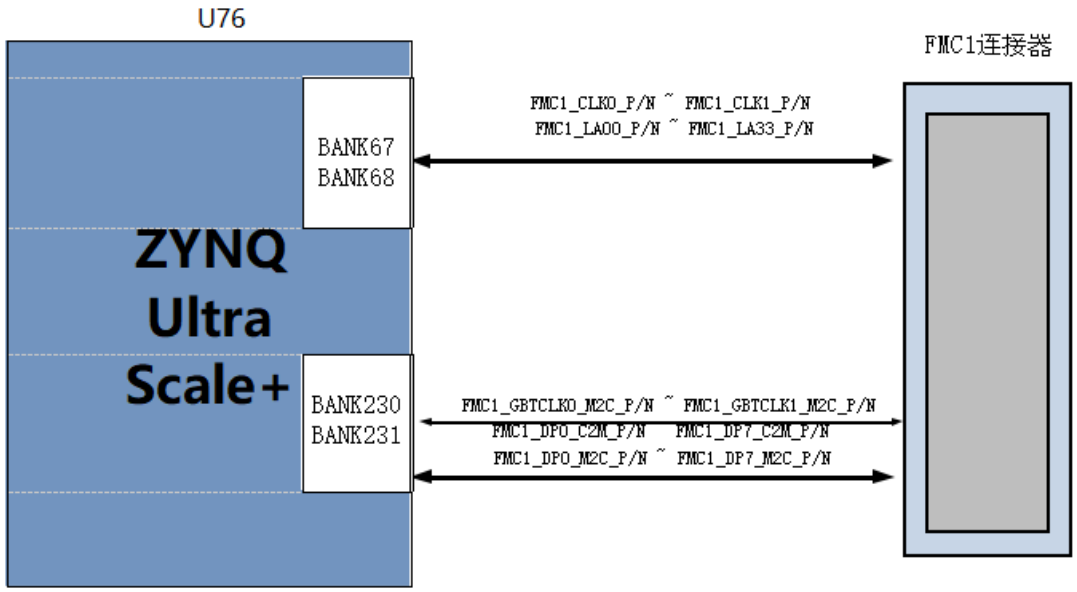


Figure 18-1: Connection of the FMC1 connector

FMC1 connector pin assignment:

Signal Name	ZYNQ Pin Name	Pin No.	Remarks
FMC1_GBTCLK0_M2C_C_N	MGTREFCLK1N_230	U9	FMC1 transceiver reference clock 0, Negative
FMC1_GBTCLK0_M2C_C_P	MGTREFCLK1P_230	U10	FMC1 transceiver reference clock 0, Positive

FMC1_GBTCLK1_M2C_N	MGTREFCLK0N_230	V11	FMC1 transceiver reference clock 1, Negative
FMC1_GBTCLK1_M2C_P	MGTREFCLK0P_230	V12	FMC1 transceiver reference clock 1, Positive
FMC1_DP4_C2M_N	MGTHTXN2_230	N5	FMC1 transceiver data transmission 4, Negative
FMC1_DP4_C2M_P	MGTHTXP2_230	N6	FMC1 transceiver data transmission 4, Positive
FMC1_DP4_M2C_N	MGTHRXN2_230	P3	FMC1 transceiver data reception 5, Negative
FMC1_DP4_M2C_P	MGTHRXP2_230	P4	FMC1 transceiver data reception 5, Positive
FMC1_DP5_C2M_N	MGTHTXN0_230	R5	FMC1 transceiver data transmission 5, Negative
FMC1_DP5_C2M_P	MGTHTXP0_230	R6	FMC1 transceiver data transmission 5, Positive
FMC1_DP5_M2C_N	MGTHRXN0_230	T3	FMC1 transceiver data reception 5, Negative
FMC1_DP5_M2C_P	MGTHRXP0_230	T4	FMC1 transceiver data reception 5, Positive
FMC1_DP6_C2M_N	MGTHTXN1_230	P7	FMC1 transceiver data transmission 6, Negative
FMC1_DP6_C2M_P	MGTHTXP1_230	P8	FMC1 transceiver data transmission 6, Positive
FMC1_DP6_M2C_N	MGTHRXN1_230	R1	FMC1 transceiver data reception 6, Negative
FMC1_DP6_M2C_P	MGTHRXP1_230	R2	FMC1 transceiver data reception 6, Positive
FMC1_DP7_C2M_N	MGTHTXN3_230	M7	FMC1 transceiver data transmission 7, Negative
FMC1_DP7_C2M_P	MGTHTXP3_230	M8	FMC1 transceiver data transmission

			7, Positive
FMC1_DP7_M2C_N	MGTHRXN3_230	N1	FMC1 transceiver data reception 7, Negative
FMC1_DP7_M2C_P	MGTHRXP3_230	N2	FMC1 transceiver data reception 7, Positive
FMC1_DP0_C2M_N	MGTHTXN3_231	H3	FMC1 transceiver data transmission 0, Negative
FMC1_DP0_C2M_P	MGTHTXP3_231	H4	FMC1 transceiver data transmission 0, Positive
FMC1_DP0_M2C_N	MGTHRXN3_231	G1	FMC1 transceiver data reception 0, Negative
FMC1_DP0_M2C_P	MGTHRXP3_231	G2	FMC1 transceiver data reception 0, Positive
FMC1_DP1_C2M_N	MGTHTXN2_231	J5	FMC1 transceiver data transmission 1, Negative
FMC1_DP1_C2M_P	MGTHTXP2_231	J6	FMC1 transceiver data transmission 1, Positive
FMC1_DP1_M2C_N	MGTHRXN2_231	J1	FMC1 transceiver data reception 1, Negative
FMC1_DP1_M2C_P	MGTHRXP2_231	J2	FMC1 transceiver data reception 1, Positive
FMC1_DP2_C2M_N	MGTHTXN1_231	K3	FMC1 transceiver data transmission 2, Negative
FMC1_DP2_C2M_P	MGTHTXP1_231	K4	FMC1 transceiver data transmission 2, Positive
FMC1_DP2_M2C_N	MGTHRXN1_231	L1	FMC1 transceiver data reception 2, Negative
FMC1_DP2_M2C_P	MGTHRXP1_231	L2	FMC1 transceiver data reception 2, Positive
FMC1_DP3_C2M_N	MGTHTXN0_231	L5	FMC1 transceiver data transmission 3, Negative

FMC1_DP3_C2M_P	MGTHTXP0_231	L6	FMC1 transceiver data transmission 3, Positive
FMC1_DP3_M2C_N	MGTHRXN0_231	M3	FMC1 transceiver data reception 3, Negative
FMC1_DP3_M2C_P	MGTHRXP0_231	M4	FMC1 transceiver data reception 3, Positive
FMC1_CLK0_N	IO_L13N_T2L_N1_GC_QBC_68	E14	FMC1 1st channel reference clock N
FMC1_CLK0_P	IO_L13P_T2L_N0_GC_QBC_68	F14	FMC1 1st channel reference clock P
FMC1_CLK1_N	IO_L12N_T1U_N11_GC_67	AT10	FMC1 2nd channel reference clock N
FMC1_CLK1_P	IO_L12P_T1U_N10_GC_67	AT11	FMC1 2nd channel reference clock P
FMC1_LA00_CC_N	IO_L11N_T1U_N9_GC_68	F17	FMC1 refers to 0 channel data N
FMC1_LA00_CC_P	IO_L11P_T1U_N8_GC_68	G17	FMC1 refers to 0 channel data P
FMC1_LA01_CC_N	IO_L12N_T1U_N11_GC_68	F15	FMC1 refers to 1st channel data N
FMC1_LA01_CC_P	IO_L12P_T1U_N10_GC_68	G16	FMC1 refers to 1st channel data P
FMC1_LA02_N	IO_L6N_T0U_N11_AD6N_68	K17	FMC1 refers to 2nd channel data N
FMC1_LA02_P	IO_L6P_T0U_N10_AD6P_68	L17	FMC1 refers to 2nd channel data P
FMC1_LA03_N	IO_L17N_T2U_N9_AD10N_68	A13	FMC1 refers to 3rd channel data N
FMC1_LA03_P	IO_L17P_T2U_N8_AD10P_68	A14	FMC1 refers to 3rd channel data P
FMC1_LA04_N	IO_L24N_T3U_N11_68	A18	FMC1 refers to 4th channel data N
FMC1_LA04_P	IO_L24P_T3U_N10_68	B18	FMC1 refers to 4th channel data P
FMC1_LA05_N	IO_L16N_T2U_N7_QBC_AD3N_68	A12	FMC1 refers to 5th channel data N
FMC1_LA05_P	IO_L16P_T2U_N6_QBC_AD3P_68	B13	FMC1 refers to 5th channel data P
FMC1_LA06_N	IO_L21N_T3L_N5_AD8N_68	D17	FMC1 refers to 6th channel data N
FMC1_LA06_P	IO_L21P_T3L_N4_AD8P_68	E17	FMC1 refers to 6th channel data P
FMC1_LA07_N	IO_L23N_T3U_N9_68	C18	FMC1 refers to 7th channel data N
FMC1_LA07_P	IO_L23P_T3U_N8_68	D18	FMC1 refers to 7th channel data P

FMC1_LA08_N	IO_L22N_T3U_N7_DBC_AD0N_68	A17	FMC1 refers to 8th channel data N
FMC1_LA08_P	IO_L22P_T3U_N6_DBC_AD0P_68	B17	FMC1 refers to 8th channel data P
FMC1_LA09_N	IO_L20N_T3L_N3_AD1N_68	B16	FMC1 refers to 9th channel data N
FMC1_LA09_P	IO_L20P_T3L_N2_AD1P_68	C16	FMC1 refers to 9th channel data P
FMC1_LA10_N	IO_L15N_T2L_N5_AD11N_68	C13	FMC1 refers to 10th channel data N
FMC1_LA10_P	IO_L15P_T2L_N4_AD11P_68	D13	FMC1 refers to 10th channel data P
FMC1_LA11_N	IO_L4N_T0U_N7_DBC_AD7N_68	L15	FMC1 refers to 11th channel data N
FMC1_LA11_P	IO_L4P_T0U_N6_DBC_AD7P_68	M15	FMC1 refers to 11th channel data P
FMC1_LA12_N	IO_L19N_T3L_N1_DBC_AD9N_68	D16	FMC1 refers to 12th channel data N
FMC1_LA12_P	IO_L19P_T3L_N0_DBC_AD9P_68	E16	FMC1 refers to 12th channel data P
FMC1_LA13_N	IO_L5N_T0U_N9_AD14N_68	K15	FMC1 refers to 13th channel data N
FMC1_LA13_P	IO_L5P_T0U_N8_AD14P_68	K16	FMC1 refers to 13th channel data P
FMC1_LA14_N	IO_L1N_T0L_N1_DBC_68	N15	FMC1 refers to 14th channel data N
FMC1_LA14_P	IO_L1P_T0L_N0_DBC_68	P15	FMC1 refers to 14th channel data P
FMC1_LA15_N	IO_L2N_T0L_N3_68	N16	FMC1 refers to 15th channel data N
FMC1_LA15_P	IO_L2P_T0L_N2_68	P16	FMC1 refers to 15th channel data P
FMC1_LA16_N	IO_L3N_T0L_N5_AD15N_68	M16	FMC1 refers to 16th channel data N
FMC1_LA16_P	IO_L3P_T0L_N4_AD15P_68	M17	FMC1 refers to 16th channel data P
FMC1_LA17_CC_N	IO_L13N_T2L_N1_GC_QBC_67	AR12	FMC1 refers to 17th channel data N
FMC1_LA17_CC_P	IO_L13P_T2L_N0_GC_QBC_67	AR13	FMC1 refers to 17th channel data P
FMC1_LA18_CC_N	IO_L11N_T1U_N9_GC_67	AT12	FMC1 refers to 18th channel data N
FMC1_LA18_CC_P	IO_L11P_T1U_N8_GC_67	AT13	FMC1 refers to 18th channel data P
FMC1_LA19_N	IO_L15N_T2L_N5_AD11N_67	AR14	FMC1 refers to 19th channel data N
FMC1_LA19_P	IO_L15P_T2L_N4_AD11P_67	AR15	FMC1 refers to 19th channel data P
FMC1_LA20_N	IO_L24N_T3U_N11_67	AK14	FMC1 refers to 20th channel data N
FMC1_LA20_P	IO_L24P_T3U_N10_67	AJ14	FMC1 refers to 20th channel data P

FMC1_LA21_N	IO_L21N_T3L_N5_AD8N_67	AM14	FMC1 refers to 21th channel data N
FMC1_LA21_P	IO_L21P_T3L_N4_AD8P_67	AL14	FMC1 refers to 21th channel data P
FMC1_LA22_N	IO_L20N_T3L_N3_AD1N_67	AK15	FMC1 refers to 22th channel data N
FMC1_LA22_P	IO_L20P_T3L_N2_AD1P_67	AJ15	FMC1 refers to 22th channel data P
FMC1_LA23_N	IO_L23N_T3U_N9_67	AN13	FMC1 refers to 23th channel data N
FMC1_LA23_P	IO_L23P_T3U_N8_67	AM13	FMC1 refers to 23th channel data P
FMC1_LA24_N	IO_L9N_T1L_N5_AD12N_67	AW10	FMC1 refers to 24th channel data N
FMC1_LA24_P	IO_L9P_T1L_N4_AD12P_67	AW11	FMC1 refers to 24th channel data P
FMC1_LA25_N	IO_L14N_T2L_N3_GC_67	AR10	FMC1 refers to 25th channel data N
FMC1_LA25_P	IO_L14P_T2L_N2_GC_67	AP10	FMC1 refers to 25th channel data P
FMC1_LA26_N	IO_L19N_T3L_N1_DBC_AD9N_67	AM15	FMC1 refers to 26th channel data N
FMC1_LA26_P	IO_L19P_T3L_N0_DBC_AD9P_67	AL15	FMC1 refers to 26th channel data P
FMC1_LA27_N	IO_L22N_T3U_N7_DBC_AD0N_67	AP14	FMC1 refers to 27th channel data N
FMC1_LA27_P	IO_L22P_T3U_N6_DBC_AD0P_67	AN14	FMC1 refers to 27th channel data P
FMC1_LA28_N	IO_L10N_T1U_N7_QBC_AD4N_67	AV8	FMC1 refers to 28th channel data N
FMC1_LA28_P	IO_L10P_T1U_N6_QBC_AD4P_67	AV9	FMC1 refers to 28th channel data P
FMC1_LA29_N	IO_L1N_T0L_N1_DBC_67	AY9	FMC1 refers to 29th channel data N
FMC1_LA29_P	IO_L1P_T0L_N0_DBC_67	AW9	FMC1 refers to 29th channel data P
FMC1_LA30_N	IO_L2N_T0L_N3_67	BB8	FMC1 refers to 30th channel data N
FMC1_LA30_P	IO_L2P_T0L_N2_67	BB9	FMC1 refers to 30th channel data P
FMC1_LA31_N	IO_L3N_T0L_N5_AD15N_67	AY8	FMC1 refers to 31th channel data N
FMC1_LA31_P	IO_L3P_T0L_N4_AD15P_67	AW8	FMC1 refers to 31th channel data P
FMC1_LA32_N	IO_L5N_T0U_N9_AD14N_67	BB6	FMC1 refers to 32th channel data N
FMC1_LA32_P	IO_L5P_T0U_N8_AD14P_67	BA6	FMC1 refers to 32th channel data P
FMC1_LA33_N	IO_L4N_T0U_N7_DBC_AD7N_67	BA7	FMC1 refers to 33th channel data N
FMC1_LA33_P	IO_L4P_T0U_N6_DBC_AD7P_67	BA8	FMC1 refers to 33th channel data P

FMC1_SDA	IO_L12N_AD8N_94	A4	I2C communication data of FMC1
FMC1_SCL	IO_L11P_AD9P_94	B6	I2C communication clock of FMC1

The 60 pairs of differential signals of the FMC2 expansion port are connected to the IO of the BANK64, 65, 66 of the ZYNQ Ultrascale+ chip, the level standard is 1.8V or 1.2V (chose by hop cap J88), and the differential signal supports LVDS data communication. Eight sets of GTH transceiver signals are connected to BANK224 and BANK225. Figure 18-2 shows the diagram of the ZYNQ Ultrascale+ and FMC2 connectors.

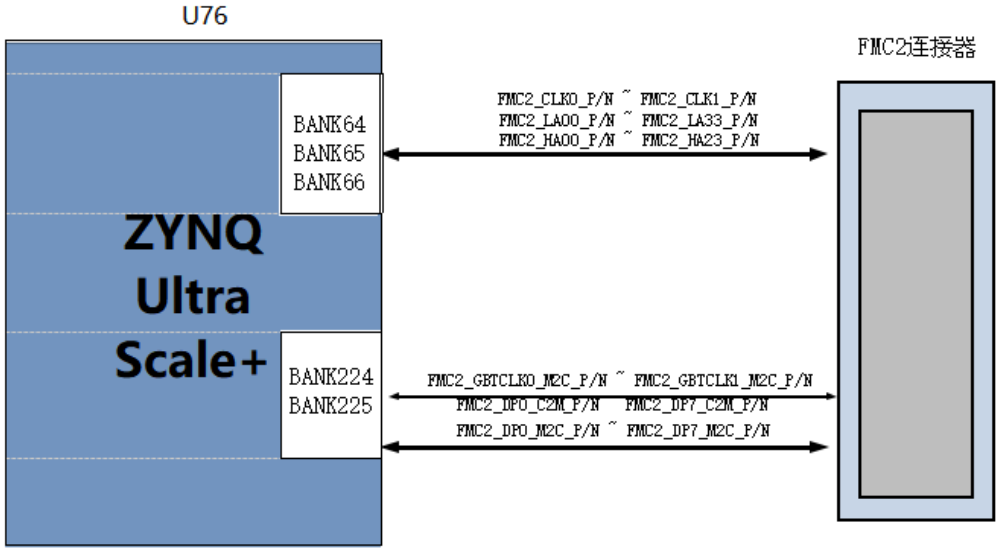


Figure 18-2: Connection of the FMC1 connector

FMC1 connector pin assignment :

Signal Name	ZYNQ Pin Name	Pin No.	Remarks
FMC2_GBTCLK0_M2C_C_N	MGTREFCLK1N_224	AJ9	FMC2 transceiver reference clock 0, Negative
FMC2_GBTCLK0_M2C_C_P	MGTREFCLK1P_224	AJ10	FMC2 transceiver reference clock 0, Positive
FMC2_GBTCLK1_M2C_N	MGTREFCLK0N_224	AK11	FMC2 transceiver reference clock 1, Negative
FMC2_GBTCLK1_M2C_P	MGTREFCLK0P_224	AK12	FMC2 transceiver reference clock 1, Positive
FMC2_DP4_C2M_N	MGTHTXN2_224	AU5	FMC2 transceiver data transmission 4, Negative

FMC2_DP4_C2M_P	MGTHTXP2_224	AU6	FMC2 transceiver data transmission 4, Positive
FMC2_DP4_M2C_N	MGTHRXN2_224	AV3	FMC2 transceiver data reception 4, Negative
FMC2_DP4_M2C_P	MGTHRXP2_224	AV4	FMC2 transceiver data reception 4, Positive
FMC2_DP5_C2M_N	MGTHTXN0_224	AY3	FMC2 transceiver data transmission 5, Negative
FMC2_DP5_C2M_P	MGTHTXP0_224	AY4	FMC2 transceiver data transmission 5, Positive
FMC2_DP5_M2C_N	MGTHRXN0_224	BA1	FMC2 transceiver data reception 5, Negative
FMC2_DP5_M2C_P	MGTHRXP0_224	BA2	FMC2 transceiver data reception 5, Positive
FMC2_DP6_C2M_N	MGTHTXN1_224	AW5	FMC2 transceiver data transmission 6, Negative
FMC2_DP6_C2M_P	MGTHTXP1_224	AW6	FMC2 transceiver data transmission 6, Positive
FMC2_DP6_M2C_N	MGTHRXN1_224	AW1	FMC2 transceiver data reception 6, Negative
FMC2_DP6_M2C_P	MGTHRXP1_224	AW2	FMC2 transceiver data reception 6, Positive
FMC2_DP7_C2M_N	MGTHTXN3_224	AT7	FMC2 transceiver data transmission 7, Negative
FMC2_DP7_C2M_P	MGTHTXP3_224	AT8	FMC2 transceiver data transmission 7, Positive
FMC2_DP7_M2C_N	MGTHRXN3_224	AU1	FMC2 transceiver data reception 7, Negative
FMC2_DP7_M2C_P	MGTHRXP3_224	AU2	FMC2 transceiver data reception 7, Positive
FMC2_DP0_C2M_N	MGTHTXN1_225	AP7	FMC2 transceiver data

			transmission 0, Negative
FMC2_DP0_C2M_P	MGTHTXP1_225	AP8	FMC2 transceiver data transmission 0, Positive
FMC2_DP0_M2C_N	MGTHRXN1_225	AR1	FMC2 transceiver data reception 0, Negative
FMC2_DP0_M2C_P	MGTHRXP1_225	AR2	FMC2 transceiver data reception 0, Positive
FMC2_DP1_C2M_N	MGTHTXN3_225	AM7	FMC2 transceiver data transmission 1, Negative
FMC2_DP1_C2M_P	MGTHTXP3_225	AM8	FMC2 transceiver data transmission 1, Positive
FMC2_DP1_M2C_N	MGTHRXN3_225	AN1	FMC2 transceiver data reception 1, Negative
FMC2_DP1_M2C_P	MGTHRXP3_225	AN2	FMC2 transceiver data reception 1, Positive
FMC2_DP2_C2M_N	MGTHTXN2_225	AN5	FMC2 transceiver data transmission 2, Negative
FMC2_DP2_C2M_P	MGTHTXP2_225	AN6	FMC2 transceiver data transmission 2, Positive
FMC2_DP2_M2C_N	MGTHRXN2_225	AP3	FMC2 transceiver data reception 2, Negative
FMC2_DP2_M2C_P	MGTHRXP2_225	AP4	FMC2 transceiver data reception 2, Positive
FMC2_DP3_C2M_N	MGTHTXN0_225	AR5	FMC2 transceiver data transmission 3, Negative
FMC2_DP3_C2M_P	MGTHTXP0_225	AR6	FMC2 transceiver data transmission 3, Positive
FMC2_DP3_M2C_N	MGTHRXN0_225	AT3	FMC2 transceiver data reception 3, Negative
FMC2_DP3_M2C_P	MGTHRXP0_225	AT4	FMC2 transceiver data reception 3, Positive

FMC2_CLK0_M2C_N	IO_L13N_T2L_N1_GC_64	AT21	FMC2 1st channel reference clock N
FMC2_CLK0_M2C_P	IO_L13P_T2L_N0_GC_64	AT22	FMC2 1st channel reference clock P
FMC2_CLK1_M2C_N	IO_L13N_T2L_N1_GC_65	AT27	FMC2 2nd channel reference clock N
FMC2_CLK1_M2C_P	IO_L13P_T2L_N0_GC_65	AR27	FMC2 2nd channel reference clock P
FMC2_LA00_CC_N	IO_L11N_T1U_N9_GC_64	AV21	FMC2 refers to 0th channel data N
FMC2_LA00_CC_P	IO_L11P_T1U_N8_GC_64	AU21	FMC2 refers to 0th channel data P
FMC2_LA01_CC_N	IO_L12N_T1U_N11_GC_64	AV19	FMC2 refers to 1st channel data N
FMC2_LA01_CC_P	IO_L12P_T1U_N10_GC_64	AU20	FMC2 refers to 1st channel data P
FMC2_LA02_N	IO_L7N_T1L_N1_QBC_64	AV23	FMC2 refers to 2nd channel data N
FMC2_LA02_P	IO_L7P_T1L_N0_QBC_64	AU23	FMC2 refers to 2nd channel data P
FMC2_LA03_N	IO_L9N_T1L_N5 _64	AW19	FMC2 refers to 3rd channel data N
FMC2_LA03_P	IO_L9P_T1L_N4 _64	AW20	FMC2 refers to 3rd channel data P
FMC2_LA04_N	IO_L16N_T2U_N7_QBC_64	AP21	FMC2 refers to 4th channel data N
FMC2_LA04_P	IO_L16P_T2U_N6_QBC_64	AN21	FMC2 refers to 4th channel data P
FMC2_LA05_N	IO_L10N_T1U_N7_QBC_64	AY18	FMC2 refers to 5th channel data N
FMC2_LA05_P	IO_L10P_T1U_N6_QBC_64	AY19	FMC2 refers to 5th channel

			data P
FMC2_LA06_N	IO_L2N_T0L_N3_64	AY22	FMC2 refers to 6th channel data N
FMC2_LA06_P	IO_L2P_T0L_N2_64	AY23	FMC2 refers to 6th channel data P
FMC2_LA07_N	IO_L3N_T0L_N5_64	BA21	FMC2 refers to 7th channel data N
FMC2_LA07_P	IO_L3P_T0L_N4 _64	BA22	FMC2 refers to 7th channel data P
FMC2_LA08_N	IO_L5N_T0U_N9_64	BB19	FMC2 refers to 8th channel data N
FMC2_LA08_P	IO_L5P_T0U_N8_64	BB20	FMC2 refers to 8th channel data P
FMC2_LA09_N	IO_L4N_T0U_N7_DBC_64	BA20	FMC2 refers to 9th channel data N
FMC2_LA09_P	IO_L4P_T0U_N6_DBC_64	AY20	FMC2 refers to 9th channel data P
FMC2_LA10_N	IO_L6N_T0U_N11 _64	BB18	FMC2 refers to 10th channel data N
FMC2_LA10_P	IO_L6P_T0U_N10 _64	BA18	FMC2 refers to 10th channel data P
FMC2_LA11_N	IO_L22N_T3U_N7_DBC_64	AK19	FMC2 refers to 11th channel data N
FMC2_LA11_P	IO_L22P_T3U_N6_DBC_64	AK20	FMC2 refers to 11th channel data P
FMC2_LA12_N	IO_L1N_T0L_N1_DBC_64	BB23	FMC2 refers to 12th channel data N
FMC2_LA12_P	IO_L1P_T0L_N0_DBC_64	BA23	FMC2 refers to 12th channel data P
FMC2_LA13_N	IO_L23N_T3U_N9_64	AJ20	FMC2 refers to 13th channel data N

FMC2_LA13_P	IO_L23P_T3U_N8_64	AJ21	FMC2 refers to 13th channel data P
FMC2_LA14_N	IO_L19N_T3L_N1_DBC_64	AN19	FMC2 refers to 14th channel data N
FMC2_LA14_P	IO_L19P_T3L_N0_DBC_64	AM19	FMC2 refers to 14th channel data P
FMC2_LA15_N	IO_L20N_T3L_N3_64	AM20	FMC2 refers to 15th channel data N
FMC2_LA15_P	IO_L20P_T3L_N2_64	AM21	FMC2 refers to 15th channel data P
FMC2_LA16_N	IO_L21N_T3L_N5_64	AL21	FMC2 refers to 16th channel data N
FMC2_LA16_P	IO_L21P_T3L_N4_64	AL22	FMC2 refers to 16th channel data P
FMC2_LA17_CC_N	IO_L14N_T2L_N3_GC_65	AR25	FMC2 refers to 17th channel data N
FMC2_LA17_CC_P	IO_L14P_T2L_N2_GC_65	AR24	FMC2 refers to 17th channel data P
FMC2_LA18_CC_N	IO_L11N_T1U_N9_GC_65	AU26	FMC2 refers to 18th channel data N
FMC2_LA18_CC_P	IO_L11P_T1U_N8_GC_65	AU25	FMC2 refers to 18th channel data P
FMC2_LA19_N	IO_L9N_T1L_N5_AD12N_65	AW27	FMC2 refers to 19th channel data N
FMC2_LA19_P	IO_L9P_T1L_N4_AD12P_65	AV27	FMC2 refers to 19th channel data P
FMC2_LA20_N	IO_L10N_T1U_N7_QBC_ 65	AV28	FMC2 refers to 20th channel data N
FMC2_LA20_P	IO_L10P_T1U_N6_QBC_ 65	AU28	FMC2 refers to 20th channel data P
FMC2_LA21_N	IO_L2N_T0L_N3_65	BB25	FMC2 refers to 21th channel

			data N
FMC2_LA21_P	IO_L2P_T0L_N2_65	BB24	FMC2 refers to 21th channel data P
FMC2_LA22_N	IO_L4N_T0U_N7_DBC_ 65	BB26	FMC2 refers to 22th channel data N
FMC2_LA22_P	IO_L4P_T0U_N6_DBC_ 65	BA26	FMC2 refers to 22th channel data P
FMC2_LA23_N	IO_L3N_T0L_N5_AD15N_65	BA25	FMC2 refers to 23th channel data N
FMC2_LA23_P	IO_L3P_T0L_N4_AD15P_65	AY25	FMC2 refers to 23th channel data P
FMC2_LA24_N	IO_L12N_T1U_N11_GC_65	AT26	FMC2 refers to 24th channel data N
FMC2_LA24_P	IO_L12P_T1U_N10_GC_65	AT25	FMC2 refers to 24th channel data P
FMC2_LA25_N	IO_L15N_T2L_N5_AD11N_65	AN26	FMC2 refers to 25th channel data N
FMC2_LA25_P	IO_L15P_T2L_N4_AD11P_65	AM26	FMC2 refers to 25th channel data P
FMC2_LA26_N	IO_L1N_T0L_N1_DBC_65	AY24	FMC2 refers to 26th channel data N
FMC2_LA26_P	IO_L1P_T0L_N0_DBC_65	AW24	FMC2 refers to 26th channel data P
FMC2_LA27_P	IO_L5N_T0U_N9_AD14N_65	AY28	FMC2 refers to 27th channel data N
FMC2_LA27_N	IO_L5P_T0U_N8_AD14P_65	AY27	FMC2 refers to 27th channel data P
FMC2_LA28_N	IO_L6N_T0U_N11_AD6N_65	BB28	FMC2 refers to 28th channel data N
FMC2_LA28_P	IO_L6P_T0U_N10_AD6P_65	BA28	FMC2 refers to 28th channel data P

FMC2_LA29_N	IO_L19N_T3L_N1_DBC_ 65	AT23	FMC2 refers to 29th channel data N
FMC2_LA29_P	IO_L19P_T3L_N0_DBC_ 65	AR23	FMC2 refers to 29th channel data P
FMC2_LA30_N	IO_L22N_T3U_N7_DBC_ 65	AN23	FMC2 refers to 30th channel data N
FMC2_LA30_P	IO_L22P_T3U_N6_DBC_ 65	AM23	FMC2 refers to 30th channel data P
FMC2_LA31_N	IO_L23N_T3U_N9 65	AL23	FMC2 refers to 31th channel data N
FMC2_LA31_P	IO_L23P_T3U_N8_ 65	AK23	FMC2 refers to 31th channel data P
FMC2_LA32_N	IO_L20N_T3L_N3_AD1N_65	AP25	FMC2 refers to 32th channel data N
FMC2_LA32_P	IO_L20P_T3L_N2_AD1P_65	AP24	FMC2 refers to 32th channel data P
FMC2_LA33_N	IO_L21N_T3L_N5_AD8N_65	AN24	FMC2 refers to 33th channel data N
FMC2_LA33_P	IO_L21P_T3L_N4_AD8P_65	AM24	FMC2 refers to 33th channel data P
FMC2_HA00_CC_N	IO_L11N_T1U_N9_GC_66	AW14	FMC2 High-level reference 0th channel data (clock) N
FMC2_HA00_CC_P	IO_L11P_T1U_N8_GC_66	AW15	FMC2 High-level reference 0th channel data (clock) P
FMC2_HA01_CC_N	IO_L12N_T1U_N11_GC_66	AV14	FMC2 High-level reference 1st channel data (clock) N
FMC2_HA01_CC_P	IO_L12P_T1U_N10_GC_66	AU14	FMC2 High-level reference 1st channel data (clock) P
FMC2_HA02_N	IO_L23N_T3U_N9_66	AM16	FMC2 High-level 2nd data N
FMC2_HA02_P	IO_L23P_T3U_N8_66	AL16	FMC2 High-level 2nd data P
FMC2_HA03_N	IO_L22N_T3U_N7_DBC_ 66	AK17	FMC2 High-level 3rd data N

FMC2_HA03_P	IO_L22P_T3U_N6_DBC_ 66	AJ17	FMC2 High-level 3rd data P
FMC2_HA04_N	IO_L15N_T2L_N5_AD11N_66	AV18	FMC2 High-level 4th data N
FMC2_HA04_P	IO_L15P_T2L_N4_AD11P_66	AU18	FMC2 High-level 4th data P
FMC2_HA05_N	IO_L19N_T3L_N1_DBC_ 66	AK18	FMC2 High-level 5th data N
FMC2_HA05_P	IO_L19P_T3L_N0_DBC_ 66	AJ18	FMC2 High-level 5th data P
FMC2_HA06_N	IO_L14N_T2L_N3_GC_66	AU15	FMC2 High-level 6th data N
FMC2_HA06_P	IO_L14P_T2L_N2_GC_66	AT15	FMC2 High-level 6th data P
FMC2_HA07_N	IO_L24N_T3U_N11_66	AP16	FMC2 High-level 7th data N
FMC2_HA07_P	IO_L24P_T3U_N10_66	AN16	FMC2 High-level 7th data P
FMC2_HA08_N	IO_L16N_T2U_N7_QBC_ 66	AT18	FMC2 High-level 8th data N
FMC2_HA08_P	IO_L16P_T2U_N6_QBC_ 66	AR18	FMC2 High-level 8th data P
FMC2_HA09_N	IO_L17N_T2U_N9_AD10N_66	AT17	FMC2 High-level 9th data N
FMC2_HA09_P	IO_L17P_T2U_N8_AD10P_66	AR17	FMC2 High-level 9th data P
FMC2_HA10_N	IO_L5N_T0U_N9_AD14N_66	AY14	FMC2 High-level 10th data N
FMC2_HA10_P	IO_L5P_T0U_N8_AD14P_66	AY15	FMC2 High-level 10th data P
FMC2_HA11_N	IO_L10N_T1U_N7_QBC_ 66	AV13	FMC2 High-level 11th data N
FMC2_HA11_P	IO_L10P_T1U_N6_QBC_ 66	AU13	FMC2 High-level 11th data P
FMC2_HA12_N	IO_L20N_T3L_N3_AD1N_66	AM18	FMC2 High-level 12th data N
FMC2_HA12_P	IO_L20P_T3L_N2_AD1P_66	AL18	FMC2 High-level 12th data P
FMC2_HA13_N	IO_L18N_T2U_N11_AD2N_66	AU16	FMC2 High-level 13th data N
FMC2_HA13_P	IO_L18P_T2U_N10_AD2P_66	AT16	FMC2 High-level 13th data P
FMC2_HA14_N	IO_L7N_T1L_N1_QBC_ 66	BA12	FMC2 High-level 14th data N
FMC2_HA14_P	IO_L7P_T1L_N0_QBC_ 66	AY12	FMC2 High-level 14th data P

FMC2_HA15_N	IO_L8N_T1L_N3_AD5N_66	BB11	FMC2 High-level 15th data N
FMC2_HA15_P	IO_L8P_T1L_N2_AD5P_66	BA11	FMC2 High-level 15th data P
FMC2_HA16_N	IO_L9N_T1L_N5_AD12N_66	BB10	FMC2 High-level 16th data N
FMC2_HA16_P	IO_L9P_T1L_N4_AD12P_66	BA10	FMC2 High-level 16th data P
FMC2_HA17_CC_N	IO_L13N_T2L_N1_GC_ 66	AV16	FMC2 High-level 17th data N
FMC2_HA17_CC_P	IO_L13P_T2L_N0_GC_ 66	AV17	FMC2 High-level 17th data P
FMC2_HA18_N	IO_L6N_T0U_N11_AD6N_66	BB13	FMC2 High-level 18th data N
FMC2_HA18_P	IO_L6P_T0U_N10_AD6P_66	BA13	FMC2 High-level 18th data P
FMC2_HA19_N	IO_L21N_T3L_N5_AD8N_66	AN17	FMC2 High-level 19th data N
FMC2_HA19_P	IO_L21P_T3L_N4_AD8P_66	AN18	FMC2 High-level 19th data P
FMC2_HA20_N	IO_L3N_T0L_N5_AD15N_66	AW16	FMC2 High-level 20th data N
FMC2_HA20_P	IO_L3P_T0L_N4_AD15P_66	AW17	FMC2 High-level 20th data P
FMC2_HA21_N	IO_L4N_T0U_N7_DBC_ 66	BB15	FMC2 High-level 21th data N
FMC2_HA21_P	IO_L4P_T0U_N6_DBC_ 66	BA15	FMC2 High-level 21th data P
FMC2_HA22_N	IO_L2N_T0L_N3_66	BB16	FMC2 High-level 22th data N
FMC2_HA22_P	IO_L2P_T0L_N2_66	BA16	FMC2 High-level 22th data P
FMC2_HA23_N	IO_L1N_T0L_N1_DBC_66	BA17	FMC2 High-level 23th data N
FMC2_HA23_P	IO_L1P_T0L_N0_DBC_66	AY17	FMC2 High-level 23th data P
FMC2_SDA	IO_L11N_AD9N_94	B5	I2C communication data of FMC2

FMC2_SCL	IO_L5N_HDGC_94	D3	I2C communication clock of FMC2

19. PCIE Interface

The Z19 development board is equipped with a slot for main-mode PCIE x8 for connecting PCIE peripherals with single-channel communication speeds of up to 5Gbps. The PCIE signal is directly connected to the BANK226 and BANK227' s transceiver of ZU19EG. The reference clock of the connector is provided by the adjustable clock chip Si5332BD11025-4. Figure 19-1 shows the design of PCIE x 8.

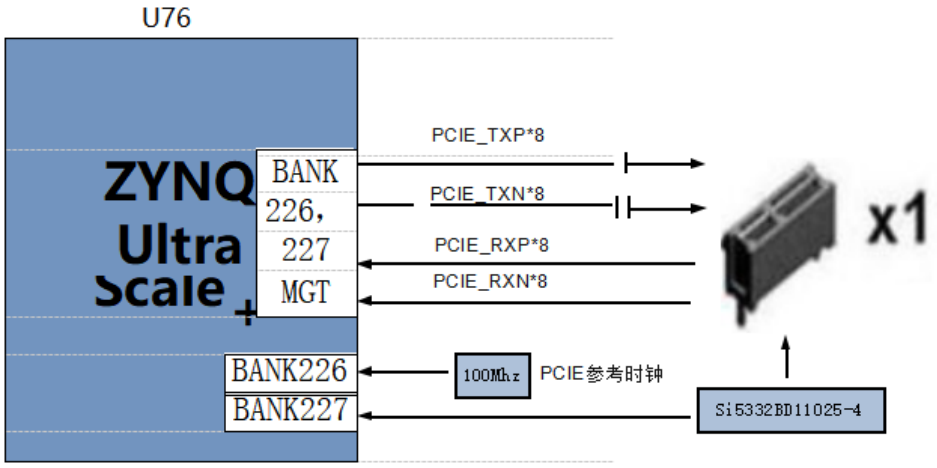


Figure 19-1: The design of PCIE interface

PCIE interface ZYNQ pin assignment:

Signal Name	Pin Name	Pin Number	Remarks
PCIE_RX0_N	MGTHRXN3_227	AE1	PCIE data reception 0 Negative
PCIE_RX0_P	MGTHRXP3_227	AE2	PCIE data reception 0 Positive
PCIE_RX1_N	MGTHRXN2_227	AF3	PCIE data reception 1 Negative
PCIE_RX1_P	MGTHRXP2_227	AF4	PCIE data reception 1 Positive
PCIE_RX2_N	MGTHRXN1_227	AG1	PCIE data reception 2 Negative

PCIE_RX2_P	MGTHRXP1_227	AG2	PCIE data reception 2 Positive
PCIE_RX3_N	MGTHRXN0_227	AH3	PCIE data reception 3 Negative
PCIE_RX3_P	MGTHRXP0_227	AH4	PCIE data reception 3 Positive
PCIE_RX4_N	MGTHRXN3_226	AJ1	PCIE data reception 4 Negative
PCIE_RX4_P	MGTHRXP3_226	AJ2	PCIE data reception 4 Positive
PCIE_RX5_N	MGTHRXN2_226	AK3	PCIE data reception 5 Negative
PCIE_RX5_P	MGTHRXP2_226	AK4	PCIE data reception 5 Positive
PCIE_RX6_N	MGTHRXN1_226	AL1	PCIE data reception 6 Negative
PCIE_RX6_P	MGTHRXP1_226	AL2	PCIE data reception 6 Positive
PCIE_RX7_N	MGTHRXN0_226	AM3	PCIE data reception 7 Negative
PCIE_RX7_P	MGTHRXP0_226	AM4	PCIE data reception 7 Positive
PCIE_TX0_N	MGTHTXN3_227	AD7	PCIE data transmission 0 Negative
PCIE_TX0_P	MGTHTXP3_227	AD8	PCIE data transmission 0 Positive
PCIE_TX1_N	MGTHTXN2_227	AE5	PCIE data transmission 1 Negative
PCIE_TX1_P	MGTHTXP2_227	AE6	PCIE data transmission 1 Positive
PCIE_TX2_N	MGTHTXN1_227	AF7	PCIE data transmission 2 Negative
PCIE_TX2_P	MGTHTXP1_227	AF8	PCIE data transmission 2 Positive
PCIE_TX3_N	MGTHTXN0_227	AG5	PCIE data transmission 3 Negative
PCIE_TX3_P	MGTHTXP0_227	AG6	PCIE data transmission 3 Positive
PCIE_TX4_N	MGTHTXN3_226	AH7	PCIE data transmission 4 Negative

PCIE_TX4_P	MGTHTXP3_226	AH8	PCIE data transmission 4 Positive
PCIE_TX5_N	MGTHTXN2_226	AJ5	PCIE data transmission 5 Negative
PCIE_TX5_P	MGTHTXP2_226	AJ6	PCIE data transmission 5 Positive
PCIE_TX6_N	MGTHTXN1_226	AK7	PCIE data transmission 6 Negative
PCIE_TX6_P	MGTHTXP1_226	AK8	PCIE data transmission 6 Positive
PCIE_TX7_N	MGTHTXN0_226	AL5	PCIE data transmission 7 Negative
PCIE_TX7_P	MGTHTXP0_226	AL6	PCIE data transmission 7 Positive
226_PCIE_CLK_N	MGTREFCLK0N_226	AF11	PCIE reference clock Negative
226_PCIE_CLK_P	MGTREFCLK0P_226	AF12	PCIE reference clock Positive
227_PCIE_CLK_N	MGTREFCLK0N_227	AD11	PCIE reference clock Negative
227_PCIE_CLK_P	MGTREFCLK0P_227	AD12	PCIE reference clock Positive

20. SATA Interface

The Z19 development board is equipped with 4 SATA interfaces, and the SATA differential signal is connected to the GTH BANK228.

SATA's reference clock of 150Mhz is provided by the programmable clock chip Si5332BD11025-4. Figure 20-1 shows the design of SATA interface.

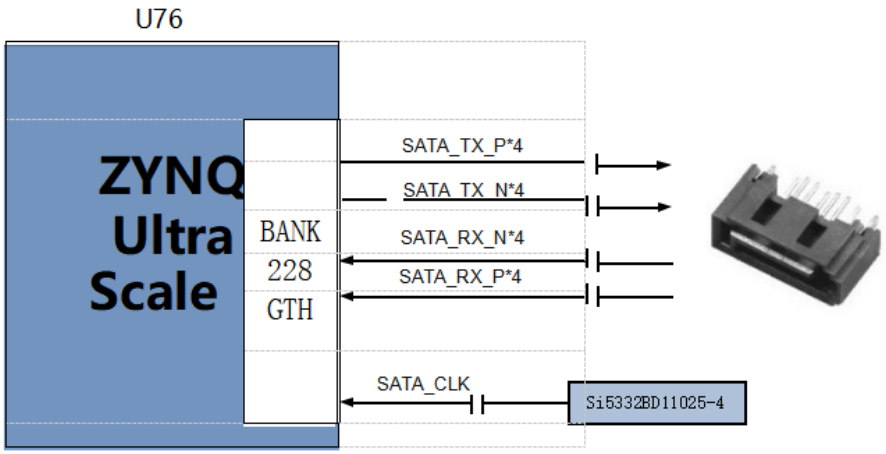


Figure 20-1: The design of SATA interface

SATA interface ZYNQ pin assignment:

Signal Name	Pin Name	Pin Number	Remarks

SATA1_RX_N	MGTHRXN0_228	AD3	SATA1 data reception Negative
SATA1_RX_P	MGTHRXP0_228	AD4	SATA1 data reception Positive
SATA2_RX_N	MGTHRXN1_228	AC1	SATA2 data reception Negative
SATA2_RX_P	MGTHRXP1_228	AC2	SATA2 data reception Positive
SATA3_RX_N	MGTHRXN2_228	AB3	SATA3 data reception Negative
SATA3_RX_P	MGTHRXP2_228	AB4	SATA3 data reception Positive
SATA4_RX_N	MGTHRXN3_228	AA1	SATA4 data reception Negative
SATA4_RX_P	MGTHRXP3_228	AA2	SATA4 data reception Positive
SATA1_TX_N	MGTHTXN0_228	AC5	SATA1 data transmission Negative
SATA1_TX_P	MGTHTXP0_228	AC6	SATA1 data transmission Positive
SATA2_TX_N	MGTHTXN1_228	AB7	SATA2 data transmission Negative
SATA2_TX_P	MGTHTXP1_228	AB8	SATA2 data transmission Positive
SATA3_TX_N	MGTHTXN2_228	AA5	SATA3 data transmission Negative
SATA3_TX_P	MGTHTXP2_228	AA6	SATA3 data transmission Positive
SATA4_TX_N	MGTHTXN3_228	Y7	SATA4 data transmission Negative
SATA4_TX_P	MGTHTXP3_228	Y8	SATA4 data transmission Positive
SATA_CLK_N	MGTREFCLK0N_228	AB11	SATA reference clock Negative
SATA_CLK_P	MGTREFCLK0P_228	AB12	SATA reference clock Positive

21. SMA Interface

The Z19 development board has three pairs of differential lines, which are drawn through six SMA interfaces, one pair is clock signal and the other two pairs are data signals. The differential signal is connected to the IO of the BANK68 (level standard 1.8V or 1.2V and can be adjusted via hop cap). Figure 21-1 shows the design of SMA interface.

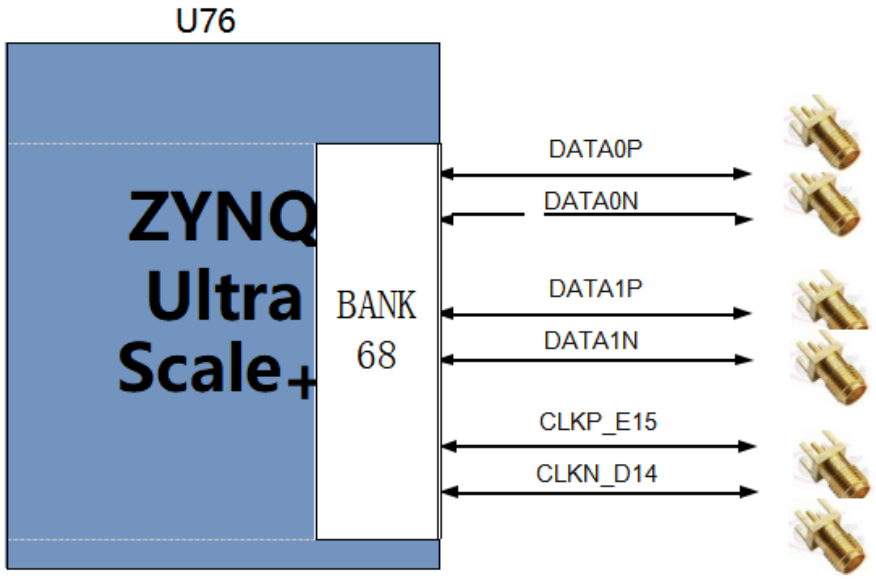


Figure 21-1: The design of SMA interface

SMA interface ZYNQ pin assignment:

Signal Name	Pin Name	Pin No.	Description
CLKN_D14	IO_L14N_T2L_N3_GC_68	D14	SMA clock Negative
CLKP_E15	IO_L14P_T2L_N2_GC_68	E15	SMA clock Positive
DATA0N	IO_L18N_T2U_N11_AD2N_68	B15	SMA data 0 reception Negative
DATA0P	IO_L18P_T2U_N10_AD2P_68	C15	SMA data 0 reception Positive
DATA1N	IO_L10N_T1U_N7_QBC_AD4N_68	F18	SMA data 1 reception Negative

DATA1P	IO_L10P_T1U_N6_QBC_AD4P_68	G18	SMA data 1 reception Positive

22. JTAG Debugging Interface

A JTAG interface is reserved on the Z19 development board for downloading ZYNQ UltraScale+ applications or curing applications to FLASH. In order to avoid damage to the ZYNQ UltraScale+ chip due to live plugging, we add a protective diode on the JTAG signal to ensure that the signal voltage is within the range accepted by the FPGA.

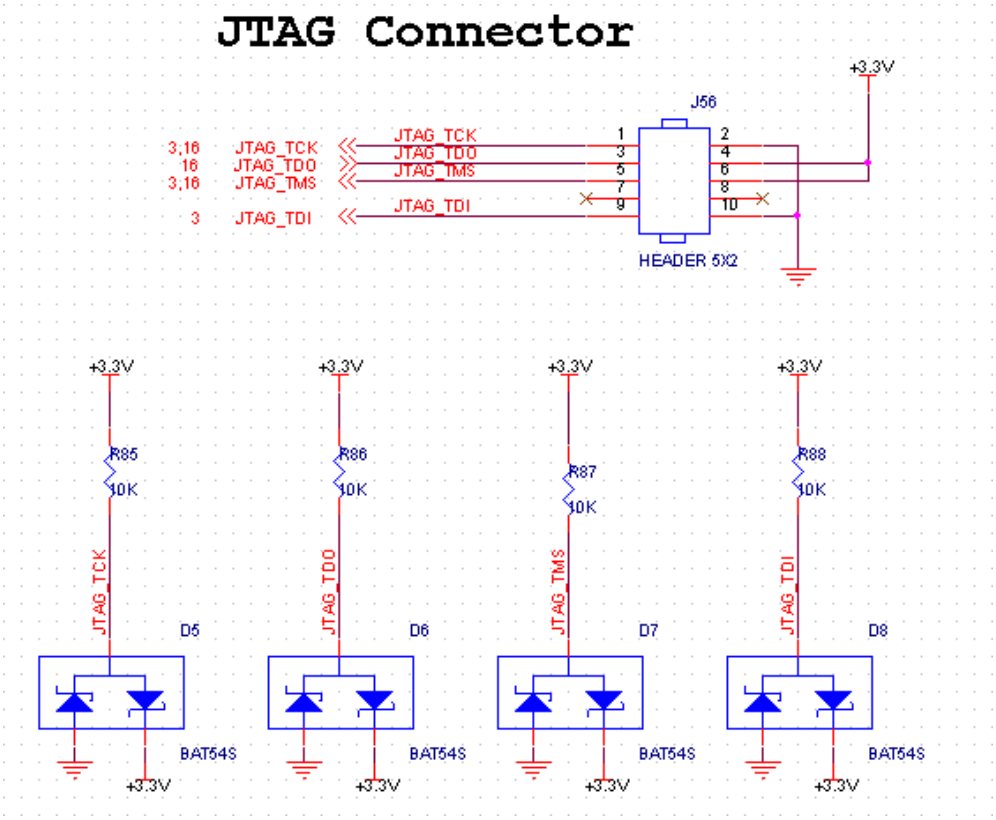


Figure 22-1: JTAG interfaces in the schematic diagram

23. RTC Real-time Clock

The ZU19EG chip has the function of RTC real-time clock inside, with year, month, day, minute and second and week timing function. The external of chip needs to be connected to a 32.768KHz passive clock to provide an accurate clock source to the internal clock circuit, so that the RTC can accurately provide clock information. At the same time, in order to make the real-time clock run normally after the power failure of

the product, it generally needs another battery to supply power to the clock chip. The 2pin 1.27mm spacing interface J22 is reserved on the development board for external battery connection. When the system is powered off, the button battery can also supply power to the RTC system and provide continuous time information. Figure 23-1 shows the schematic diagram of the RTC real-time clock.

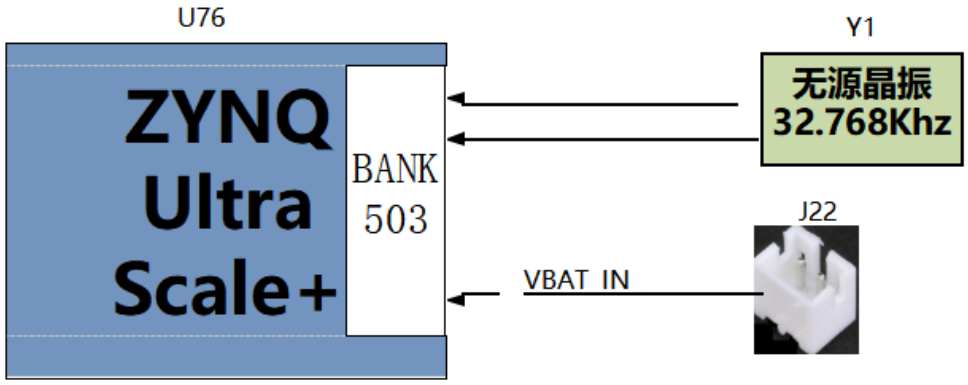


Figure 23-1: The schematic diagram of the RTC real-time clock

24. EEPROM and Temperature Sensor

The Z19 development board carries an EEPROM (Model: 24LC04, Capacity: 4Kbit (2*256*8bit)), which is connected to the PS side through the IIC bus for communication. The board also carries a high-precision, low-power consumption, digital temperature sensor chip called ON Semiconductor's LM75, which has a temperature accuracy of 0.5 degrees. The EEPROM and temperature sensor are mounted to the Bank501 MIO of ZYNQ UltraScale+ via the I2C bus. Figure 24-1 shows the schematic diagram of EEPROM and temperature sensor.

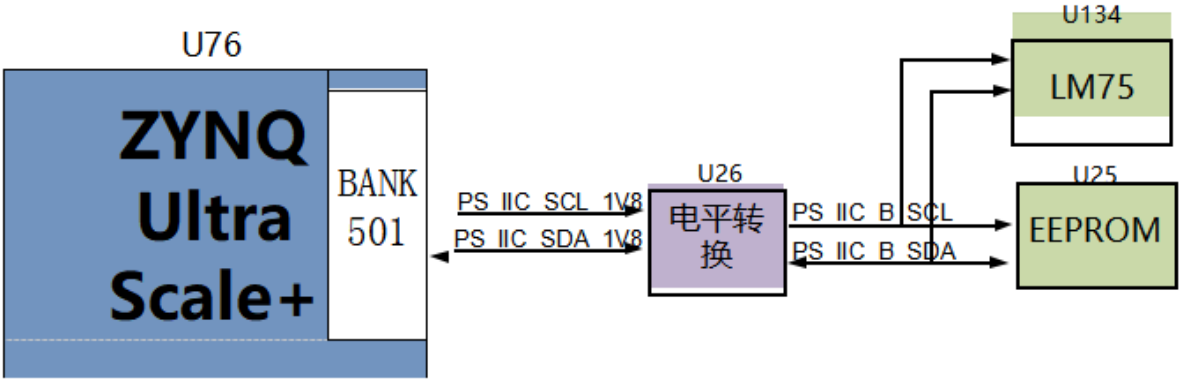


Figure 24-1: The schematic diagram of EEPROM and temperature sensor

25. LED Light

There are 4 LEDs on the Z19 development board, including 1 power indicator, 1 DONE indicator, 1 PS control indicator, 1 PL control indicator. Users can control the on or off through the program. The hardware connection diagram of the user LED light is shown in Figure 25-1:

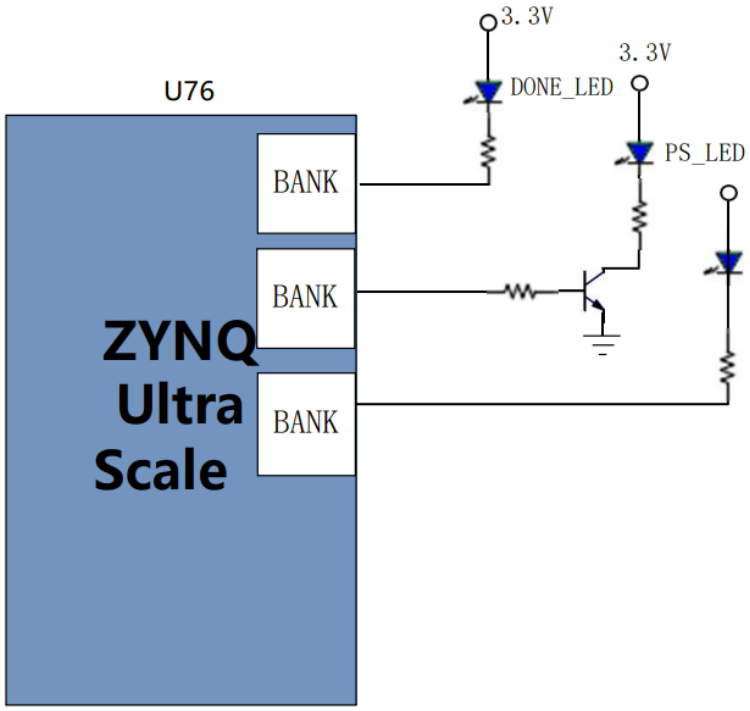


Figure 25-1: The hardware connection diagram of the user LED light

User LED light pin assignment:

Signal Name	Pin Name	Pin Number	Remarks
PS_LED1	PS_MIO42_501	T30	User PS LED Light
PL_LED1	IO_L10P_AD10P_94	B3	User PL LED Light

26. Keys

The Z19 development board has one "RESET" key (attached to the side of the board) and two user keys. The reset signal is connected to the power reset pin of the core board, and users can use this "RESET" key to reset the ZYNQ system. One of the user keys is connected to the MIO of PS, and the other one is connected to the IO of PL. Both

the reset key and user keys are active at low levels. Figure 26-1 shows the connection diagram of user keys:

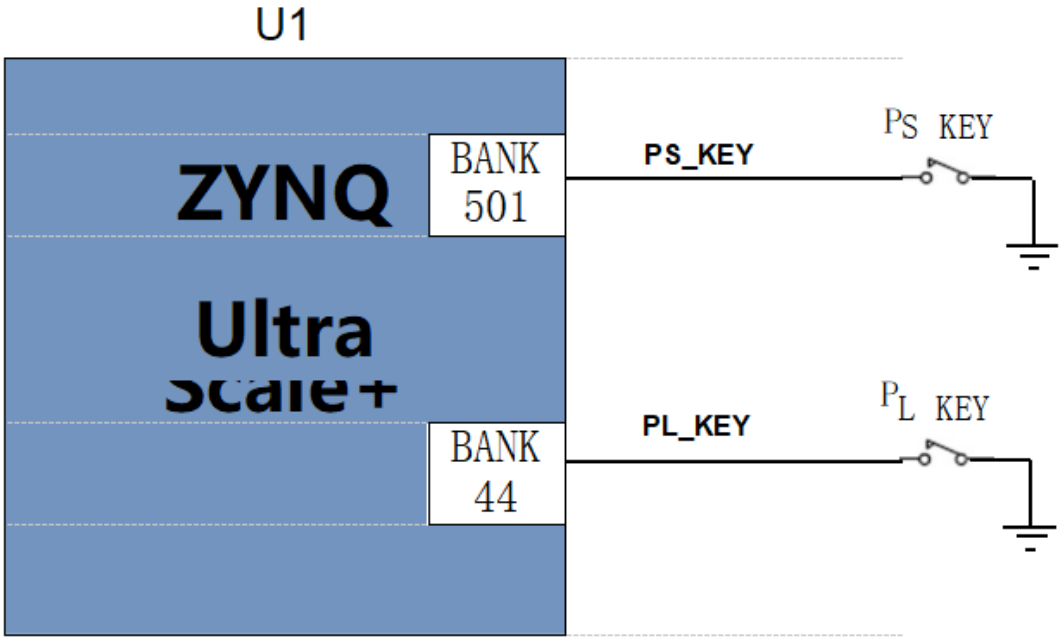


Figure 26-1: The connection diagram of user keys

Keys ZYNQ pin assignment:

Signal Name	Pin Name	Pin Number	Remarks
PS_KEY	PS_MIO26_501	L27	PS key input
PL_KEY	IO_L5P_HDGC_94	D4	PL key input

27. Dip Switch Configuration

There is a 4-bit dip switch SW1 on the development board to configure the startup mode of the ZYNQ system. The Z19 system development platform supports four kinds of startup modes: JTAG debug mode, QSPI FLASH, EMMC and SD2.0 card startup mode. After the ZU9EG chip is powered on, it checks the (PS_MODE0~3) level to determine which startup mode to use. You can select different startup modes by using dip switch SW1 on the expansion board. Table 27-1 shows the startup mode configuration of SW1.

SW1	Dip Position (4, 3, 2, 1)	MODE[3:0]	Startup Mode

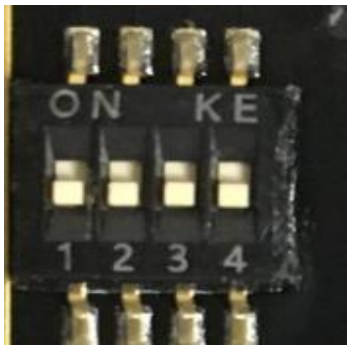
	ON，ON，ON，ON	0000	PS JTAG
	ON，ON，OFF ,ON	0010	QSPI FLASH
	ON，OFF，ON，OFF	0101	SD Card
	ONOFF，OFF，ON	0110	EMMC

Table 27-1: Startup mode configuration of SW1

28. Fan

Because ZU19EG generates a lot of heat when it works properly, we added a cooling fin and fan to the chip on the board to prevent it from overheating. The fan is controlled by ZYNQ chip, and the control pin is connected to the IO of BANK94. If the IO level output is high, the MOSFET tube will be on and the fan will work, if the IO level output is low, the fan will stop work. The design of fan on the board is shown in Figure 28-1:

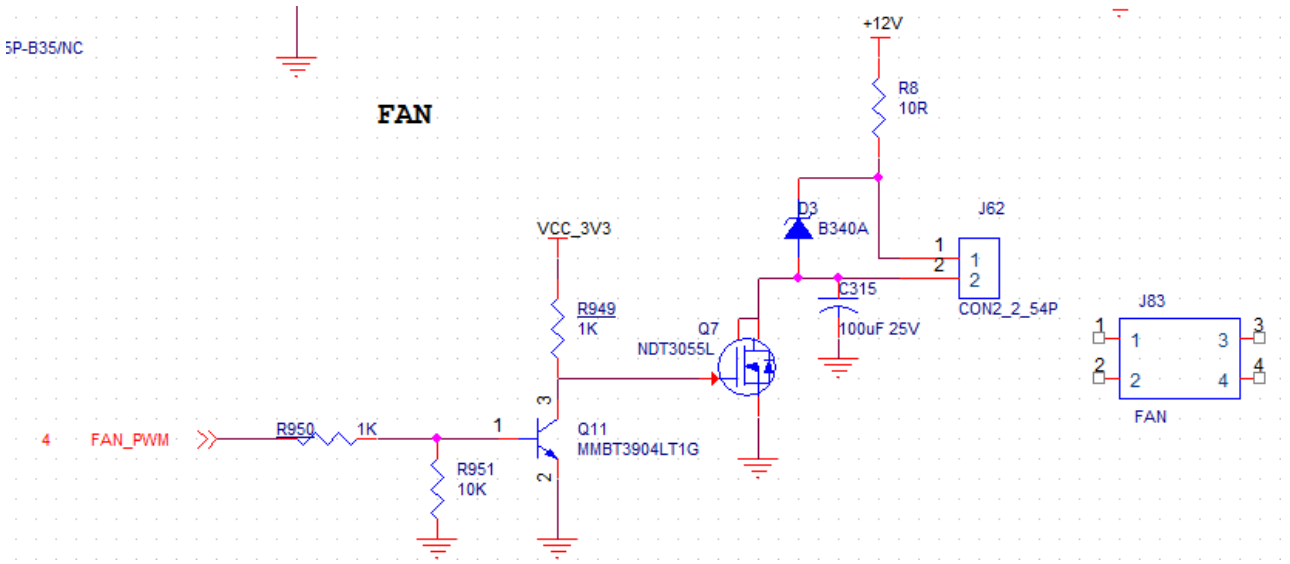


Figure 28-1: The design of fan on the development board

The fan has been fixed on the development board with screws before delivery. The power supply of the fan is connected to the socket of the J62. The red one is positive and the black one is negative.

29. Structure and Dimension

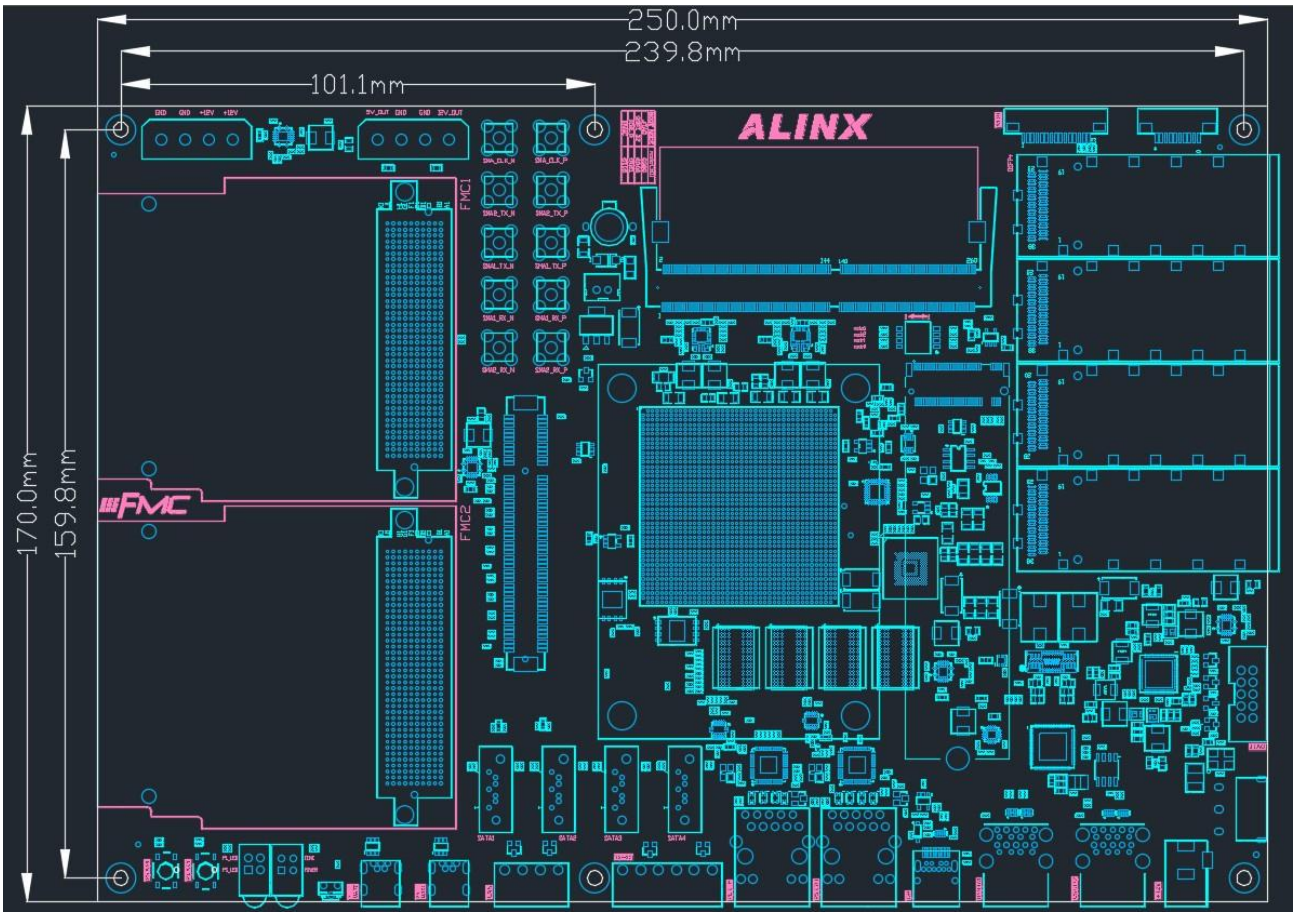


Figure 29-1: Top View